A Study of BER-optimal ADC-based Receiver for Serial Links

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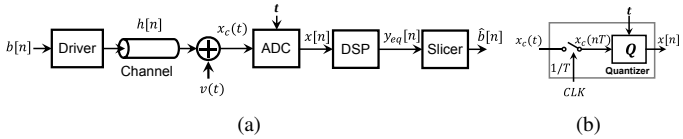
***Abstract*—Analog-to-digital converter (ADC)-based multi-Gb/s serial link receivers have gained increasing attention in the backplane community due to the desire for higher I/O throughput, ease of design portability, and flexibility. However, the power dissipation in such receivers is dominated by the ADC. ADCs in serial links employ signal-to-noise-and-distortion ratio (SNDR) and effective-number-of-bit (ENOB) as performance metrics as these are the standard for generic ADC design. This paper studies the use of information-based metrics such as bit-error-rate (BER) to design a BER-optimal ADC (BOA) for serial links. Channel parameters such as the m-clustering value and the threshold non-uniformity metric h_t are introduced and employed to quantify the BER improvement achieved by a BOA over a conventional uniform ADC (CUA) in a receiver. Analytical expressions for BER improvement are derived and validated through simulations. A prototype BOA is designed, fabricated and tested in a $1.2\,\mathrm{V}$, $90\,\mathrm{nm}$ LP CMOS process to verify the results of this study. BOA's variable-threshold and variable-resolution configurations are implemented via an 8-bit single-core, multiple-output passive digital-to-analog converter (DAC), which incurs an additional power overhead of $< 0.1\%$ (approximately 50 μW). Measurement results show examples in which the BER achieved by the 3-bit BOA receiver is lower by a factor of 10^9 and 10^{10}, as compared to the 4-bit and 3-bit CUA receivers, respectively, at a data rate of 4-Gb/s and a transmitted signal amplitude of 180 $\mathrm{mV_{ppd}}$.**

***Index Terms*—analog-to-digital converter, bit-error-rate, serial links, energy efficiency, mixed-signal**

I. INTRODUCTION

The emergence of analog-to-digital converter (ADC)-based multi-Gb/s serial link receivers [1], [2], [3], [4], [5], [6] has enabled the application of digital signal processing (DSP) techniques to recover data under severe channel impairments such as channel loss, reflection, and crosstalk while being constrained by a stringent power budget. This paper studies the effectiveness of employing *information-based metrics* such as the link bit-error-rate (BER) in reducing the energy consumption of serial link components such as the ADC, which tends to be the most power hungry block, e.g., the ADC itself (excluding the clock buffer) consumes 41% of the total receiver power in [4].

In conventional serial links (see Fig. 1(a)), the ADC is designed to be a transparent conduit of the input analog waveform $x_c(t)$. In such ADCs, the quantization thresholds $\boldsymbol{t}$ are set uniformly within their full scale range (FSR). We refer to such an ADC as a *conventional uniform ADC* (CUA). The signal-to-quantization noise ratio (SQNR) of a CUA can be approximated by $SQNR = 6.02B_x + 4.8 - 20\log_{10}(V_{max}/\sigma_x)$ [7], where σ_x^2 is the average signal power at the ADC input and V_{max} is the maximum input amplitude. The SQNR is a *signal fidelity* metric as it measures the average squared difference between the ADCs sampled input $x_c(nT)$ and its quantized output $x[n]$. Other signal fidelity based metrics such as signal-to-noise-and-distortion-ratio (SNDR) or effective-number-of-bits (ENOB) are also employed. Such fidelity-based metrics impose overly stringent specifications on the ADC because they ignore the true role of the ADC in a communication link, which is to preserve the *information content* in the input signal $x_c(t)$ in order to recover the transmitted data reliably. One direct consequence of employing fidelity-based metrics is that the ADC needs more resolution B_x than needed. In such ADCs, a single bit reduction in B_x can result in significant power savings. For example, in flash ADCs, the area, power consumption, and input capacitance increase exponentially with B_x. These result in large preamplifier bandwidth and multiple stages of latches which exacerbate the ADC power consumption problem [8], [9]. Therefore, the design of low-power and high-speed ADCs in serial links is a major challenge, which has drawn great interest from both industry and academia.



(a) (b)

Figure 1. Role of an ADC in a serial link: (a) block diagram of a serial link, and (b) idealized model for the ADC in (a).

This paper investigates the use of the link BER for designing a BER-optimal ADC (BOA) in serial links. Past work on BER-optimal link components includes [10], in which an adaptive minimum BER (AMBER) algorithm is proposed to adapt the equalizer coefficients. It was shown that minimum-BER equalizers outperform conventional minimum mean square error (MMSE) equalizers over a wide variety of channels especially when the BER lies in a regime of rapid descent with the number of equalizer coefficients. Chen, et al. [11] demonstrated the benefits of adapting the transmit and receive equalizer coefficients, and the sampling phase of the clock-data-recovery (CDR), to minimize the BER in serial links via the design of a prototype IC in $65\,\mathrm{nm}$ CMOS for a $6.25\,\mathrm{Gb/s}$ serial link. In [12], [13], an algorithm to determine the BOA representation levels was proposed. The *ADC shaping gain* $SG(p_e, B_u, B_o)$ defined below, was employed to quantify the benefits of BER optimality

$$SG(p_e, B_u, B_o) = SNR_u(p_e, B_u) - SNR_o(p_e, B_o), \quad (1)$$

where $SNR_u(p_e, B_u)$ and $SNR_o(p_e, B_o)$ are the signal-to-noise ratios (SNRs) needed by a CUA and a BOA, respectively, to achieve a BER equal to p_e with identical receiver processing, and B_u and B_o are the resolutions of the CUA and the BOA, respectively. This metric quantifies the reduction in the channel SNR necessary in order to achieve a given BER p_e due to the use of a BOA. The ADC shaping gain is analogous to a coding gain when evaluating links with error control coding. It was shown in [12], [13] that $SG(10^{-12}, 3, 3)$

ranged from $2.5\,\mathrm{dB}$ to more than $30\,\mathrm{dB}$ for highly dispersive channels. We note that a BOA employs representation levels that are dependent on signal statistics and BER, and hence are typically non-uniformly spaced within the FSR of the ADC. The work in [12], [13] also showed that the non-uniform BOA representation levels are significantly different from and superior to the non-uniform (also signal statistics-dependent) representation levels obtained from the well-known Lloyd-Max (LM) quantization algorithm [14], [15]. This is because the LM algorithm minimizes the SQNR, which is also a fidelity metric. In [16], it was shown that BOA can relax the component specifications of ADCs. In particular, BOA can achieve the same or even better BER while it has less stringent metastability and preamplifiler bandwidth requirements on the ADC comparators.

A power optimized ADC-based $10\,\mathrm{Gb/s}$ serial link receiver in $65\,\mathrm{nm}$ CMOS was designed in [4] using a low-gain analog and mixed-mode pre-equalizer in conjunction with non-uniform representation levels for the ADC. The work in [4], [17] proposes to merge slicers whose thresholds are similar into one for loop-unrolled decision feedback equalizers (DFEs) and adjusts a pseudo-BER metric (voltage margin) to minimize BER, which in effect emulates a BOA followed by a DFE. However, this technique is applicable only to loop-unrolled DFEs, and has to rely on a continuous-time linear equalizer to cancel the precursor ISI. In contrast, our solution employs the true system BER to adjust the ADC thresholds, and is applicable to ADC-based receivers with different equalizer designs. Second, as mentioned in [17], their procedure to determine the optimal threshold placement is not suitable for online calibration. In contrast, our solution employs a standard gradient descent algorithm to compute the thresholds iteratively, and is able to adapt the ADC thresholds online. More recently, Son, et al. [18] proposed a power efficient equalizing receiver front-end that includes a two-step adaptive BER-minimizing equalizer algorithm. These works demonstrate that the use of information-based metrics such as the BER are indeed quite effective in reducing link component power in serial links.

In [13], BOA benefits under various channels, modulation and equalization techniques were studied and presented. This work augments the results presented in [13] with the following three new contributions. First, we study, through analysis and simulations, the benefits of the BOA over the CUA in a serial link receiver. In particular, we propose two channel-dependent parameters to quantify these benefits: 1) m-clustering value, and 2) the threshold non-uniformity metric h_t. Furthermore, we show that the BER improvement is greater than 10^6 when $m \geq 5$ and $h_t \leq 0.8$ for a family of channels. Second, we present the design of a $4\,\mathrm{GS/s}$, 4-bit BOA IC in a $90\,\mathrm{nm}$ CMOS process that includes a single-core, multiple-output passive DAC to enable a variable-threshold and variable-resolution ADC configuration and verify the aforementioned analysis. Measured results demonstrate that a 3-bit BOA has lower SNR requirement than a 4-bit CUA, thereby supporting the claims in [12], [13], [16] in the presence of non-idealities, such as finite sampling bandwidth and metastability. In the process, we demonstrate conclusively that ENOB is not the best metric when designing ADCs for serial links. Third, we propose architectures to implement the gradient descent algorithm in [12], [13] which is employed to compute the representation levels iteratively. In particular, architectures for the quantization level update unit (QL-UD) and the individual representation level update (RL-UD) block are proposed.

The rest of this paper is organized as follows. Section II reviews the theory behind the BOA. Section III discusses how to maximize the benefits of a BOA receiver over a CUA receiver. In Section IV, the design of a $4\,\mathrm{GS/s}$, 4-bit BOA IC in a $90\,\mathrm{nm}$ CMOS process is described. Both stand-alone ADC and link measurement results are summarized in Section V, and conclusions are drawn in Section VI.

II. BOA REVIEW

In this section, the concept of the BOA is reviewed. Figure 1(a) depicts a typical ADC-based serial link, where the ADC is followed by an equalizer prior to detection. When considering an equivalent discrete-time, symbol-spaced, time-invariant channel corrupted by additive white Gaussian noise (AWGN), and 2-PAM modulation, the channel output at time n is given by

$$x_c[n] = x_c(nT) = \textstyle\sum_{i=0}^{L-1} h[i]b[n-i] + v[n],$$

where $b[n] \in \{\pm 1\}$ is the transmitted sequence, $h[n]$ is the equivalent discrete time channel impulse response (see Fig. 2 for an example) with memory L, and $v[n]$ is AWGN with variance σ_v^2. At the receiver, the processor estimates the transmitted symbols from quantized channel outputs through the ADC. A subsequent slicer determines the transmitted bit. A subsequent slicer determines the transmitted bit. Figure 2 shows an example of the channel response $\boldsymbol{h}$ for a 20" backplane channel carrying $10\,\mathrm{Gb/s}$ data [19].

A. Comparison Metric

Comparison of a BOA and a CUA requires an appropriate metric to be defined. The ADC shaping gain $SG(p_e, B_u, B_o)$ in (1) is one such metric. In applications where it is difficult to measure the underlying circuit and environmental noise, however it is easy to maintain consistent operational conditions between two experiments, comparing the ratio of the resulting bit-error-rates, or "BER ratio" may be of interest. Similarly, when two systems are being compared, and only one of the two experiences an exponential decay in BER with SNR as shown in Fig. 3(e), it may not be possible to measure a "shaping gain" in SNR (i.e. the additional SNR required to achieve the same BER) given a target BER, however at a given SNR, the ratio of the measured BERs may be readily measurable. Once again, the BER ratio becomes a quantity of interest. In our application, the resolution of the ADC may be insufficient to reach the so-called "waterfall" regime of the BER, (i.e.

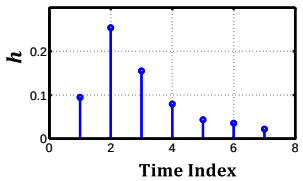


Figure 2. Channel response $\boldsymbol{h} = [0.0949, 0.2539, 0.1552, 0.0793, 0.0435, 0.0356, 0.0220]$ with $L = 7$ of a 20" backplane channel carrying $10\,\mathrm{Gb/s}$ data [19].

where BER falls off exponentially with SNR), we will use this BER ratio as a metric of comparison. We recognize that this metric may be more susceptible to measurement sensitivities, since we are comparing quantities that may differ by orders of magnitude, however we proceed with this metric for the above mentioned reasons. Therefore, in this paper we employ the *BER ratio* (BERR) defined as:

$$BERR(SNR, B_u, B_o) = \frac{p_{eu}(SNR, B_u)}{p_{eo}(SNR, B_o)},$$

where $p_{eu}(SNR, B_u)$ and $p_{eo}(SNR, B_o)$ are the BERs achieved by a B_u-bit CUA and a B_o-bit BOA with identical receiver processing and channel SNR given by $SNR = \sum_{i=0}^{L-1} |h[i]|^2/\sigma_v^2$.

B. An Illustrative Example

A BOA [12] exploits signal statistics to maximize the probability of correctly detecting the transmitted bits. To provide insight into the operation of a BOA, we consider an ADC followed by a memoryless symbol-by-symbol maximum likelihood (ML) detector (ADC-ML) receiver, as shown in Fig. 3(a) and provide an example to illustrate the point.

First, we define the set of quantization thresholds for the CUA and the BOA.

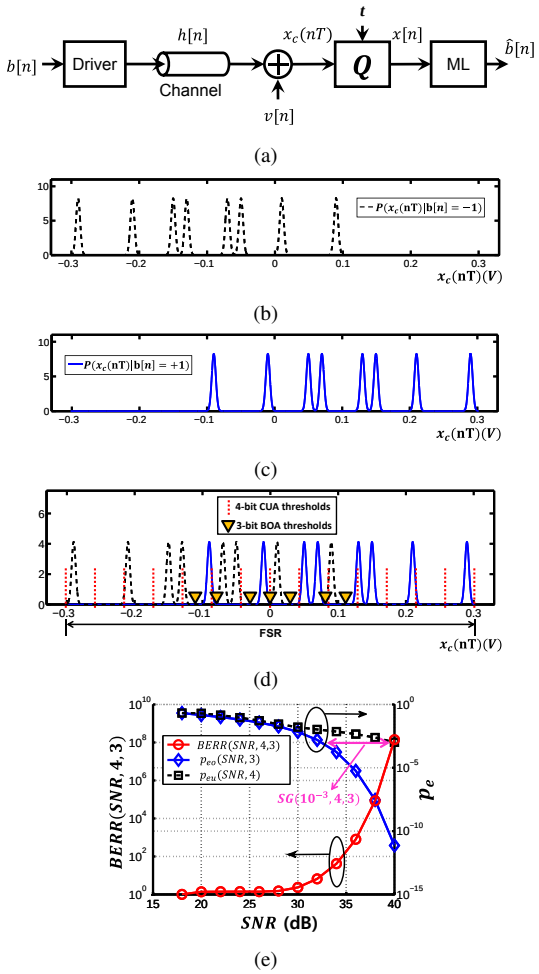


Figure 3. An illustrative example: (a) the block diagram of an ADC-ML receiver, (b) the conditional pdf of the channel output given $b[n] = -1$, (c) the conditional pdf of the channel output given $b[n] = +1$, (d) BOA's quantization thresholds (inverted triangles in yellow) and uniform quantization thresholds (dashed lines in red) for channel $\boldsymbol{h} = [0.08, 0.07, 0.1, 0.04]$ when $SNR = 36\,\text{dB}$, and (e) the simulated $BERR(SNR, 4, 3)$, $p_{eo}(SNR, 3)$ and $p_{eu}(SNR, 4)$ versus SNR plot.

Definition 1. The vectors $\boldsymbol{t}_u = [t_{u,1}, t_{u,2}, \cdots, t_{u,M}]$, $\boldsymbol{r}_u = [r_{u,1}, r_{u,2}, \cdots, r_{u,M+1}]$, and the set $\boldsymbol{I}_u = \{I_{u,1}, I_{u,2}, \cdots, I_{u,M+1}\}$ are the thresholds, output representation levels, and interval set of a $log_2(M+1)$-bit CUA, where $I_{u,1} = (-\infty, t_{u,1}]$, $I_{u,k} = [t_{u,k-1}, t_{u,k}]$ for $k = 2, \cdots, M$, $I_{u,M+1} = [t_{u,M}, +\infty)$, and the CUA output $x[n] = r_{u,k}$ if $x_c(nT) \in I_{u,k}$ for $k = 1, \cdots, M+1$. Similarly, the vectors $\boldsymbol{t}_o = [t_{o,1}, t_{o,2}, \cdots, t_{o,N}]$, $\boldsymbol{r}_o = [r_{o,1}, r_{o,2}, \cdots, r_{o,N+1}]$, and the set $\boldsymbol{I}_o = \{I_{o,1}, I_{o,2}, \cdots, I_{o,N+1}\}$ are the thresholds, output representation levels, and interval set of a $log_2(N+1)$-bit BOA, where $I_{o,1} = (-\infty, t_{o,1}]$, $I_{o,k} = [t_{o,k-1}, t_{o,k}]$ for $k = 2, \cdots, N$, $I_{o,N+1} = [t_{o,N}, +\infty)$, and the BOA output $x[n] = r_{o,k}$ if $x_c(nT) \in I_{o,k}$ for $k = 1, \cdots, N+1$.

Consider a 4-tap channel with impulse response $\boldsymbol{h} = [0.08, 0.07, 0.1, 0.04]$. The conditional probability density functions (pdfs) $P(x_c[n]|b[n] = -1)$ and $P(x_c[n]|b[n] = +1)$ corresponding to the marginal pdf of the channel output conditioned on the bit $b[n]$ being either -1 or $+1$ at time n, are illustrated in Fig. 3(b) and Fig. 3(c), respectively. In a CUA, the thresholds are set uniformly within the ADC's FSR. Assuming that the FSR is $[-0.3, +0.3]$, a 4-bit CUA will have its thresholds at $\boldsymbol{t}_u$= $[\pm 0.26005, \pm 0.2290, \pm 0.18575, \pm 0.14875, \pm 0.1145, \pm 0.0743, \pm 0.03715, 0]$ (Fig. 3(d)). In contrast, the thresholds in a BOA are positioned at the crossover points of the two conditional pdfs. For this example, the BOA's thresholds are found to be $\boldsymbol{t}_o = [\pm 0.11, \pm 0.08, \pm 0.03, 0]$ (see Fig. 3(d)) as there are 7 crossover points. Thus, the BOA illustrated here is a 3-bit ADC. Figure 3(e) shows that the BOA achieves a 1 bit reduction in the ADC resolution while achieving $BERR(40, 4, 3) \approx 10^8$ and $SG(10^{-3}, 4, 3) \approx 8\,\text{dB}$.

In order to compute $\boldsymbol{t}_o$, we need the following definition of noise-free channel outputs:

Definition 2. The $\boldsymbol{\mu}$-set of a channel $\boldsymbol{h} = [h_0, h_1, \cdots, h_{L-1}]$ is an ordered set defined as $\boldsymbol{\mu} = \{\boldsymbol{\mu}^+ \cup \boldsymbol{\mu}^-\}$, where both $\boldsymbol{\mu}^+ = \{\mu_l^+\}_{l=1}^{2^{L-1}}$ and $\boldsymbol{\mu}^- = \{\mu_l^-\}_{l=1}^{2^{L-1}}$ are ordered sets of noise-free channel outputs conditioned on the transmitted symbol $b[n]$ taking the value $+1$ and -1, respectively. The $\boldsymbol{\mu}$, $\boldsymbol{\mu}^+$ and $\boldsymbol{\mu}^-$ sets have elements in ascending order.

In general, the N thresholds of a BOA for an ADC-ML receiver can be obtained [12] as the N solutions for the unknowns $\{t_{o,i}\}$ $(i = 1, \cdots, N)$ to the following equation:

$$2^{-L+1} \sum_{l=1}^{2^{L-1}} \mathcal{N}(t_{o,i}; \mu_l^+, \sigma_n) = 2^{-L+1} \sum_{l=1}^{2^{L-1}} \mathcal{N}(t_{o,i}; \mu_l^-, \sigma_n), \ (i = 1, \cdots, N) \quad (2)$$

where $\mathcal{N}(x; \mu, \sigma_n) = \frac{1}{\sqrt{2\pi\sigma_n^2}} e^{\frac{-(x-\mu)^2}{2\sigma_n^2}}$, $N \leq 2^L - 1$, μ_l^+ and μ_l^- $(1 \leq l \leq 2^{L-1})$ are the 2^{L-1} noise-free channel outputs (see **Definition** 2). In the example shown in Fig. 3, $\boldsymbol{h} = [0.08, 0.07, 0.1, 0.04]$, $L = 4$, $\{\mu_l^+\}_{l=1}^8 = \{-0.09, -0.01, 0.05, 0.07, 0.13, 0.15, 0.21, 0.29\}$ and $\{\mu_l^-\}_{l=1}^8 = \{-0.29, -0.21, -0.15, -0.13, -0.07, -0.05, 0.01, 0.09\}$.

C. BOA with a Linear Equalizer (LE)

Consider a BOA followed by a K-tap linear equalizer (LE) with taps $\mathbf{w} = [w_0, w_1, \ldots, w_{K-1}]$, such that the equalizer

output $y_{eq}[n] = \sum_{k=0}^{K-1} w_k x[n-k]$. In a BOA, the representation levels $\boldsymbol{r}_o = \{r_{o,1}, r_{o,2}, ..., r_{o,N+1}\}$ and the thresholds $\boldsymbol{t}_o$ are chosen to minimize the link BER. Obtaining a closed form expression for the BOA's representation levels in the presence of channel ISI and a LE is in general intractable. Therefore, the gradient descent algorithm [12] is employed to compute the representation levels iteratively as follows:

$$\begin{aligned} BER &= f(h, \boldsymbol{r_o}, \boldsymbol{t_o}, \mathbf{w}, \sigma_n) \\ \Delta BER &= f(h, \boldsymbol{r_o} + \triangle \boldsymbol{r_o}, \boldsymbol{t}_o + \triangle \boldsymbol{t_o}, \mathbf{w}, \sigma_n) \\ &\quad - f(h, \boldsymbol{r_o}, \boldsymbol{t}_o, \mathbf{w}, \sigma_n), \quad (3) \\ \boldsymbol{r}_o[j] &= \boldsymbol{r}_o[j-1] + \mu \left(\frac{\partial BER}{\partial \boldsymbol{r}_o} \right)_{|_{\boldsymbol{r}_o = \boldsymbol{r}_o[j-1]}} \\ &\approx \boldsymbol{r}_o[j-1] + \mu \left(\frac{\Delta BER}{\Delta \boldsymbol{r}_o} \right)_{|_{\boldsymbol{r}_o = \boldsymbol{r}_o[j-1]}}, \quad (4) \end{aligned}$$

where it is assumed that $BER = f(h, \boldsymbol{r_o}, \boldsymbol{t_o}, \mathbf{w}, \sigma_n)$ is known, and $\boldsymbol{r}_o[j] = \{r_{o,1}[j], r_{o,2}[j], \cdots, r_{o,N+1}[j]\}$ are the ADC representation levels in the j^{th} iteration of the gradient search. The thresholds in the j^{th} iteration are obtained as follows:

$$t_{o,i}[j] = \frac{r_{o,i}[j] + r_{o,i+1}[j]}{2}, i = 1, \cdots, N. \quad (5)$$

The BOA's representation levels adaptation algorithm is as follows. First, the ADC parameters $\boldsymbol{r}_o$ and $\boldsymbol{t}_o$ are initialized. Then, the gradient vector is estimated by computing finite differences based on (4). The next step is to update $\boldsymbol{t}_o$ using (5). The last two steps are repeated until the BER converges, i.e., when the difference in the BER between adjacent iterations is less than a prespecified value.

III. ACHIEVABLE BER IMPROVEMENT VIA BOA

In this section, we study through analysis and simulations how to maximize the benefits of the BOA over the CUA. Note: a BOA receiver always achieves the same if not better BER as compared to a CUA receiver, given the same number of bits, channel and noise power, because a CUA is a special case of the BOA. An important question to ask is under what conditions are the benefits offered by a BOA over a CUA substantial. Specifically, we wish to determine channel conditions under which $BERR(SNR, B_u, B_o)$ is say at least $10\times$. $BERR(SNR, B_u, B_o)$ is empirically observed to depend strongly on the difference between the CUA's and the BOA's thresholds, the number of adjacent noise-free channel outputs with opposing signs, channel SNR and the ADC resolution. We therefore discuss the relationship between these factors on $BERR(SNR, B_u, B_o)$. We restrict our analysis to channels with memory $L < 7$ in order to enable the derivation of useful insights analytically. Note that the performance of BOA for channels with large memory $L > 7$ has been studied in [13].

In this section, for tractability of analysis, we assume that the ADC (BOA or CUA) is followed by a memoryless symbol-by-symbol ML decoder and that BPSK signaling is used over a known channel with impulse response $\boldsymbol{h}$. Thus, dropping the time index 'n', and employing the notation X_c and X_u to represent the random variables (RVs) corresponding to $x_c(nT)$ and $x[n]$, respectively, for a CUA, we have:

$$P(X_u = r_{u,k}|b) = P(X_c \in I_{u,k}|b),\ (k = 1, \cdots, M+1)$$

where $X_u \in \{r_{u,1}, r_{u,2}, \cdots, r_{u,M+1}\}$, $r_{u,k}$ is the k^{th} CUA representation level (see **Definition** 1). Then, the memoryless ML decision rule for a CUA is given by:

$$\hat{b} = \begin{cases} +1, & \text{if } \frac{P(X_u|b=+1)}{P(X_u|b=-1)} > 1 \\ -1, & \text{otherwise} \end{cases}.$$

Similarly, let X_o be the RV corresponding to $x[n]$ for a BOA. Then,

$$P(X_o = r_{o,k}|b) = P(X_c \in I_{o,k}|b),\ (k = 1, \cdots, N+1)$$

where $X_o \in \{r_{o,1}, r_{o,2}, \cdots, r_{o,N+1}\}$ and $r_{o,k}$ is the k^{th} BOA representation level (see **Definition** 1). Then, the memoryless ML decision rule for a BOA is given by:

$$\hat{b} = \begin{cases} +1, & \text{if } \frac{P(X_o|b=+1)}{P(X_o|b=-1)} > 1 \\ -1, & \text{otherwise} \end{cases}.$$

A. BERR Expression

We wish to analytically predict $BERR(SNR, B_u, B_o)$ given its arguments and the channel $\boldsymbol{h}$. Such analysis will eliminate the need for expensive Monte-Carlo (MC) simulations. Furthermore, conditions under which a BOA can offer a $BERR(SNR, B_u, B_o)$ of 10^r can be derived.

First, the following definitions are provided.

Definition 3. A channel $\boldsymbol{h}$ is said to be m-clustered if there are m transitions (μ-transitions) in its $\boldsymbol{\mu}$-set, where a μ-transition occurs when an element of the $\boldsymbol{\mu}^+$ set is followed by an element of the $\boldsymbol{\mu}^-$ set or vice versa. Note: $m > 0$ and takes odd values only, and $m > N$ at low SNR scenario while $m = N$ at high SNR scenario.

Definition 4. The threshold non-uniformity metric h_t of a $log_2(N+1)$-bit BOA is a measure of the difference between $\boldsymbol{t}_o$ and $\boldsymbol{t}_u$, and is defined as:

$$\begin{aligned} h_t = \frac{-1}{log_2(\frac{N+1}{2})} \sum_{i=2}^{(N+1)/2} & \left[\left(\frac{t_{o,i} - t_{o,i-1}}{y_{max}} \right) log_2 \left(\frac{t_{o,i} - t_{o,i-1}}{y_{max}} \right) \right. \\ & \left. + \left(\frac{t_{o,1} + y_{max}}{y_{max}} \right) log_2 \left(\frac{t_{o,1} + y_{max}}{y_{max}} \right) \right] \quad (6) \end{aligned}$$

where $[-y_{max}, y_{max}]$ is the ADC FSR, and only the non-positive BOA thresholds are used since the BOA's thresholds are symmetric about the origin. Note: $0 \leq h_t \leq 1$, and the larger the value of h_t the closer are the BOA's thresholds to those of the CUA.

Figure 4(a) shows an example when $m = 3$ for a 4-tap channel (thus there are $2^4 = 16$ elements in $\boldsymbol{\mu}$), and Fig. 4(b) illustrates two examples when $h_t = 0.7564$ and $h_t = 1$, respectively. Algorithm 1 can be employed to obtain m and h_t for a specific channel.

Definition 5. Let $d^*_{o,k} = \min_{\mu \in \boldsymbol{\mu}}(|t_{o,k} - \mu|)$ be the minimum distance of the k^{th} BOA threshold $t_{o,k}$ $(k = 1, \cdots, N)$ to the nearest noise-free channel output μ. Then, the *minimum BOA distance* $d_{o,min} = \min_{1 \leq k \leq N}(d^*_{o,k})$.

Definition 6. Each of the $(M+1)$ intervals $I_{u,k}$ with $k = 1, \cdots, M+1$, in a CUA has a *dominant noise-free channel output* μ^*_k given by,

(a) (b)

Figure 4. Examples of m-clustering and h_t: (a) m-clustering with $m = 3$, and (b) h_t for $\boldsymbol{t}_o = [\pm 0.3, \pm 0.2, \pm 0.1, 0]$ (case I where $h_t = 1$) and $\boldsymbol{t}_o = [\pm 0.3, \pm 0.11, \pm 0.09, 0]$ (case II where $h_t = 0.7564$) with $y_{max} = 0.3$.

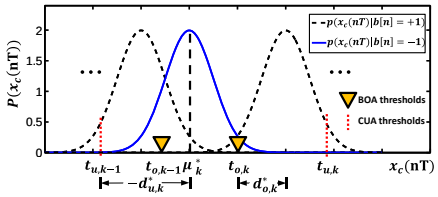


Figure 5. An illustrative example for $d_{o,k}^*$, μ_k^* and $d_{u,k}^*$.

$$\mu_k^* = \begin{cases} \underset{\mu_l^- \in \boldsymbol{\mu}^-}{arg\ max} \left[\int_{I_{u,k}} \mathcal{N}(x; \mu_l^-, \sigma_n) dx \right], & \text{if } \frac{P(X_u = r_{u,k} | b=+1)}{P(X_u = r_{u,k} | b=-1)} > 1 \\ \underset{\mu_l^+ \in \boldsymbol{\mu}^+}{arg\ max} \left[\int_{I_{u,k}} \mathcal{N}(x; \mu_l^+, \sigma_n) dx \right], & \text{otherwise} \end{cases}.$$

Definition 7. Let $d_{u,k}^* = -min(\mu_k^* - t_{u,k-1}, t_{u,k} - \mu_k^*)$ be the minimum distance of the k^{th} CUA's dominant noise-free channel output μ_k^* from the boundaries of the k^{th} interval $I_{u,k}$. Then, the *minimum CUA distance* $d_{u,min} = \underset{1 \le k \le (M+1)}{min} (d_{u,k}^*)$.

Figure 5 shows an example of the marginal pdf of the channel output, illustrating the corresponding $d_{o,k}^*$, μ_k^* and $d_{u,k}^*$.

In the appendix, we show that $BERR(SNR, B_u, B_o)$ is given by:

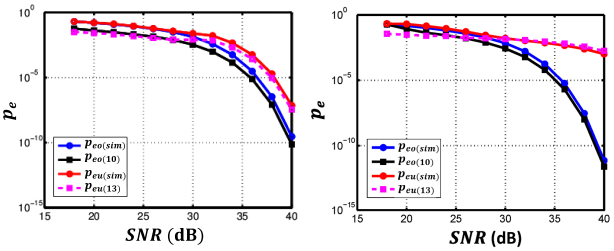
$$BERR(SNR, B_u, B_o) \approx \begin{cases} \frac{d_{o,min}}{2d_{u,min}} e^{\frac{d_{o,min}^2 - d_{u,min}^2}{2\sigma_n^2}}, & \text{if } d_{u,min} > 0 \\ \sqrt{\frac{\pi}{2}} \frac{d_{o,min}}{\sigma_n} e^{\frac{d_{o,min}^2}{2\sigma_n^2}}, & \text{if } d_{u,min} < 0 \\ \sqrt{\frac{\pi}{8}} \frac{d_{o,min}}{\sigma_n} e^{\frac{d_{o,min}^2}{2\sigma_n^2}}, & \text{if } d_{u,min} = 0 \end{cases}. \quad (7)$$

Equation (7) indicates that $BERR(SNR, B_u, B_o)$ increases with $d_{o,min}^2$ or $(d_{o,min}^2 - d_{u,min}^2)$. Furthermore, $BERR(SNR, B_u, B_o)$ can be predicted given the channel $\boldsymbol{h}$ (thus $\boldsymbol{\mu}^-$, $\boldsymbol{\mu}^+$, $d_{o,min}^2$ and $d_{u,min}^2$) and SNR.

MC simulations of link BER were run with 10^8 (for $SNR \le 36\,\text{dB}$) or 10^{12} (for $SNR > 36\,\text{dB}$) samples and for SNR ranging from $18\,\text{dB}$ to $40\,\text{dB}$ for channels $\boldsymbol{h} = [0.09, 0.1, 0.08, -0.05]$ and $\boldsymbol{h} = [0.08, 0.07, 0.1, 0.04]$, respectively. Figure 6 indicates that the analytical expressions (10) and (13) can predict the results of the MC simulations to within an order-of-magnitude, and thus can be employed to estimate the p_{eo} and p_{eu}. Furthermore, as expected, the expressions (10) and (13) become more accurate at high SNRs. Finally, it can be seen in Fig. 6 that 3-bit BOA achieves a shaping gain of $2\,\text{dB}$ ($8\,\text{dB}$) over a 6-bit (4-bit) CUA at a BER of 10^{-5} (10^{-3}). Figure 7 shows that BERR can also be predicted via (7) to within an order-of-magnitude of MC simulations, and that it increases with SNR.

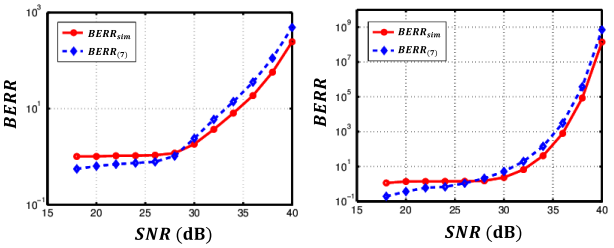
Algorithm 1 Algorithm to obtain m-clustered value and h_t for an ADC-ML receiver.

1. Initialize the channel $\boldsymbol{h}$ and the SNR, calculate noise variance σ_v^2 based on $\boldsymbol{h}$ and the SNR.
2. Define the main cursor of $\boldsymbol{h}$, calculate $\boldsymbol{\mu}^+ = \{\mu_i^+\}_{l=1}^{2^{L-1}}$ and $\boldsymbol{\mu}^- = \{\mu_i^-\}_{l=1}^{2^{L-1}}$, respectively, and obtain the ordered set $\boldsymbol{\mu} = \{\boldsymbol{\mu}^+ \bigcup \boldsymbol{\mu}^-\}$.
3. Count the number of transitions in $\boldsymbol{\mu}$, which is the m-clustered value.
4. Obtain $\boldsymbol{t_0}$ using equation (2).
5. Calculate h_t using equation (6).



(a) (b)

Figure 6. Comparison among p_{eo} from MC simulation ($p_{eo(sim)}$), p_{eo} estimated using (10) ($p_{eo(10)}$), p_{eu} from MC simulation ($p_{eu(sim)}$), and p_{eu} estimated using (13) ($p_{eu(13)}$), for channels (a) $\boldsymbol{h} = [0.09, 0.1, 0.08, -0.05]$ when $B_u = 6$ and $B_o = 3$, and (b) $\boldsymbol{h} = [0.08, 0.07, 0.1, 0.04]$ when $B_u = 4$ and $B_o = 3$, respectively.



(a) (b)

Figure 7. Comparison between $BERR(SNR, B_u, B_o)$ from MC simulation ($BERR_{sim}$), and $BERR(SNR, B_u, B_o)$ estimated using (7) ($BERR_{(7)}$) for channels (a) $\boldsymbol{h} = [0.09, 0.1, 0.08, -0.05]$ when $B_u = 6$ and $B_o = 3$, and (b) $\boldsymbol{h} = [0.08, 0.07, 0.1, 0.04]$ when $B_u = 4$ and $B_o = 3$, respectively.

B. BER Improvement vs. Channel ISI

This subsection presents an empirical study of BERR as a function of channel ISI. In the rest of this subsection, we consider the special case of $log_2(m+1)$-bit BOA and CUA, i.e., $B_u = B_o = log_2(m+1)$. Specifically, we study the relationship between $BERR(SNR, B_u, B_o)$ and m-cluster and h_t, for a set of 4-tap channels $\boldsymbol{h} = [1, a_1, a_2, a_3]$ ($a_i = 0.1 : 0.1 : 0.9, i = 1, 2, 3$) using an ADC-ML receiver. The corresponding results are shown in Fig. 8, where $BERR(SNR, B_u, B_o)$ is calculated using BER expressions (10) and (13) when $SNR = 38\,\text{dB}$. Note: the results when $p_{e,u} > 10^{-1}$, which occurs because $m = 1$ or the channel ISI is too large for the given SNR, are removed in Fig. 8 for better illustration. The $BERR(SNR, B_u, B_o)$ and h_t for the channel (under which the measured results are shown in Fig. 18) is also shown in Fig. 8, which has $log_2(m+1) = 2.6 \approx 3$ and $h_t \approx 0.46$. Figure 8 indicates that smaller h_t and larger m combinations are likely to result in larger $BERR(SNR, B_u, B_o)$. Furthermore, Fig. 8 shows that $BERR(SNR, B_u, B_o) > 10^6$, when $m \ge 5$ and $h_t \le 0.8$.

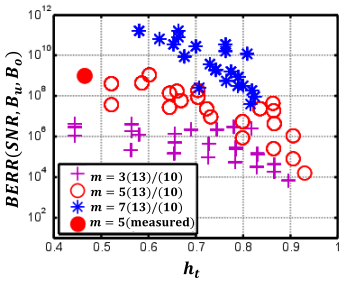


Figure 8. $BERR(SNR, B_u, B_o)$ vs. h_t, where $B_u = B_o = \log_2(m+1)$, for channels $\boldsymbol{h} = [1, a_1, a_2, a_3]$ $(a_i = 0.1 : 0.1 : 0.9,\ i = 1, 2, 3)$ using an ADC-ML receiver when $SNR = 38\,\text{dB}$. The value of h_t and measured $BERR(SNR, 4, 3)$ for a FR4 channel using an ADC-LE receiver (described in section V) are also shown.

C. BER Improvement vs. Number of Bits B_x in the ADC

In this subsection, we claim that for any given realization of the type considered in this section, there exists an optimal ADC resolution in the sense that it achieves the maximum of the function $BERR(SNR, B_x, B_x)$. To see this, note that $p_{e,u}$ decreases with B_x, which is a consequence of $p_{eu}(SNR, B_x + 1)$ being defined through a maximization over the set of decision regions that includes those used to achieve $p_{eu}(SNR, B_x)$ as a subset. Except on a set of measure zero (for which $p_{eu}(SNR, B_x) = p_{eo}(SNR, B_x)$), $p_{eu}(SNR, B_x + 1) < p_{eu}(SNR, B_x)$, for all B_x. On the other hand, we note that p_{eo} decreases with B_x for $B_x < log_2(N + 1)$, following the same reasoning. However, once $B_x = log_2(N + 1)$, further increases in B_x provide no additional improvement in p_{eo} (for the memoryless symbol-by-symbol detector used in this analysis). As a result, the ratio $BERR(SNR, B_x, B_x)$ will monotonically decrease for $B_x > log_2(N+1)$. Hence, it must achieve a maximal value for one (or more) $B_x \leq log_2(N+1)$. The $BERR(SNR, B_x, B_x)$ versus B_x plot in Fig. 9(a) shows that $BERR(36\,\text{dB}, B_x, B_x)$ is maximized when $B_x = 3$.

The intuition gained from the analysis of the ADC-ML receiver holds for the ADC-LE receivers. This is confirmed by the simulated $BERR(SNR, B_x, B_x)$ versus B_x plot shown in Fig. 9(b), which is obtained for a FR4 channel at $10\,\text{Gb/s}$ in Fig. 2, when $SNR = 36\,\text{dB}$. Fig. 9(b) shows, under the given condition, $B_x = 3$ maximizes the $BERR(SNR, B_x, B_x)$.

IV. IMPLEMENTATION OF BOA RECEIVER

In this section, a prototype IC implementation of BOA receiver is described. Figure 10 shows the block diagram of the receiver, which consists of a BOA chip and an Altera FPGA board. The FPGA board implements the back-end DSP

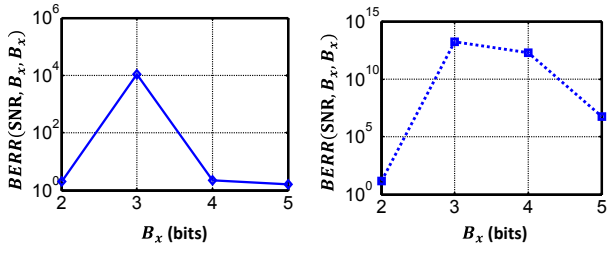


Figure 9. $BERR(SNR, B_x, B_x)$ vs. B_x of (a) an ADC-ML receiver, when the channel impulse response is $\boldsymbol{h} = [0.09, 0.1, 0.08, 0.04]$ and $SNR = 36\,\text{dB}$, and (b) an ADC-LE receiver, when the channel impulse response is equal to the FR-4 channel (see Fig. 2) and $SNR = 36\,\text{dB}$.

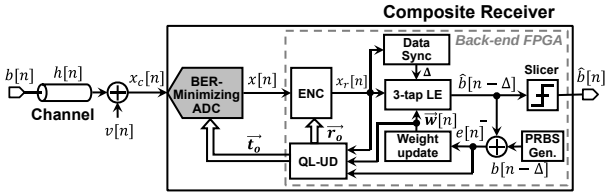


Figure 10. Block diagram of the BOA receiver.

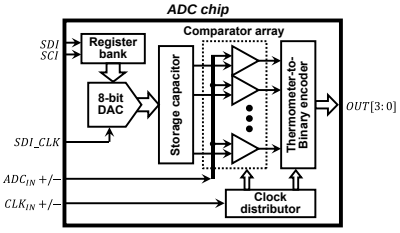


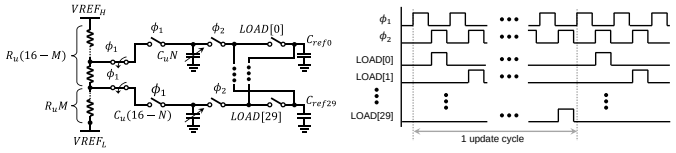
Figure 11. Block diagram of the BOA chip.

blocks. The ADC chip includes a reconfigurable 4-bit $4\,\text{GS/s}$ flash ADC and an 8-bit digital-to-analog converter (DAC). The 8-bit DAC enables variable-threshold and variable-resolution ADC configurations, so that the performance of a CUA receiver can be compared with that of the BOA receiver. The back-end DSP block includes a LE and QL-UD. In the BOA receiver, the ADC quantizes the channel outputs and provides these into the back-end DSP block, which implements an adaptive LE. Once the equalizer coefficients converge, the quantization levels $\boldsymbol{r_o}$ that minimize link BER are obtained using gradient descent search algorithm. The updated quantization thresholds $\boldsymbol{t_o}$ are then fed back into the ADC chip.

A. ADC Full-chip Block Diagram

The ADC chip consists of an 8-bit DAC, storage capacitor array, and a 4-bit flash ADC, as illustrated in Fig. 11. In a conventional flash ADC, the threshold voltages are generated by a resistor ladder. A BOA, however, requires variable thresholds; thus, a DAC is employed for threshold generation. System analysis shows that an 8-bit DAC is required to ensure that the 3-bit BOA receiver can achieve similar or better BER performance compared to a 4-bit CUA receiver. In principle, 30 DACs are needed for 4-bit ADC threshold generation. To minimize power and area overhead, a single-core, multiple-output passive DAC, which is an extension of the single-core single-output passive DAC presented in [20], is proposed to generate the variable threshold voltages. The threshold voltage generator has a power overhead of 10% ($\sim 50\,\mu\text{W}$) compared to a fixed resistor string for a CUA.

Figure 12 illustrates the operation of the 8-bit DAC. A single voltage threshold update occurs over two phases of non-overlapping clocks ϕ_1 and ϕ_2. In phase I ($\phi_1 = 1$,$\phi_2 = 0$), the 4 MSBs of the 8-bit DAC input selects a 4-bit section of the resistor ladder to charge the 4-bit unit capacitor (C_u) array. In phase II ($\phi_1 = 0$, $\phi_2 = 1$), C_u and C_{ref} are connected together. The resulting charge sharing shifts the threshold voltage toward the desired value. The nominal, post-layout extracted operating frequency of the DAC core is $12\,\text{MHz}$, resulting in an update frequency per C_{ref} of $375\,\text{kHz}$. This is more than sufficient to compensate for leakage. The 8-bit DAC updates the thresholds of the comparator array sequentially.



(a) (b)

Figure 12. The 8-bit single-core multiple-output DAC: (a) circuit schematic, and (b) timing diagram.

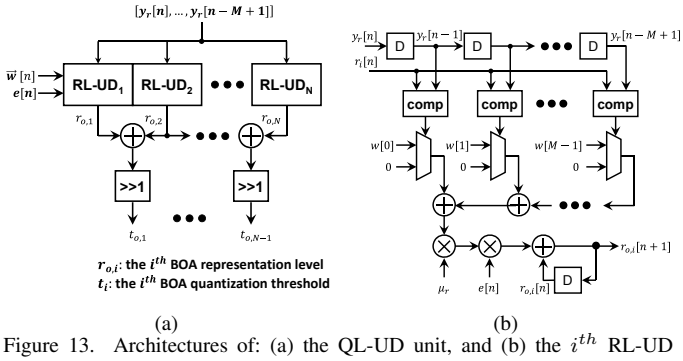
Therefore, only the threshold of one comparator is updated at each moment. The storage capacitors hold the thresholds for the other comparators. In a flash ADC, one input of each comparator is connected to the analog input, while the other input is connected to the corresponding threshold. The comparator array compares the analog input with the threshold voltages simultaneously and produces comparison results in the form of a thermometer code. Thus, a binary encoder following the comparator array is needed for the ease of back-end digital processing.

B. Back-end DSP in the FPGA

The back-end DSP units are implemented in an Altera Transceiver Signal Integrity Development FPGA board [21], in which the DSP units operate at a frequency of $100\,\mathrm{MHz}$. Thus, 40 parallel channels are used to handle the $4\,\mathrm{Gb/s}$ outputs from the ADC chip. As shown in Fig. 10, the back-end DSP block consists of an encoder (ENC), data synchronization unit (Data Sync), LE, and QL-UD. The binary encoder converts the ADC output $x[n]$ into two's complement number representation $x_r[n]$, while the data synchronization unit provides the start position of the pseudorandom binary sequence (PRBS). A 3-tap LMS adaptive equalizer is designed to compensate for channel ISI, while the QL-UD unit adjusts the ADC quantization thresholds $\boldsymbol{t_o}$ and representation levels $\boldsymbol{r_o}$ to achieve the minimum BER. As other blocks are standard DSP functional blocks, we focus on the implementation of the QL-UD unit. The equalizer computes an estimate of the transmitted symbol $b[n-\Delta]$ based on the encoder output $[x_r[n],\ldots,x_r[n-M+1]]^T$ as:

$$\hat{b}[n-\triangle]=\sum_{k=0}^{M-1} w[k]x_r[n-k].$$

The estimation error $e[n]=b[n-\Delta]-\hat{b}[n-\triangle]$ is used to adjust the equalizer coefficients $\mathbf{w}$. Once $\mathbf{w}$ converges, $e[n]$ can be used to update the ADC representation levels. Fixing the quantization thresholds $\boldsymbol{t_o}$, the optimal representation levels $\boldsymbol{r_o}$ that minimize the MSE between $b[n]$ and $\hat{b}[n]$ can be obtained from gradient descendent search. The LMS update



(a) (b)

Figure 13. Architectures of: (a) the QL-UD unit, and (b) the i^{th} RL-UD unit.

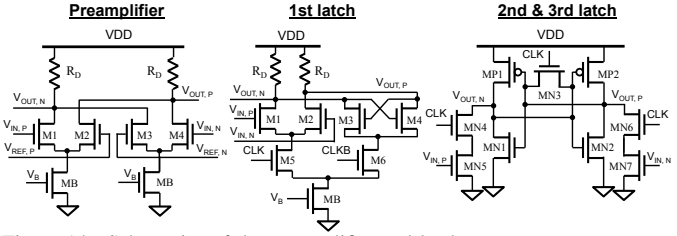


Figure 14. Schematics of the preamplifier and latches.

of the quantization levels is obtained by approximating the gradient of the MSE by its instantaneous value,

$$r_{o,i}[n+1]=r_{o,i}[n]+\mu_r e[n]\textstyle\sum_{k:x_r[n-k]=r_{o,i}}\mathbf{w}[k].$$

The LMS update can be further modified to the AMBER algorithm [10]:

$$r_{o,i}[n+1]=r_{o,i}[n]+\mu_r I[n]sgn(e[n])\textstyle\sum_{k:x_r[n-k]=r_{o,i}}\mathbf{w}[k],$$

where $I[n]$ is the bit error indicator function. Figure 13 is the block diagram of the quantization level update unit and the individual RL-UD block, which update each quantization level based on the current ADC output, equalizer estimation error, and equalizer coefficients. The architecture of the update unit for each representation level $r_{o,i}$ is shown in Fig. 13(b). A total of 2^{B_o} such units are needed to update the representation levels $\boldsymbol{r_o}$. The total number of gates and power consumption of the QL-UD unit are estimated to be about $90\mathrm{K}$ (NAND gates equivalent) and $12.3\,\mathrm{mW}$, respectively. This power accounts for about 44% of the total power of the back-end DSP, and is expected to reduce with technology scaling. Note: the QL-UD unit can be turned off once BOA representation levels are obtained.

C. Comparator Design

The comparator consists of a preamplifier and 3 cascaded latches, and Fig. 14 illustrates the schematics of the preamplifier and latches. The preamplifier subtracts the analog input from the threshold and provides polarity of the comparison result. The cascaded latches amplify the preamplifier output to reduce the occurrence of meta-stability. The preamplifier design is shown in Fig. 14, which is widely employed for high-speed ADCs [7], [8]. The first latch is a current mode latch [7], which is composed of an input differential pair (M_1, M_2) and a cross-coupled regenerative latch pair (M_3, M_4) sharing the same resistive load, R_D. When CLK is high, the circuit is in tracking mode with low gain and large bandwidth. When the CLK is low, the circuit shifts to the regenerative mode, and the sampled signal from the tracking mode is amplified and delivered to the next stage. The second and third latches do not consume static power once they fully regenerate, and are referred to as dynamic latches [22], [23]. In this design, only the first latch uses a current mode latch because it is the most critical to guarantee accurate comparison results. For example, if the first latch does not have a large enough bandwidth to follow the updated polarity of the preamplifier output, the comparator may generate an incorrect output, regardless of how well the following latches perform. It should be noted that the cascaded latches operate in a pipelined manner for speed consideration. In particular, when the preceding latch is working in a tracking mode, the subsequent latch is working in regeneration mode, and vice versa.

D. Encoder Design

A Gray encoder is used because it is more compact and faster than a summing encoder [8]. Since less pipelining is required for multi-gigahertz operation, the Gray encoder consumes less power than a summing encoder. There are three steps to encoding. First, the thermometer code is converted to a 1-of-N code. And then, the 1-of-N code is converted to a Gray code to suppress bubble errors. The Gray code is finally converted to binary code by XOR gates, for the purpose of further DSP processing in the subsequent blocks. In this chip, pipelined D flip-flops (DFFs) are used between adjacent logic gates in the encoder to guarantee $4\,\mathrm{Gb/s}$ operation.

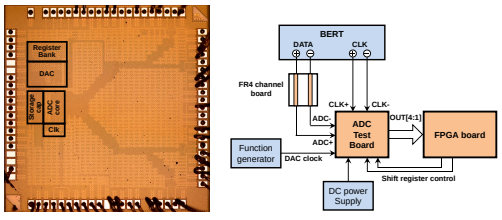
V. MEASUREMENT RESULTS

This section summarizes the measurement results of both the stand-alone ADC chip and the ADC-based receiver. A 4-bit $4\,\mathrm{GS/s}$ ADC chip is fabricated in a $90\,\mathrm{nm}$ low power (LP) CMOS technology with an active area of $0.33\,\mathrm{mm}^2$ and tested in a chip-on-board assembly. The chip's micrograph is shown in Fig. 15(a).

First, we ensure the standalone ADC performance is sufficient to support link operation. Since the ADC chip includes an 8-bit DAC for variable-threshold and variable-resolution ADC configuration, we utilize it to configure the ADC's threshold voltages for calibration. The measured DNL and INL characteristics before and after calibration are shown in Fig. 16(a) and (b), respectively. The DNL and INL are reduced from ± 1.3 LSB and 4 LSB to ± 0.04 LSB and 0.14 LSB, respectively, after calibration, indicating the effectiveness of the calibration process. Figure 16(c) illustrates that the ADC can achieve up to 3.4 bits of ENOB at near-Nyquist rate input frequency of $1.9375\,\mathrm{GHz}$. The figure of merit (FOM) of the ADC is $1.42\,\mathrm{pJ/conv.step}$ at $4\,\mathrm{GS/s}$ excluding clock buffers, which is comparable to the state-of-art using a similar technology [8], [9].

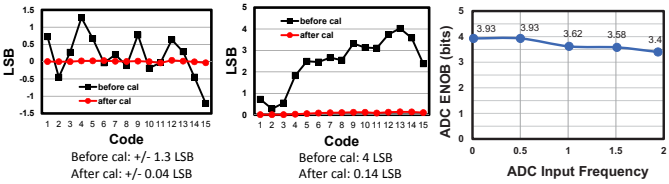
Figure 15(b) shows the block diagram of the link test set-up, which mainly consists of a BER tester (BERT), channel board, ADC PCB board, and FPGA board. The BERT provides $4\,\mathrm{Gb/s}$ synchronous data and clock, with the data passing through a 20-inch FR4 channel before entering the ADC board. The ADC chip quantizes the incoming analog signal and its outputs are fed into the FPGA board. The back-end DSP units in the FPGA then perform equalization and optimal ADC representation levels search. Finally, the updated representation levels are fed back to the ADC chip. However, in our experiment, the BOA's representation levels are obtained off-line due to a synchronization problem in the interface between the BOA chip and the FPGA board.

Link tests were conducted at $4\,\mathrm{Gb/s}$ over a 20-inch channel with $2^{23}-1$ PRBS data. The BOA's representation levels were



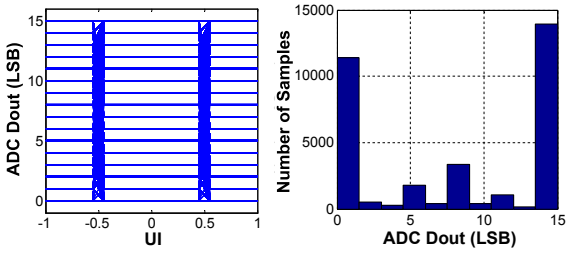
(a) (b)

Figure 15. (a) Micrograph of the BOA chip, and (b) the test set-up.



(a) (b) (c)

Figure 16. Standalone ADC measurement results: (a) DNL and (b) INL characteristics before/after calibration, and (c) measured ENOB vs. input frequency.

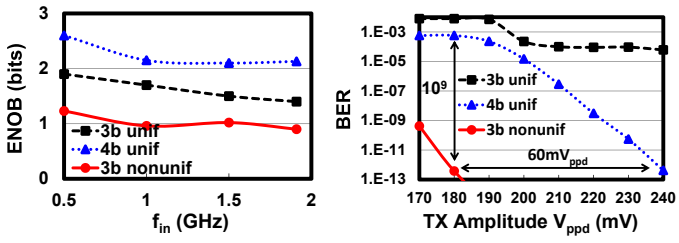


(a) (b)

Figure 17. Measured ADC output: (a) eye diagram, and (b) histogram for a 20-inch FR4 channel at $4\,\mathrm{Gb/s}$ when TX amplitude is $180\,\mathrm{mV_{ppd}}$ and ADC FSR is $100\,\mathrm{mV_{ppd}}$.

obtained by first extracting the converged equalizer coefficients with the ADC IC in a 4-bit uniform mode, followed by an off-line adaptive channel estimation and gradient search procedure [12]. The ADC representation levels were then manually set in the lab. Figure 17 shows the post-ADC eye diagram and histogram of the ADC code at a 20-inch FR4 channel, with TX amplitude of $180\,\mathrm{mV_{ppd}}$ and a CUA FSR of $100\,\mathrm{mV_{ppd}}$, which indicate that the received eye is closed. In particular, the channel loss at Nyquist rate is about $-22\,\mathrm{dB}$.

Figure 18(a) compares the measured ENOB when the FSR of the CUA is $100\,\mathrm{mV_{ppd}}$. The FSR of the 4-bit CUA was adjusted to achieve the best BER under the given TX amplitude and channel loss. The 3-bit BOA has the lowest ENOB. The ENOB difference between the 4-bit CUA and the 3-bit BOA is in the range of 1.37-bit to 1.08-bit, while the difference between the 3-bit CUA and the 3-bit BOA is in the



(a) (b)

Figure 18. ENOB and BER measurements: (a) ENOB vs. input frequency, and (b) BER vs. TX amplitude at $4\,\mathrm{Gb/s}$ when the FSR of the CUA is $100\,\mathrm{mV_{ppd}}$.

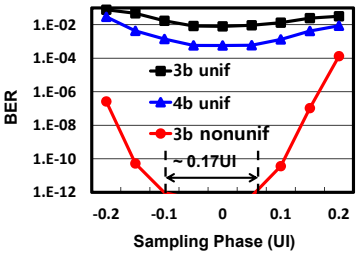


Figure 19. Measured BER vs. sampling phase using a 20-inch channel when TX amplitude is $180\,\mathrm{mV_{ppd}}$ and the FSR of the CUA is $100\,\mathrm{mV_{ppd}}$.

Table I
PERFORMANCE SUMMARY OF THE ADC-BASED RECEIVERS

ADC operating mode		3-bit BOA	4-bit uniform
Technology		90 nm LP CMOS (1P8M)	
Core die area		$0.38\,\mathrm{mm}^2$	
Supply voltage		1.2 V for analog, 1.28 V for digital & clock	
Data rate		$4\,\mathrm{Gb/s}$	
Power consumption	ADC [mW]	30.7	59.7
	B/E digital [mW]	$^{*}(30/^{**}17.7)$	$^{*}16.4$

*Digital back-end power estimated from synthesis in 90 nm LP CMOS, **The power of the QL-UD unit is excluded.

Table II
PERFORMANCE COMPARISON WITH STATE-OF-ART ADC-BASED RECEIVERS AND ANALOG RECEIVERS IN CMOS

	ADC-based Receivers					Analog Receivers		
	This work	[4]	[2]	[3]	[5]	[25]	[26]	[27]
Process	90 nm LP	65 nm	65 nm	65 nm	65 nm	40 nm	40 nm	90 nm
Sampling rate [GS/s]	4	2.5	2.575	2.5	1.2875	5.1563	7.0125	3.125
Number of bits	3	3	6	5	8	N/A	N/A	N/A
BER@Channel	$< 10^{-12}$	$< 10^{-7}$	$< 10^{-15}$	$< 10^{-12}$	N/A	$< 10^{-12}$	$< 10^{-15}$	$< 10^{-15}$
Channel loss	−22 dB	−17 dB	−26 dB	34″	N/A	~ -28 dB	−26 dB	−15 dB
RX power [mW]	60.7	106	500	192	1600	87	410	8.0
Efficiency [pJ/bit]	$^{*}(15.2/^{**}12.1)$	10.6	48.5	38.4	155.3	$^{***}8.4$	$^{****}29.23$	1.28
FOM2	$^{*}(10.9/^{**}13.7)$	18.8	10.3	0.5568	N/A	74.8	13.6	24.7

*Digital back-end power estimated from synthesis in 90 nm LP CMOS, **The power of the QL-UD unit is excluded.
***with both Tx and Rx, ****with both Tx and Rx and under the worst case PVT conditions.
Note: $\mathrm{FOM2} = \mathrm{DR(Gb/s)} \times 10^{\frac{\mathrm{loss}}{10}} / \mathrm{Power(mW)}$ [24], where DR stands for data rate.

range of 0.74-bit to 0.48-bit. Figure 18(b) illustrates that the BER achieved by the 3-bit BOA receiver is lower by a factor of 10^9 and 10^{10}, as compared to the 4-bit and 3-bit CUA receivers, respectively, at a TX amplitude of $180\,\mathrm{mV_{ppd}}$. This is in spite of the 3-bit BOA having a poorer ENOB than both the 3-bit and 4-bit CUA. Furthermore, the 3-bit BOA requires a $60\,\mathrm{mV_{ppd}}$ lower TX swing compared to a 4-bit CUA to achieve BER $< 10^{-12}$. Thus, Fig. 18 indicates that ENOB is not the best ADC design metric for serial links. The bathtub curve in Fig. 19 shows that the 3-bit BOA can tolerate a peak-to-peak jitter of about 43 ps (∼0.17 UI) at BER=10^{-12} with a TX amplitude of $180\,\mathrm{mV_{ppd}}$, while the 4-bit and 3-bit CUAs are unable to achieve BER < 10^{-4} and 10^{-3}, respectively, under identical conditions.

Table I summarizes the performance of the proposed BOA receiver, and Table II compares this work against state-of-the-art ADC-based receivers [2], [3], [4], [5] and analog receivers [25], [26] in CMOS. The ADC IC consumes $59.7\,\mathrm{mW}$ in 4-bit CUA mode and $30.7\,\mathrm{mW}$ in 3-bit non-uniform mode excluding the clock buffers. The clock buffers in our design accept external clocks and have to drive a long interconnnect before they reach the ADC comparators, as the ADC occupies a small fraction ($< 9\%$) of the die area. Furthermore, the power consumption of the clock buffers for the ADC core alone could not be measured because the power pins of the clock buffers driving the interconnect and the ADC core are shared. The power of the clock buffers driving the ADC core alone, extracted from post-layout simulations, is about $10\,\mathrm{mW}$ when the ADC operates at $4\,\mathrm{GS/s}$, 4-bit CUA mode. The digital back-end power including all the functional blocks in the FPGA was estimated to be $30\,\mathrm{mW}$ and $17.7\,\mathrm{mW}$ via synthesis when including and excluding the QL-UD unit, respectively. The energy efficiency of this receiver excluding the clock buffers is $15.2\,\mathrm{pJ/bit}$ and $12.1\,\mathrm{pJ/bit}$ when including and excluding the QL-UD unit, respectively.

The presented receiver achieves a BER of less than 10^{-12} with the lowest ADC resolution (3-bit non-uniform; Note: a 3-bit CUA was not able to achieve BER $< 10^{-3}$ under the same conditions) at the highest ADC sampling rate ($4\,\mathrm{GS/s}$) while achieving more than $2\times$ higher energy efficiency compared with [2], [3] and [5]. Taking channel loss into account, our solution achieves higher (better) figure-of-merit FOM2 (proposed in [24]) than [2] and [3]. Implemented in a more advanced technology and combining several low power circuit techniques, [4] achieves a better energy efficiency than this work. However, [4] only showed measured BER of 10^{-7} although an extrapolated BER of 10^{-15} was reported. A 2.3-bit (5 comparators) BOA is sufficient if the target BER is relaxed from 10^{-12} to 10^{-7} based on simulations, which translates to about $2/7$ power savings in the ADC. As a result, the efficiency is improved to 13.0 pJ/bit from 15.2 pJ/bit. Furthermore, it should be noted that the power consumption of a flash ADC is mostly determined by its sampling rate and the process technology. Compared to [4], our ADC has higher sampling rate ($4\,\mathrm{GS/s}$ vs. $2.5\,\mathrm{GS/s}$ in [4]) while being implemented in a slower technology (90 nm LP vs. 65 nm in

[4]). Therefore, it is expected that our solution will achieve comparable or better energy efficiency if the sampling rate and process technology were identical. On the other hand, Table II shows that energy efficiency and FOM2 of ADC-based receivers need to be further improved compared with analog receivers [25], [26], [27].

A key outcome of this work is the demonstration of information-based metric benefits, such as the BER, in reducing the ADC precision requirements, and the identification of conditions that maximize the BER improvement offered by a BOA receiver over a CUA receiver under the same condition. Although we demonstrate BOA concept via a flash ADC, BOA is applicable to different ADC architectures in principle, because BOA adjusts the ADC thresholds but does not change the ADC architecture. However, the power savings when designing BOA using other ADC architectures will not be as great as with flash ADCs. In particular, for flash ADC every bit decrease in resolution almost halves the size of the ADC core circuitry and the power. In contrast, for a SAR, pipelined, or sigma-delta ADC, the die size and power will decrease linearly with a decrease in resolution.

VI. Conclusions

This paper studies the benefits of BOA for serial links. First, we discuss conditions that maximize BER improvement by a BOA receiver over a CUA receiver, and propose two channel-dependent parameters to quantify these conditions. Furthermore, a $4\,\mathrm{Gb/s}$ BOA receiver, which employs the true system BER to adjust the ADC representation levels and a linear equalizer, was implemented in $90\,\mathrm{nm}$ LP CMOS to demonstrate that a 3-bit BOA needs a lower SNR than a 4-bit CUA at a BER < 10^{-12}. This study verifies that the use of information-based metric (BER) to design ADC in serial links enables about $50\,\%$ power savings in the ADC while achieving even better BER performance compared with a CUA receiver.

VII. Acknowledgment

This work was supported in part by Systems on Nanoscale Information fabriCs (SONIC), one of the six SRC STARnet Centers, sponsored by SRC and DARPA. The authors acknowledge discussions with Hyeon-Min Bae (KAIST) and Pavan Hanumolu (UIUC).

Appendix

In this Appendix, we derive (7).

In an ADC-ML receiver, the BER of a $log_2(N+1)$-bit BOA is given by:

$$p_{eo}(SNR, B_o) = \sum_{k=1}^{N} p_{eo,k}, \tag{8}$$

where $p_{eo,k}$ is the BER contribution from the k^{th} μ-transition. Specifically, $p_{eo,k}$ includes the BER contribution from all the peaks $\mathcal{N}(x; \mu_l^+, \sigma_n)$ with $\mu_l^+ \in \boldsymbol{\mu}^+$ $\left(\mathcal{N}(x; \mu_l^-, \sigma_n) \text{ with } \mu_l^- \in \boldsymbol{\mu}^-\right)$ to the interval $[t_{o,k}^l, t_{o,k})$ and the BER contribution from all the peaks $\mathcal{N}(x; \mu_l^-, \sigma_n)$ with $\mu_l^- \in \boldsymbol{\mu}^-$ $\left(\mathcal{N}(x; \mu_l^+, \sigma_n) \text{ with } \mu_l^+ \in \boldsymbol{\mu}^+\right)$ to the interval $[t_{o,k}, t_{o,k}^r)$ if the memoryless ML decision for the interval $[t_{o,k}^l, t_{o,k})$ is -1 $(+1)$, where $t_{o,k}^l$ and $t_{o,k}^r$ are defined as follows,

$$t_{o,k}^l = \begin{cases} -\infty, & \text{if } k = 1 \\ \frac{t_{o,k-1}+t_{o,k}}{2} & , \text{ if } 1 < k \le N \end{cases},$$

$$t_{o,k}^r = \begin{cases} \frac{t_{o,k}+t_{o,k+1}}{2}, & \text{if } 1 \le k < N \\ +\infty, & \text{if } k = m \end{cases}.$$

Note: if the decision for the interval $[t_{o,k}^l, t_{o,k})$ is $+1$ (or -1) then the decision for the interval $[t_{o,k}, t_{o,k}^r)$ is -1 (or $+1$). At high SNR, this contribution is well-approximated by:

$$p_{eo,k} \approx 2^{-(L-1)} Q\left(\frac{d_{o,k}^*}{\sigma_n}\right), \tag{9}$$

where $d_{o,k}^*$ (see **Definition** 5) is the minimum distance of the k^{th} BOA threshold to the nearest noise-free channel output μ.

Substituting (9) into (8), employing the high SNR approximation for the Q-function ($Q(y) \approx \frac{1}{y\sqrt{2\pi}} e^{\frac{-y^2}{2}}$, for $y > 0$), and the approximation $\sum_k e^{a_k} \approx e^{\max\limits_k(a_k)}$, we get:

$$\begin{aligned} p_{eo}(SNR, B_o) &= \sum_{k=1}^{N} p_{eo,k} \approx \sum_{k=1}^{N} \left[2^{-(L-1)} Q\left(\frac{d_{o,k}^*}{\sigma_n}\right)\right] \\ &= \sum_{k=1}^{N} \left[2^{-(L-1)} \frac{\sigma_n}{\sqrt{2\pi} d_{o,k}^*} e^{-\frac{1}{2}\left(\frac{d_{o,k}^*}{\sigma_n}\right)^2}\right]. \\ &\approx 2^{-(L-1)} \frac{\sigma_n}{\sqrt{2\pi} d_{o,min}} e^{-\frac{1}{2}\left(\frac{d_{o,min}}{\sigma_n}\right)^2} \end{aligned} \tag{10}$$

Similarly, the BER of a $log_2(M+1)$-bit CUA receiver is given by:

$$p_{eu}(SNR, B_u) = \sum_{k=1}^{M+1} p_{eu,k}, \tag{11}$$

where $p_{eu,k}$ denotes the BER contributed by the k^{th} interval $I_{u,k}$. Specifically, $p_{eu,k}$ includes BER contribution from all the peaks $\mathcal{N}(x; \mu_l^+, \sigma_n)$ with $\mu_l^+ \in \boldsymbol{\mu}^+$ $\left(\mathcal{N}(x; \mu_l^-, \sigma_n) \text{ with } \mu_l^- \in \boldsymbol{\mu}^-\right)$ to the interval $I_{u,k}$ if the memoryless ML decision for the interval $I_{u,k}$ is -1 $(+1)$. At high SNR, this contribution is well-approximated by:

$$p_{eu,k} \approx 2^{-L} Q\left(\frac{d_{u,k}^*}{\sigma_n}\right), \tag{12}$$

where $d_{u,k}^*$ (see **Definition** 7) is the minimum distance of the k^{th} dominant noise-free output μ_k^* from the boundaries of the interval $I_{u,k}$.

Substituting (12) into (11), employing the high SNR approximation for the Q-function, the approximation $\sum_k e^{a_k} \approx e^{\max\limits_k(a_k)}$, and the relationship $Q(y) = 1 - Q(-y)$ for $y < 0$, we get:

$$\begin{aligned} &p_{eu}(SNR, B_u) \\ &= \sum_{k=1}^{M+1} p_{eu,k} \approx \sum_{k=1}^{M+1} \left[2^{-L} Q\left(\frac{d_{u,k}^*}{\sigma_n}\right)\right] \\ &\approx 2^{-L} Q\left(\frac{d_{u,min}}{\sigma_n}\right) \end{aligned}$$

$$= \begin{cases} 2^{-L}\frac{\sigma_n}{\sqrt{2\pi}d_{u,min}}e^{-\frac{1}{2}\left(\frac{d_{u,min}}{\sigma_n}\right)^2}, & \text{if } d_{u,min} > 0 \\ 2^{-L}\left[1+\frac{\sigma_n}{\sqrt{2\pi}d_{u,min}}e^{-\frac{1}{2}\left(\frac{d_{u,min}}{\sigma_n}\right)^2}\right], & \text{if } d_{u,min} < 0 \\ 2^{-(L+1)}, & \text{if } d_{u,min} = 0 \end{cases} \cdot \quad (13)$$

Therefore, from (10) and (13), we obtain:

$$BERR(SNR, B_u, B_o) = \frac{p_{eu}(SNR, B_u)}{p_{eo}(SNR, B_o)} \approx \begin{cases} \frac{d_{o,min}}{2d_{u,min}}e^{\frac{d_{o,min}^2 - d_{u,min}^2}{2\sigma_n^2}}, & \text{if } d_{u,min} > 0 \\ \frac{d_{o,min}}{2d_{u,min}}e^{\frac{d_{o,min}^2 - d_{u,min}^2}{2\sigma_n^2}}(1+\chi), & \text{if } d_{u,min} < 0 \\ \sqrt{\frac{\pi}{8}}\frac{d_{o,min}}{\sigma_n}e^{\frac{d_{o,min}^2}{2\sigma_n^2}}, & \text{if } d_{u,min} = 0 \end{cases}, \quad (14)$$

where $\chi = \frac{\sqrt{2\pi}d_{u,min}}{\sigma_n}e^{\frac{d_{u,min}^2}{2\sigma_n^2}}$. Note: $d_{o,min} \geq d_{u,min}$ and $d_{o,min} \geq 0$. Applying the approximation $\sum_k e^{a_k} \approx e^{\max\limits_k(a_k)}$ to the case when $d_{u,min} < 0$, (14) can be further simplified to (7).

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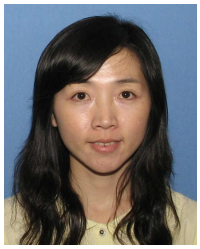

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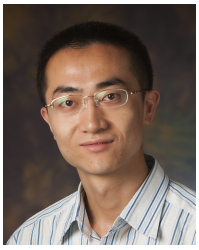

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Elyse Rosenbaum received the B.S. degree (with distinction) from Cornell University in 1984, the M.S. degree from Stanford University in 1985, and the Ph.D. degree from the University of California, Berkeley in 1992. All of these degrees were in electrical engineering. From 1984 through 1987, she was a Member of Technical Staff at AT&T Bell Laboratories in Holmdel, NJ. She is currently a Professor in the Department of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign.

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Dr. Rosenbaum has been a visiting professor at Katholieke University in Leaven, Belgium and National Chiao-Tung University in Hsinchu, Taiwan. She has been the recipient of a Best Student Paper Award from the IEDM, an Outstanding Paper Award from the EOS/ESD Symposium, a Technical Excellence Award from the SRC, an NSF CAREER award, an IBM Faculty Award, and a UIUC Bliss Faculty Scholar Award. She is a Fellow of the IEEE.

Andrew C. Singer received the S.B., S.M., and Ph.D. degrees, all in electrical engineering and computer science, from the Massachusetts Institute of Technology. From 1996 to 1998, he was a Research Scientist at Sanders, A Lockheed Martin Company in Manchester, New Hampshire. Since 1998, he has been on the faculty of the Department of Electrical and Computer Engineering at the University of Illinois at Urbana-Champaign, where he currently holds a Fox Family Endowed Professorship in the Electrical and Computer Engineering department. His research interests include signal processing and communication systems. In 2000, he co-founded Intersymbol Communications, Inc., a fabless semiconductor IC company, based in Champaign, Illinois, which built the world's fastest signal-processing-enhanced receivers for 10Gb/s optical communications. In 2007, Intersymbol Communications, Inc. was acquired by Finisar Corporation (FNSR). He continues to work in areas related to signal processing algorithms and their potential to enhance mixed-signal analog and digital circuits both in his research and as Associate Director of the SRC-funded Systems On Nanoscale Information fabriCs (SONIC) center. He received the National Science Foundation CAREER Award in 2000; in 2001 he received the Xerox Faculty Research Award, and in 2002 he was named a Willett Faculty Scholar. In 2005, he was appointed the Director of the Technology Entrepreneur Center at the University of Illinois, where he directs a wide range of entrepreneurship activities in the College of Engineering. In 2006 he received the IEEE Journal of Solid State Circuits Best Paper Award for the paper entitled "An MLSE Receiver for Electronic Dispersion Compensation of OC-192 Fiber Links." In 2008, he received the IEEE Signal Processing Magazine Award for the paper entitled "Turbo Equalization." In 2009, he was elected Fellow of the IEEE "for contributions to signal processing techniques for digital communication," and in 2014, he was named as a Distinguished Lecturer of the IEEE Signal Processing Society.