Low-Power Filtering via Adaptive Error-Cancellation

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***Abstract*—A low-power technique for digital filtering referred to as *adaptive error-cancellation* (AEC) is presented in this paper. The AEC technique falls under the general class of *algorithmic noise-tolerance* (ANT) techniques proposed earlier for combating transient/soft errors. The proposed AEC technique exploits the correlation between the input and soft errors to estimate and cancel out the latter. In this paper, we apply AEC along with *voltage overscaling* (VOS), where the voltage is scaled beyond the minimum (referred to as $V_{dd\text{-}crit}$) necessary for correct operation. We employ the AEC technique in the context of a frequency-division multiplexed (FDM) communication system and demonstrate that up to 71% energy reduction can be achieved over present-day voltage-scaled systems.**

***Index Terms*—Adaptive filtering, algorithmic noise-tolerance, algorithm transformations, fault tolerance, low power, soft DSP, voltage scaling.**

I. Introduction

THE RAPID growth in demand for portable and wireless computing systems is driving the need for increasingly higher functionality with low energy consumption [1]–[4]. However, with feature sizes being scaled into the deep submicron (DSM) regime, the emergence of DSM noise [5], [6] consisting of ground bounce, crosstalk, IR drops, clock jitter, charge sharing, process variations, etc., resulting from relentless scaling of feature sizes [7], has raised questions about our ability to design reliable and efficient (hence affordable) microsystems and, hence, the ability to extend Moore's law [8] well into the deep submicron regime.

Our past research [9]–[11] on energy-efficiency bounds of DSM VLSI systems in the presence of noise strongly suggests that design techniques based on *noise-tolerance* need to be developed if energy-efficiency and reliability are to be jointly addressed. Indeed, the 2001 International Technology Roadmap for Semiconductors [7] refers to *error-tolerance* as a design challenge for the next decade. We have developed noise-tolerance at the algorithmic [12] as well as circuit [13] levels of the design hierarchy. In [12], we proposed algorithmic noise-tolerance (ANT) as a technique that, when combined with supply *voltage overscaling* (VOS), enables the design of low-power signal processing systems that operate at energy-efficiencies beyond those achieved by present-day systems. The overall approach of employing VOS in combination with ANT for low-power is referred to as *soft DSP*. In soft DSP systems, energy efficiency and reliability issues are addressed jointly. This is the key difference between the ANT and fault-tolerant computing techniques [14]–[18].

In this paper, we propose a new ANT technique referred to as *adaptive error-cancellation* (AEC). The proposed AEC technique is based on the observation that soft errors at the output of a voltage overscaled system exhibits an extremely complicated (though deterministic) dependence on the input signal and the underlying datapath architecture. Hence, by modeling the soft-error signal as a stochastic process and exploiting its correlation with the input signal, one can devise an error cancellation scheme that is akin to echo cancellation techniques employed in voiceband modems. The configuration of the error cancellation scheme can be calibrated adaptively by the well-known *least mean square* (LSM) algorithm.

We optimize the proposed AEC technique by developing an energy-optimum AEC design that minimizes the energy overhead due to error cancellation while being subject to an algorithmic performance constraint. In comparison with the previously proposed *prediction-based error-control* (PEC) scheme [12] for narrowband frequency-selective filters, the proposed AEC technique is well-suited for broadband signal processing and communication systems, e.g., 3G wireless communications [19], [20] and next-generation digital subscriber loop (DSL) systems [21], [22]. We employ the proposed AEC technique to design a low-power frequency-division multiplexed (FDM) system [23] for which the input signal is composed of several bandlimited signals occupying adjacent frequency bands. Simulation results demonstrate that an AEC-based filter achieves 43–71% energy savings without incurring any algorithmic degradation.

The paper is organized as follows. In Section II, we review our past work on ANT. In Section III, we propose the adaptive error-cancellation (AEC) technique that is suitable for the design of low-power broadband DSP and communication systems. An energy-optimum AEC design strategy is developed in Section IV. Simulation results are presented and evaluated in Section V.

II. Algorithmic Noise-Tolerance (ANT)

In this section, we present VOS and ANT and describe their use in the design of low-power signal processing systems.

A. Voltage Overscaling (VOS)

Dedicated DSP implementations are designed subject to an application-specific throughput requirement. Specifically, for correct operation, the critical path delay T_{cp} of the DSP

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architecture should be less than or equal to the sample period T_s of the application, i.e.,

$$T_{cp} \leq T_s. \tag{1}$$

The critical path delay T_{cp} is a function of the supply voltage. As voltage is scaled down, power dissipation reduces quadratically (assuming that dynamic power is the dominant source), whereas the delay (including the critical path delay T_{cp}) increases. At a certain point, (1) is violated, and soft errors start to appear internally and eventually at the output. The supply voltage at which $T_{cp} = T_s$ is referred to as the critical supply voltage and denoted as $V_{dd\text{-}crit}$. Present-day voltage scaling stops at the point where $V_{dd} = V_{dd\text{-}crit}$. Overscaling supply voltage beyond $V_{dd\text{-}crit}$ results in output errors if critical paths, and other longer paths are excited by certain input patterns, i.e., soft errors occur. This induces algorithmic performance degradation such as a loss in the output signal-to-noise ratio (SNR).

For the purpose of illustration, consider a simple four-tap FIR filter implementation as shown in Fig. 1. The worst-case delay is shown to be $22T_{a,V_{dd}}$, where $T_{a,V_{dd}}$ is the propagation delay of 1-bit full adder at V_{dd}. Assume that the supply voltage is overscaled to a value $V_{dd\text{-}sub} < V_{dd\text{-}crit}$ such that $T_{a,V_{dd\text{-}sub}} = 1.375T_{a,V_{dd\text{-}crit}}$, i.e., VOS is applied. With the same clock rate (throughput), we see that

$$T_s = 22T_{a,V_{dd\text{-}crit}} = 16T_{a,V_{dd\text{-}sub}} \tag{2}$$

but

$$T_{cp,V_{dd\text{-}sub}} = 22T_{a,V_{dd\text{-}sub}}. \tag{3}$$

This indicates that the top six MSBs of the filter output will be in error when input patterns exciting the critical paths and other longer paths are applied. Note that most arithmetic units employed in practice use LSB-first computation. This makes soft errors appear at the MSBs first, thereby creating errors of large magnitude. Hence, error detection is easy, but error correction is difficult to achieve. This opens up a unique opportunity for ANT.

B. Algorithmic Noise-Tolerance

The key idea behind ANT is to employ a low-complexity error-control block that detects and corrects errors that may arise in a comparatively large VOS block. An effective ANT technique is one that has low complexity (compared with the VOS block) and is able to mitigate the performance degradation. These techniques may observe the input, output, and certain intermediate signals of the VOS block to generate an output $y_o[n] \approx y[n]$, where $y[n]$ is the error-free output of the VOS block.

We now derive the conditions under which soft DSP leads to energy savings over optimal error-free voltage-scaled systems (defined as systems operating at $V_{dd\text{-}crit}$). The dynamic energy dissipation per clock cycle $\mathcal{E}_{\text{orig}}$ of such a system is given by

$$\mathcal{E}_{\text{orig}} = C_{\text{orig}}{V_{dd\text{-}crit}}^2 \tag{4}$$

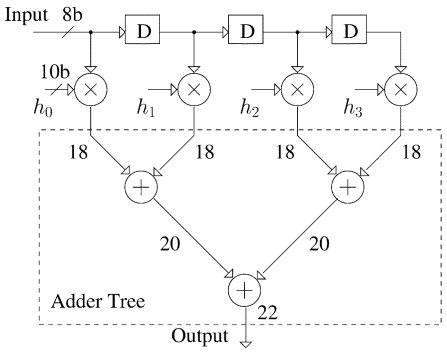

Fig. 1. Delay of a simple four-tap filter.

where C_{orig} is the average switching capacitance that accounts for signal transition activities, voltage swing ranges, load, and parasitic capacitances at all of the circuit nodes. It can be regarded as a measure of the hardware complexity of the underlying architecture. Note that $\mathcal{E}_{\text{orig}}$ is the minimum energy dissipation that conventional voltage scaling can achieve.

In comparison, the dynamic energy dissipation per clock cycle $\mathcal{E}_{\text{soft}}$ of the corresponding soft DSP system is given by

$$\mathcal{E}_{\text{soft}} = C_{\text{orig}}\left(\frac{V_{dd\text{-}crit}}{k_{\text{vos}}}\right)^2 + C_{\text{ANT}}V_{dd\text{-}ant}^2 \tag{5}$$

where C_{ANT} represents the overhead complexity due to ANT, $V_{dd\text{-}ant}$ is the critical supply voltage for the ANT-based error-control block, and $k_{\text{vos}} > 1$ is the VOS factor (VOSF). From (4) and (5), it can be easily shown that $\mathcal{E}_{\text{soft}} < \mathcal{E}_{\text{orig}}$, provided

$$C_{\text{ANT}}V_{dd\text{-}ant}^2 < C_{\text{orig}}V_{dd\text{-}crit}^2\left(1 - \frac{1}{{k_{\text{vos}}}^2}\right). \tag{6}$$

In practice, the condition in (6) is easily satisfied by making C_{ANT} as small as possible and/or by making k_{vos} as large as possible. There is indeed an interesting direct relationship between k_{vos} and C_{ANT}. When k_{vos} is increased, the performance degradation becomes larger as more critical paths and other longer paths start to fail. This requires increasingly sophisticated and perhaps complex ANT techniques that may increase C_{ANT}.

Fig. 2 depicts the previously proposed *prediction-based error-control* (PEC) technique [12]. The PEC technique is effective in reducing energy dissipation for narrowband filters while incurring a minor performance loss. Many modern-day DSP and communication applications require broadband signal processing techniques. In this paper, we propose an ANT technique referred to as *adaptive error-cancellation* (AEC), which is suitable for broadband signal processing.

III. Adaptive Error Cancellation

In this section, we present the AEC technique. The soft-error signal is modeled as a stochastic process, and the cross-correlation between the input signal and the soft-error signal is exploited for error control. As soft errors are input dependent, they can be regarded as an *echo* of the input signal, and hence, echo cancellation algorithms used in modern communication systems can be employed to effectively restore the system performance.

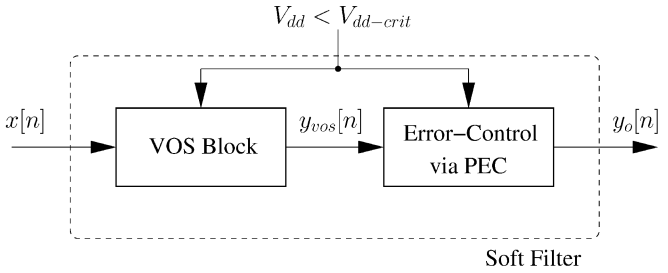

Fig. 2. Past work on the prediction-based error-control (PEC) technique.

A. AEC Algorithm

Fig. 3 illustrates the proposed AEC technique. In the presence of soft errors due to VOS, the output $y_{\rm vos}[n]$ of an N-tap VOS filter $H(z)$ can be expressed as

$$y_{\rm vos}[n] = \sum_{k=0}^{N-1} h_k x[n-k] + e_s[n] = y[n] + e_s[n] \quad (7)$$

where $y[n]$ is the error-free output, $e_s[n]$ is the soft output error, h_k is the kth-tap coefficient, and $x[n-k]$ is the kth delayed input sample.

For a given implementation of $H(z)$, soft error $e_s[n]$ depends on the input samples $x[n]$, $x[n-1]$, …, $x[n-N+1]$. Therefore, an error canceler $H_c(z)$ can be employed to generate a statistical replica of the soft errors from these input samples, which can then be subtracted from the output. The resulting estimate of $e_s[n]$, which is denoted by $\hat{e}_s[n]$, is given by

$$\hat{e}_s[n] = \sum_{k=0}^{N-1} w_k x[n-k] \quad (8)$$

where $\underline{\mathbf{w}} = \{w_0, w_1, \ldots, w_{N-1}\}$ is the coefficient vector of the error canceler $H_c(z)$. It can be chosen to minimize the estimation error $e[n]$, which is defined as

$$e[n] = e_s[n] - \hat{e}_s[n]. \quad (9)$$

Here, we use the commonly employed *minimum mean-squared error* (MMSE) criterion that minimizes

$$\mathcal{J}[n] = E\left(e[n]^2\right). \quad (10)$$

While the value of $\underline{\mathbf{w}}$ that minimizes (10) can be obtained as a solution to the Weiner–Hopf equation [24], in practical signal processing systems, an adaptive algorithm such as the *least mean square* (LMS) algorithm [24] given below is commonly employed:

$$\hat{e}_s[n] = \sum_{k=0}^{N-1} \hat{w}_k[n-1] x[n-k] \quad (11)$$

$$e[n] = e_s[n] - \hat{e}_s[n] \quad (12)$$

$$\hat{w}_k[n] = \hat{w}_k[n-1] + \mu e[n]^* x[n-k] \quad (13)$$

where $\underline{\hat{\mathbf{w}}} = \{\hat{w}_0[n], \hat{w}_1[n], \ldots, \hat{w}_{N-1}[n]\}$ is an estimate of the optimum tap-weight vector of $H_c(z)$, $e[n]^*$ is the complex conjugate of $e[n]$, and μ is the step size. The computations in (11) are done in the filter (F) block of the AEC and those in (13) are executed in the weight-update (WUD) block. Note that the feedback loop shown in Fig. 3 is employed to adapt the error canceler. The stability of this feedback structure is governed by the well-known stability analysis of the LMS algorithm, which can be found in [24]. This analysis shows that stability is guaranteed as long as the step-size μ is less than an upper bound.

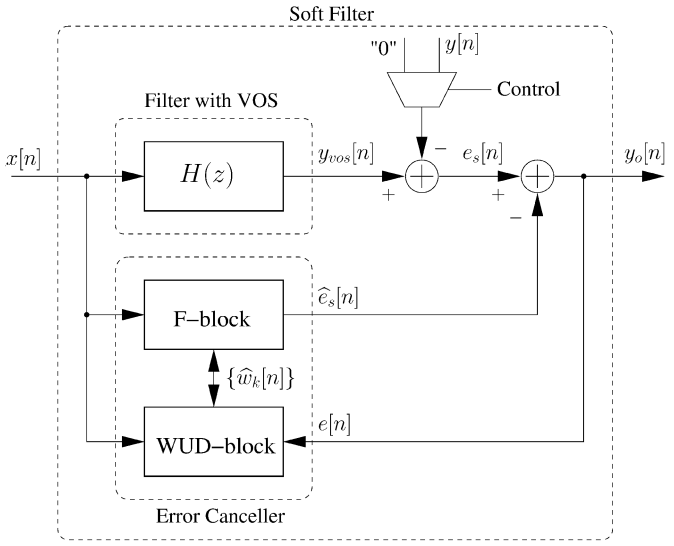

Fig. 3. Proposed adaptive error-cancellation technique.

A practical approach to implement the AEC algorithm described above is to have an auto-calibration phase during powerup. Note that such calibration is commonly used in many practical adaptive systems. During this phase, a predefined input signal is passed through the VOS filter $H(z)$, and a precomputed error-free output $y[n]$ is used as the desired signal (see the multiplexer in Fig. 3). After the tap-weight vector $\underline{\hat{\mathbf{w}}}$ has converged, the WUD-block can be powered-down, and the multiplexer control signal can be flipped so that $\hat{e}_s[n]$ gets subtracted directly from the output $y_{\rm vos}[n]$, thereby canceling out the soft errors. If the WUD-block is left powered up then the error canceler would be able to track variations in the temperature.

B. Algorithmic Performance Measures

We now define algorithmic performance measures needed for characterizing the energy-optimum AEC design presented in Section IV. Note that the filter output under VOS can be written as

$$y_{\rm vos}[n] = y[n] + e_s[n] = s[n] + \eta[n] + e_s[n] \quad (14)$$

where $y[n]$ is the error-free output composed of a desired signal $s[n]$ and signal noise $\eta[n]$, and $e_s[n]$ denotes the soft error due to VOS. While the relationship between $e_s[n]$ and the input is deterministic, it is extremely complex for any reasonable-sized filters. Hence, we choose to model this relationship in a statistical manner by quantifying the degradation in the output SNR.

Definition 1: The output SNR of a conventional VOS filter is defined as $\text{SNR}_{\rm vos}$, which is given by

$$\text{SNR}_{\rm vos} = 10\log_{10}\left(\frac{\sigma_s^2}{\sigma_n^2 + \sigma_{es}^2}\right) \quad (15)$$

where σ_s^2, σ_n^2, and σ_{es}^2 are the variances of the desired signal $s[n]$, signal noise $\eta[n]$, and soft error $e_s[n]$, respectively.

Definition 2: The output SNR of a soft filter employing the AEC for ANT is defined as SNR_{ANT}, which is given by

$$\text{SNR}_{\text{ANT}} = 10\log_{10}\left(\frac{\sigma_s^2}{\sigma_n^2+\sigma_e^2}\right) \tag{16}$$

where σ_e^2 is the variance of the residual soft error $e[n]$ [or estimation error, see (12)] after the AEC.

In practice, AEC-based soft filters are designed for an application-specific performance requirement $\text{SNR}_{\text{design}}$, such that

$$\text{SNR}_{\text{ANT}} \geq \text{SNR}_{\text{design}} = \left(\frac{\sigma_s^2}{\sigma_{n,\,\text{design}}^2}\right) \tag{17}$$

where $\sigma_{n,\,\text{design}}^2$ denotes the variance of the worst-case signal noise $\eta[n]$ at the filter output.

The error canceler $H_c(z)$ in Fig. 3 is an adaptive filter that takes the soft error $e_s[n]$ as the desired signal and generates the estimated signal $\hat{e}_s[n]$ as its output. Thus, the estimation error $e[n]$ between $e_s[n]$ and $\hat{e}_s[n]$ is seen as the output noise. The AEC algorithm given in (11)–(13) must achieve the algorithmic performance as specified in (17) for a given $\text{SNR}_{\text{design}}$. Parameters that determine the SNR_{ANT} include the VOSF, length N_c of the error canceler $H_c(z)$, precision B_F of the F-block, and precision B_{WUD} of the WUD-block.

C. Energy-Savings Measures

The average energy savings $\mathcal{E}_{\text{sav}}$ achieved by an AEC-based soft filter is defined as

$$\mathcal{E}_{\text{sav}} = \left(1-\frac{\mathcal{E}_{\text{soft}}}{\mathcal{E}_{\text{conv}}}\right)\times 100\% \tag{18}$$

where $\mathcal{E}_{\text{conv}}$ is the energy dissipation of the conventional filter at the optimally scaled voltage of $V_{dd\text{-}crit}$, and $\mathcal{E}_{\text{soft}}$ is the energy dissipation of the soft filter at the overscaled voltage of $V_{dd\text{-}sub}$. It can be seen from Fig. 3 that $\mathcal{E}_{\text{soft}}$ is given by

$$\mathcal{E}_{\text{soft}} = \mathcal{E}_H + \mathcal{E}_{\text{AEC}} \tag{19}$$

where $\mathcal{E}_H$ and $\mathcal{E}_{\text{AEC}}$ are the energy dissipations of the primary filter $H(z)$ and the error canceler $H_c(z)$, respectively.

For a given input signal, the value of $\mathcal{E}_H$ is determined by the supply voltage $V_{dd\text{-}sub}$, length N, and coefficients $\{h_0, h_1, \ldots, h_{N-1}\}$ of the primary filter $H(z)$. To quantify $\mathcal{E}_{\text{AEC}}$, we define a vector $\underline{\mathbf{b}} = \{b_0, b_1, \ldots, b_{N-1}\} \in \mathcal{B}^N$, where N is the length of the primary filter $H(z)$, and $\mathcal{B}^N$ is an N-dimension vector space with binary elements b_js $\in \{0, 1\}$. We denote $b_j = 1$ if the jth tap of the error canceler $H_c(z)$ is powered up and $b_j = 0$ otherwise. The length N_c of $H_c(z)$ can be written as

$$N_c = \sum_{j=0}^{N-1} b_j. \tag{20}$$

We assume that the WUD-block is switched off after $H_c(z)$ has converged. This gives

$$\mathcal{E}_{\text{AEC}}(\underline{\mathbf{b}}) = \sum_{j=0}^{N-1} b_j \mathcal{E}_{F,\,j} \tag{21}$$

where $\mathcal{E}_{F,\,j}$ is the energy dissipation due to the jth tap of $H_c(z)$. Given the coefficient w_j, $\mathcal{E}_{F,\,j}$ can be estimated as a function of w_j via the weighted multiplier energy model [25]. Note that $\mathcal{E}_{F,\,j}$ can be obtained via any of the available power modeling approaches [26], [27] and then employed to solve the energy optimization problem.

To achieve maximum energy savings, we need to minimize $\mathcal{E}_{\text{soft}}$ subject to the performance constraint (17). This is formulated as an energy optimization problem as given in

$$\begin{aligned} &\text{minimize:} && \mathcal{E}_{\text{soft}} = \mathcal{E}_H + \mathcal{E}_{\text{AEC}} \\ &\text{subject to:} && \text{SNR}_{\text{ANT}} \geq \text{SNR}_{\text{design}}. \end{aligned} \tag{22}$$

In the next section, we will derive the energy-optimum AEC design based on the solution of (22).

IV. Energy-Minimum Error-Cancellation Algorithm

We now consider a given filter $H(z)$ whose length N and coefficients $\{h_0, h_1, \ldots, h_{N-1}\}$ are determined by frequency domain specifications such as filter bandwidth. For a given input signal, energy dissipation $\mathcal{E}_H$ of $H(z)$ is a function of the supply voltage $V_{dd\text{-}sub}$ or equivalently the VOSF. From (21), energy dissipation $\mathcal{E}_{\text{AEC}}$ of the corresponding error canceler $H_c(z)$ is a function of the VOSF and vector $\underline{\mathbf{b}}$. Thus, $\mathcal{E}_{\text{soft}}$ in (22) is a function of VOSF and vector $\underline{\mathbf{b}}$ only, of which the energy-optimum solutions are provided in Sections IV-A and B, respectively.

A. Energy-Optimum VOSF

To illustrate the relationship between $\mathcal{E}_{\text{soft}}$ and VOSF, we rewrite (5) as

$$\mathcal{E}_{\text{soft}} = C_{\text{orig}}\left(\frac{V_{dd\text{-}crit}}{k_{\text{vos}}}\right)^2 + C_{\text{ANT}}V_{dd\text{-}ant}^2 \tag{23}$$

$$= (C_{\text{orig}} + C_{\text{ANT}})\left(\frac{V_{dd\text{-}crit}}{k_{\text{vos}}}\right)^2 \tag{24}$$

where C_{orig} and $V_{dd\text{-}crit}$ are determined by the architecture of the primary filter $H(z)$, $V_{dd\text{-}ant} = V_{dd\text{-}crit}/k_{\text{vos}}$ is the supply voltage for the error canceler $H_c(z)$, and $k_{\text{vos}} > 1$ is the VOSF. The first and second terms on the right-hand side of (23) correspond to $\mathcal{E}_H$ and $\mathcal{E}_{\text{AEC}}$ in (19), respectively.

Note that C_{ANT} and k_{vos} in (24) are related. Starting with $k_{\text{vos}} = 1$ and $C_{\text{ANT}} = 0$, C_{ANT} increases with k_{vos} because more and more taps of $H(z)$ contribute to the soft errors at the output and the magnitude of the soft errors themselves increase. However, the relationship between C_{ANT} and k_{vos} is extremely complex and nonlinear. Hence, in this paper, we find the optimum value of k_{vos} by determining the optimum value of C_{ANT} for a given value of k_{vos}, as described next. It is shown in our simulations that k_{vos} needs to be maximized at the point where the algorithmic performance constraint in (22) is just satisfied.

B. Energy-Optimum AEC

We now derive the energy-optimum $\underline{\mathbf{b}}$ for a given $H(z)$ and VOSF. The reason for the existence of energy-optimum AEC is that performance degradation due to VOS is dominated by soft errors from a few of the taps of $H(z)$ having large coefficient

magnitude as these taps can easily excite the critical paths and other longer paths thereby contributing more to the performance degradation. Therefore, a reduced-order AEC exists that can restore the algorithmic performance.

In what follows, we assume a zero-mean and uncorrelated input signal $x[n]$. This is a reasonable assumption for most practical broadband systems because such systems employ scramblers to deliberately "whiten" input signals for the purpose of easing timing recovery functions in the receiver and combating interference. Note that the above assumption on input signal is only for the purpose of simplifying the mathematical development so that the key advantages of the proposed AEC technique can be illustrated clearly. In Section V, we relax this assumption to include nonzero mean and correlated signals.

From (8), (9), and (20), the variance of residual soft error $e[n]$ after cancellation by the AEC can be expressed as

$$\sigma_e^2 = \sigma_{es}^2 - \sum_{j=0}^{N-1} b_j w_j^2 \sigma_x^2 \tag{25}$$

where σ_x^2 and σ_{es}^2 are the variances of the input signal $x[n]$ and soft output error $e_s[n]$, respectively, for the given $H(z)$ and VOSF, and w_js are the optimum coefficients of $H_c(z)$, given by [24]

$$w_j = \frac{E\left(x[n-j]e_s[n]\right)}{\sigma_x^2}. \tag{26}$$

Note that from (16) and (17), σ_e^2 in (25) due to the N_c-tap $H_c(z)$ has the following constraint:

$$\sigma_e^2 \le \sigma_{n,\,design}^2 - \sigma_n^2 \tag{27}$$

where σ_n^2 is determined by $H(z)$.

Using the above notations, the energy optimization problem for AEC can be expressed as an explicit function of the vector $\underline{\mathbf{b}}$, as follows:

$$\begin{aligned} \underset{\underline{\mathbf{b}}\in\mathcal{B}^N}{\text{minimize:}} \quad & \mathcal{E}_{\text{AEC}}(\underline{\mathbf{b}}) \\ \text{subject to:} \quad & \sigma_e^2 \le \sigma_{n,\,design}^2 - \sigma_n^2 \end{aligned} \tag{28}$$

where $\mathcal{E}_{\text{AEC}}(\underline{\mathbf{b}})$, σ_e^2, σ_n^2, and $\sigma_{n,\,design}^2$ are given by (21), (25), (16), and (17), respectively.

The optimization problem (28) can be solved via the Lagrange multiplier method [28]. We define the Lagrangian function $L(\underline{\mathbf{b}}, \lambda)$ as

$$\begin{aligned} L(\underline{\mathbf{b}}, \lambda) &= \mathcal{E}_{\text{AEC}}(\underline{\mathbf{b}}) + \lambda(\sigma_e^2 + \sigma_n^2 - \sigma_{n,\,\text{design}}^2) \\ &= \sum_{j=0}^{N-1} b_j(\mathcal{E}_{F,j} - \lambda w_j^2 \sigma_x^2) \\ &\quad + \lambda(\sigma_{es}^2 + \sigma_n^2 - \sigma_{n,\,\text{design}}^2) \end{aligned} \tag{29}$$

where λ is the *sensitivity vector* of the Lagrange multiplier. The solution to (28) is obtained at the point $(\underline{\mathbf{b}}^*, \lambda^*)$, satisfying

$$L(\underline{\mathbf{b}}^*, \lambda) \le L(\underline{\mathbf{b}}^*, \lambda^*) \le L(\underline{\mathbf{b}}, \lambda^*) \tag{30}$$

for any $\underline{\mathbf{b}} \in \mathcal{B}^N$ and $\lambda \ge 0$. It can be shown that $\underline{\mathbf{b}}^* = \{b_0^*, b_1^*, \ldots, b_{N-1}^*\} \in \mathcal{B}^N$ in (30) is given by [25]

$$b_j^* = \begin{cases} 1, & \text{if } \dfrac{\mathcal{E}_{F,j}}{w_j^2\sigma_x^2} < \lambda^* \\ 0, & \text{if } \dfrac{\mathcal{E}_{F,j}}{w_j^2\sigma_x^2} \ge \lambda^* \end{cases} \tag{31}$$

where λ^* is the optimum value of λ. The energy-optimum length $N_c^{\mathbf{opt}}$ of the error canceler $H_c(z)$ is obtained as

$$N_c^{\mathbf{opt}} = \sum_{j=0}^{N-1} b_j^*. \tag{32}$$

From (31), if the jth tap of $H_c(z)$ has a large coefficient w_j while consuming a relatively small energy $\mathcal{E}_{F,\,j}$, then $b_j^* = 1$. In other words, the input $x[n-j]$ has to be utilized to cancel the soft output errors. On the other hand, we can switch off the jth tap of $H_c(z)$ if this tap consumes more energy (large $\mathcal{E}_{F,\,j}$) but has a minor contribution in terms of error cancellation (small w_j). In practice, we can avoid the computation of λ^* by powering down those taps in $H_c(z)$ starting with the tap with the largest value of $\mathcal{E}_{F,\,j}/w_j^2\sigma_x^2$ and continuing until the performance constraint in (28) is violated.

We now describe the relationship between the performance degradation due to VOS and the energy-optimum AEC configuration. Denote $e_{s,\,j}[n]$ as the soft-error component from the jth tap of $H(z)$. As $e_{s,\,j}[n]$ is excited by the input $x[n-j]$, it is reasonable to assume that $e_{s,\,j}[n]$ is statistically independent of $e_{s,\,i}[n]$ and $x[n-i]$ for $i \ne j$. Thus, we can rewrite (26) as

$$w_j = \frac{E\left(x[n-j]\left(\sum_{i=0}^{N-1} e_{s,i}[n]\right)\right)}{{\sigma_x}^2} = \frac{E\left(x[n-j]e_{s,j}[n]\right)}{\sigma_x^2}. \tag{33}$$

In general, if the jth tap of $H(z)$ has a large coefficient h_j, then critical paths and other longer paths get excited easily, thereby resulting in a larger value for $e_{s,\,j}[n]$ and for $E(x[n-j]e_{s,\,j}[n])$. From (33), this implies that w_j is large, which in turn implies [from (31)] $b_j^* = 1$. This is to be expected as $e_{s,\,j}[n]$ is induced by $x[n-j]$ and thus can only be canceled by the jth tap of $H_c(z)$. As the filter bandwidth increases, the predominant contribution to the soft-error energy at the output will be from fewer taps of $H(z)$. This is because wideband filters have a narrow impulse response. Thus, more b_j^*s will be zero, resulting in a smaller $N_c^{\mathbf{opt}}$. This indicates that the proposed AEC technique is best suited for wideband filters.

Finally, we study the convergence characteristics of the energy-optimum AEC. Employing the same assumption on $x[n]$ as above, the *misadjustment* $\mathcal{M}$, which is defined as the ratio of the excess MSE (in the steady state) to the optimum MSE, can be expressed as [24]

$$\mathcal{M} \approx \frac{\mu}{2} N_c^{\mathbf{opt}} \sigma_x^2 \tag{34}$$

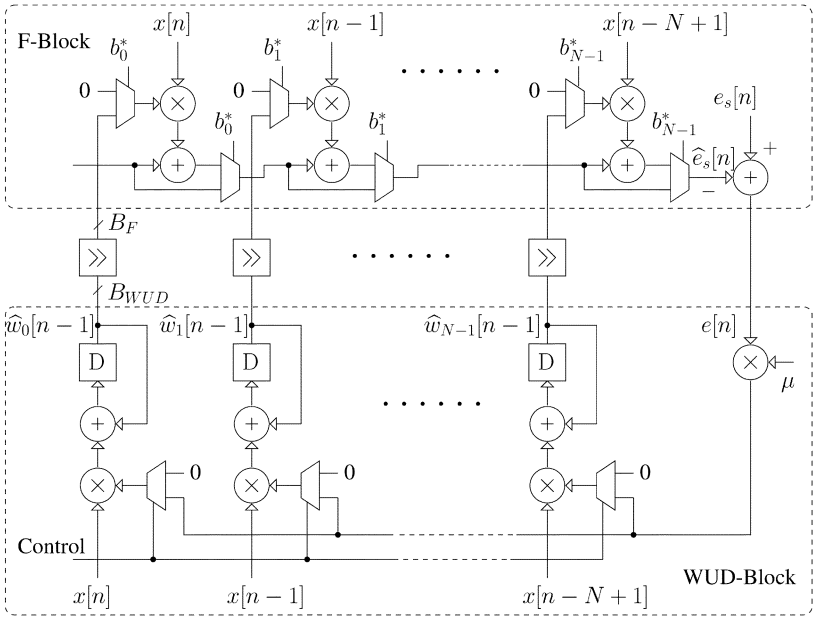

Fig. 4. Reduced-order AEC architecture.

whereas the *convergence time constant* $\tau_{\rm mse}$ is given by [24]

$$\tau_{\rm mse} \approx \frac{1}{2\mu\sigma_x^2}. \tag{35}$$

From (34), for the same amount of misadjustment, the energy-optimum AEC having a smaller $N_c^{\rm opt}$ can employ a larger step size μ for the calibration. This results in a faster settling time [see (35)] than that of a conventional AEC, thereby reducing the energy overhead during the calibration. This further demonstrates that the proposed AEC technique is well-suited for wideband filters.

C. Reduced-Order AEC Algorithm

Employing the energy-optimum AEC derived above, we propose a reduced-order LMS algorithm to compute the AEC coefficients, as shown in

$$\hat{e}_s[n] = \sum_{i=0}^{N_c^{\rm opt}-1} \hat{w}_{k_i}[n-1]x[n-k_i] \tag{36}$$

$$e[n] = y_{\rm vos}[n] - y[n] - \hat{e}_s[n] \tag{37}$$

$$\hat{w}_{k_i}[n] = \hat{w}_{k_i}[n-1] + \mu e[n]^* x[n-k_i] \tag{38}$$

where $N_c^{\rm opt}$ is given by (32) and $k_i = j$ if $b_j^* = 1$ in (31).

We now determine the precisions of F-block and WUD block in the energy-optimum AEC. Assuming a uniform stochastic model for the quantization errors in the coefficients $\hat{w}_{k_i}$s, the mean-squared quantization noise J_Q referred to the output of $H_c(z)$ is given by [29]

$$J_Q = \frac{N_c^{\rm opt}\sigma_x^2 A^2 2^{-2(B_F-1)}}{12} \tag{39}$$

where σ_x^2 is the variance of the input signal $x[n]$, A is the maximum magnitude of $\hat{w}_{k_i}$s, and B_F denotes the precision of $\hat{w}_{k_i}$s in the F-block.

To make quantization errors arbitrarily small, we define a factor $\alpha \ll 1$ such that $J_Q \le \alpha\sigma_e^2$, where σ_e^2 is given by (25). The precision B_F is then obtained as [30]

$$B_F \ge \frac{1}{2}\log_2\left(\frac{N_c^{\rm opt}A^2\sigma_x^2}{3\alpha\sigma_e^2}\right). \tag{40}$$

From (40), a smaller $N_c^{\rm opt}$ also reduces the precision of the F-block, thereby favoring energy reduction.

We employ the *stopping criterion* [31] to determine the precision of the WUD block. The stopping criterion asserts that the WUD block will stop adapting if the correction term $(\mu e[n]^* x[n-k_i])$ in (38) becomes smaller than half of the least significant bit of $\hat{w}_{k_i}$s. This can be expressed as

$$\mu^2\sigma_e^2\sigma_x^2 \ge A^2 2^{-2B_{\rm WUD}} \tag{41}$$

where $B_{\rm WUD}$ is the precision of $\hat{w}_{k_i}$s in the WUD block. From (41), the lower bound on $B_{\rm WUD}$ is given by

$$B_{\rm WUD} \ge \frac{1}{2}\log_2\left(\frac{A^2}{\mu^2\sigma_e^2\sigma_x^2}\right). \tag{42}$$

Fig. 4 shows the architecture of the proposed reduced-order AEC. Simulation results in the next section demonstrate significant reduction in hardware complexity as compared with the conventional LMS algorithm, whereas the performance loss is negligible. Thus, we are able to satisfy (6) easily. Furthermore, even if the supply voltage of the reduced-order AEC is made identical to that of the VOS $H(z)$ for simplicity of implementation, the reduced-order AEC is error-free because its critical path is much smaller than that of the filter $H(z)$.

V. Application to FDM Systems

In this section, we study the performance of the proposed AEC-based low-power filter in the context of a frequency-division multiplexed (FDM) communication system. FDM is

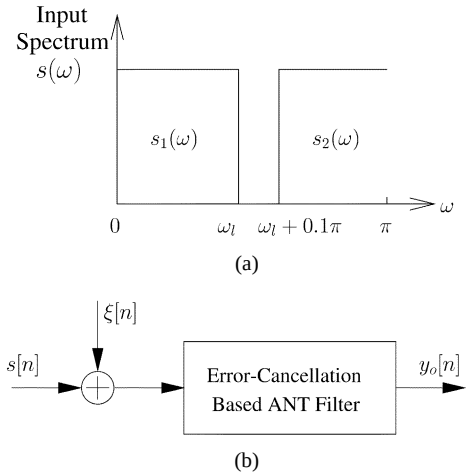

Fig. 5. Simulation setup. (a) Input signal spectrum. (b) Lowpass filtering via the proposed AEC technique.

employed in many broadband communication systems today such as very high-speed digital subscriber line and wireless communication standards. We first describe the simulation setup and then evaluate the achievable energy savings versus algorithmic performance tradeoff.

A. Simulation Setup

Fig. 5(a) illustrates the spectrum of the input signal $s[n]$, which consists of a baseband signal $s_1[n]$ occupying the $[0, \omega_l]$ band and a bandpass signal $s_2[n]$ in the adjacent $[\omega_l + 0.1\pi, \pi]$ band. This input signal emulates a FDM signal [23]. The input signal $s[n]$ is also corrupted by a white Gaussian noise source $\xi[n]$. We assume that all the signals $s_1[n]$, $s_2[n]$, and noise $\xi[n]$ are statistically independent.

The goal of the receiver signal processing is to extract the primary signal $s_1[n]$. This is accomplished by passing the input signal through a lowpass filter to suppress the out-of-band signal and noise components. We employ the optimization strategy given in Section IV to design AEC-based low-power filters that perform frequency-selective filtering [see Fig. 5(b)]. In order to evaluate the energy-performance tradeoff for FDM systems at different bandwidths, we vary the bandwidth ω_l of $s_1[n]$ from 0.3π to 0.8π. All the simulations employ the filter architecture shown in Fig. 1, where two's complement carry–save Baugh–Wooley multipliers [32] and ripple–carry tree-style adders are being employed.

We employ a logic level simulation to calculate the number of full-adder delays T_a on every path from the input to the filter output given a sequence of inputs. Thus, all paths, and not just the critical paths, are included. The corresponding circuit delay under VOS is obtained by determining the delay $T_{a,\,V_{dd}}$ of a full adder with respect to supply voltage V_{dd} via circuit simulation using HSPICE. Table I tabulates $T_{a,\,V_{dd}}$ with respect to V_{dd} for a 0.25-μm CMOS process. If the constraint in (1) is violated, the corresponding output will not be able to settle to its new value but instead retain its previous value, thereby resulting in an output error. The output SNR is calculated by averaging over the entire input data set. The energy dissipation is obtained via the gate-level simulation tool MED [33]. The energy overhead due to AEC includes the computations in the F-block as well as in the WUD block.

TABLE I
FULL-ADDER DELAY (DRIVING ANOTHER FULL ADDER AS FAN-OUT) IN A 0.25 μm CMOS AT DIFFERENT SUPPLY VOLTAGES

V_{dd} (V)	2.5	2.3	2.1	1.9	1.7	1.5	1.3	1.1
$T_{a,V_{dd}}$ (ns)	1.0	1.03	1.06	1.11	1.17	1.25	1.37	1.45

B. Performance Comparison

In these simulations, FDM systems are assumed to have a 22-dB output SNR requirement, i.e., $\mathrm{SNR}_{\mathrm{design}} = 22$ dB. Thus, conventional optimally voltage-scaled filters have been designed to meet this performance specification with minimal complexity. The energy-optimum AEC filters were designed using the methodology described in Section IV to achieve the same algorithmic performance. Table II summarizes the results of this design methodology for different filter bandwidths. Note that the minimum-complexity $H(z)$ has a 0.1π transition bandwidth for different filter bandwidths. Using the optimal Parks–McClellan design method [34], we obtained an $H(z)$ with 32 taps. The optimum VOSF was found to be around 2.0.

In Fig. 6, we compare the energy-performance tradeoff achieved by an energy-optimum AEC-based filter for a bandwidth of 0.7π. Table II shows that $N_c^{\mathbf{opt}} = 8$ for this filter. For the purpose of comparison, we also provide in Fig. 6 the energy-performance tradeoff for this filter with an AEC with $N_c = 4$, 8, and 12 taps, respectively. Note that due to the presence of adjacent-band signals, soft output errors occur frequently as soon as the supply voltage is reduced below $V_{dd\text{-}crit}$. Thus, a sharp SNR drop is observed for the conventional filter. Fig. 6 shows that energy savings of 37, 69, and 64% are achieved at the desired output SNR with $V_{dd\text{-}sub} =$ 1.8 V, 1.3 V, and 1.4 V, by using the four-tap, eight-tap, and 12-tap AEC, respectively. Hence, the eight-tap AEC gives the best energy-performance tradeoff.

Table II also indicates the trends in energy savings achieved by the energy-optimum AEC-based filters at different bandwidths. It can be seen that the hardware complexity of the energy-optimum AEC decreases with the filter bandwidth increasing from 0.3 to 0.8π. This is because wideband filters have a narrow soft-error energy distribution with respect to filter taps. Therefore, fewer filter taps contribute to the performance degradation and this reduces the complexity of AEC algorithm, thereby enabling larger energy reduction. The achievable energy savings ranges from 43.1 to 71.2% (when the WUD block is off) and 22.3 to 65.9% (when the WUD block is on, and thus, the energy savings is offset by the energy dissipation from the WUD block) as the filter bandwidth increases from 0.3 to 0.8π.

We now evaluate the convergence speed of the energy-optimum AEC. Fig. 7 shows two learning curves of energy-optimum AEC for filters with bandwidth of 0.3 and 0.7π, respectively. The step size μ is suitably chosen to obtain an output SNR equal to 22 dB. As indicated in Table II, the settling time N_{set} for an energy-optimum AEC ranges

TABLE II
DESIGN SPECIFICATIONS AND ENERGY SAVINGS FOR ENERGY-OPTIMUM AEC-BASED FILTERS

ω_l	$H(z)$			$H_c(z)$				$\mathcal{E}_{sav}$ %	
	N	B_{input}	B_{coeff}	$N_c^{\mathbf{opt}}$	B_F	B_{WUD}	t_{set} (samples)	WUD OFF	WUD ON
0.3π	32	8b	10b	14	7b	10b	630	43.1	22.3
0.4π	32	8b	10b	12	7b	10b	580	48.4	31.5
0.5π	32	8b	10b	10	7b	10b	510	55.3	44.1
0.6π	32	8b	10b	10	6b	10b	430	58.3	49.5
0.7π	32	8b	10b	8	6b	10b	310	68.7	61.6
0.8π	32	8b	10b	6	6b	10b	220	71.2	65.9

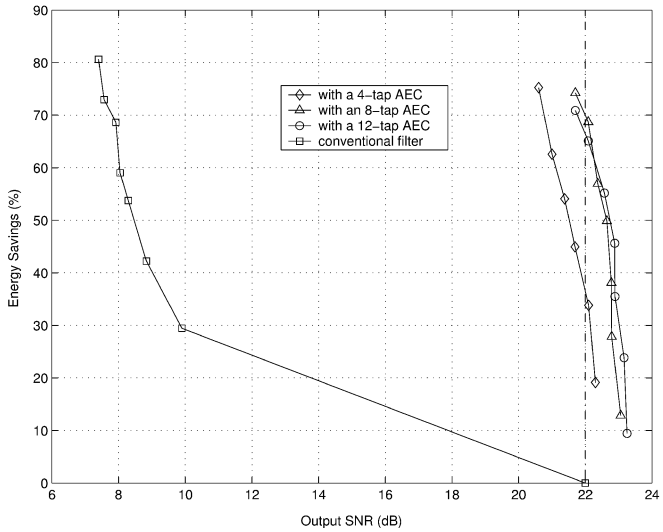

Fig. 6. Performance of the energy-optimum AEC-based filter with 0.7π bandwidth. Each point on the curves corresponds to a different value of VOSF.

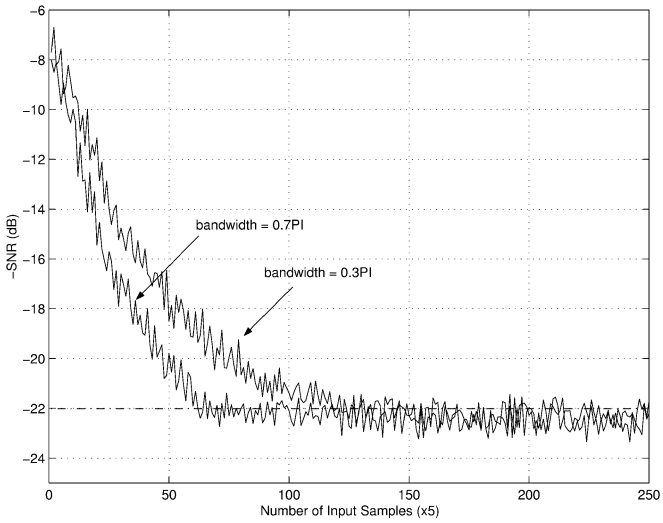

Fig. 7. Convergence speed of the energy-optimum AEC for filters with bandwidth of 0.3π and 0.7π.

from 220∼630 samples, depending on the filter bandwidth. A relatively larger value for N_{set} is expected for filters with a narrower bandwidth as $N_c^{\mathbf{opt}}$ is large for such filters. This is consistent with the observations in (34) and (35).

VI. CONCLUSIONS

In this paper, we have proposed an adaptive error-cancellation (AEC) algorithm for designing low-power soft DSP systems. We apply the AEC technique in the context of a FDM communication system and demonstrate significant energy savings over conventional filters without performance loss. Future work is being directed toward the application of the proposed AEC and combination of AEC and PEC [12] in practical broadband communication systems. Developing ANT techniques for adaptive filters is of great interest, given the presence of such filters as equalizers in many communication systems. Soft DSP provides a new direction for research in the design of energy-efficient DSP algorithms and architectures, whereby DSP algorithms, architectures, and circuit properties are jointly optimized to push the limits of energy reduction.

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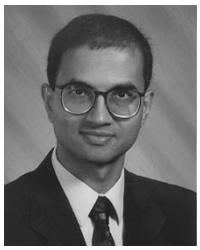

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