VLSI Systems Design of 51.84 Mb/s Transceivers for ATM-LAN and Broadband Access

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***Abstract*— We present the following in this paper: 1) system design issues for the implementation of 51.84 Mb/s ATM-LAN and broadband access transceivers and 2) a pipelined fractionally spaced linear equalizer (FSLE) architecture. Algorithmic concerns such as signal-to-noise ratio (SNR) and bit-error rate (BER) along with VLSI constraints such as power dissipation, area, and speed were addressed in a common framework. The first step is to obtain a thorough understanding of major channel impairments. For the LAN environment, these include near-end crosstalk (NEXT), intersymbol interference (ISI), and impulse noise. The broadband access environment suffers from far-end crosstalk (FEXT), ISI, radio-frequency interference (RFI), impulse noise, and splitter losses. Measured characteristics of the channel are compared with analytical models. These are then employed in the design of the transmitter and receiver algorithms. The carrierless amplitude/phase (CAP) transmission scheme is presented as a practical bandwidth-efficient scheme for these applications. An adaptive FSLE employed in a CAP receiver eliminates ISI, suppresses NEXT (in case of ATM-LAN) and FEXT (in case of broadband access), and provides robustness to timing jitter. However, fractional tap spacing in combination with the high-data rates results in a high sample rate adaptive computation. Fortunately, throughput enhancing techniques such as pipelining can be employed for high-speed and low-power operation. A hardware-efficient pipelined architecture for the adaptive FSLE equalizer is presented. This architecture has been developed via the technique of *relaxed look-ahead*, which maintains the algorithm functionality rather than the input–output mapping. Simulation and experimental results for high-speed digital CAP transceivers for LAN and broadband access are also presented.**

I. Introduction

NUMEROUS high-bit rate digital communication systems are currently being proposed for digital subscriber loops (DSL's). These applications include asymmetric digital subscriber loop [10], [23] (ADSL), high-speed digital subscriber loop (HDSL) [21], [36] very high-speed digital subscriber loop (VDSL) [10], [18] asynchronous transfer mode (ATM) LAN [17], and broadband access [15].

In this paper, we focus on the design of 51.84 Mb/s transceivers for ATM-LAN and broadband access. Initially, ATM networks were envisioned to be a wide-area transport technology for delivering integrated services on public networks. However, the potential benefits of this technology has led to the acceptance of ATM technology in a new generation of LAN's [1]. Unlike existing LAN technologies like Ethernet, token-ring, token-bus, and fiber distributed data interface (FDDI), data in ATM is transferred between systems via point-to-point switched fixed size cells. In case of broadband access, the community network connects the video server and the set-top equipment. There are two community network architectures being considered to deliver broadband services in the local loop, which are based on hybrid fiber-coax (HFC) and fiber-to-the-curb (FTTC) technologies [4]–[6]. Although HFC networks use less fiber and more coaxial cable, the FTTC takes fiber much closer to the customer.

In both ATM-LAN and broadband access applications, the bandlimited nature of the channel and the required performance levels necessitate the use of highly complex digital communications algorithms. Furthermore, the need to reduce costs is driving the industry toward increased levels of integration. The goal is to reliably integrate multiple systems on a single device, thereby improving performance and reducing costs. In addition to the increasing computational complexity, the requirements on a silicon implementation have also become stringent at the same time. There is no doubt that a cost-effective silicon implementation is critical for a successful deployment of any new technology. Therefore, constraints from a VLSI implementation perspective such as power dissipation, area, speed, and reliability also come into the picture.

The contribution of this paper is two fold. We present 1) system level issues in the design of data transceivers for ATM-LAN and broadband access and 2) a hardware-efficient pipelined adaptive fractionally-spaced linear equalizer (FSLE).

System level issues include an understanding of the physical channel and its impairments. For the LAN environment, these impairments include near-end crosstalk (NEXT), intersymbol interference (ISI), and impulse noise. On the other hand, the broadband access environment suffers from far-end crosstalk (FEXT), ISI, radio-frequency interference (RFI), impulse noise, and splitter losses. Measured characteristics of the channel are compared with analytical models, which are then employed in the design of the transmitter and receiver algorithms. The selection of the modulation scheme involves numerous tradeoff's, including the one between performance (noise margin for a given reach) and the hardware complexity of the transceiver. The carrierless amplitude/phase (CAP) [17] modulation scheme is presented as a practical bandwidth-efficient scheme for these applications. An adaptive FSLE, which is employed in a CAP receiver, eliminates ISI, sup-

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presses NEXT (in case of ATM-LAN), and provides robustness to timing jitter.

Another scheme, which is a standard for ADSL and a candidate for VDSL, is the discrete multitone (DMT) [11] modulation technique. Unlike, CAP, the DMT technique employs multiple carriers, where each is assigned a different number of bits per symbol. It, thus, is able to exploit the frequency variations in the channel signal-to-noise ratio (SNR) and approximate Shannon's [35] water-filling argument. On the other hand, the peak-to-average ratio of a DMT signal is higher than that of a CAP signal, and hence, the A/D and D/A converters for DMT would require more precision.

The traditional approach to realizing a concept in silicon consists of two major steps: 1) algorithm design and 2) VLSI implementation. The major concerns in the algorithm design phase consisted of meeting the algorithmic performance requirements such as SNR and bit-error rate (BER). Constraints from the VLSI domain such as area, power dissipation, and throughput were addressed only after the parameters (and sometimes the structure) of the algorithm were well defined. It is now well recognized that such an approach results in a long transition time from algorithm design to a silicon prototype. Therefore, there is a strong need to develop *a unified design paradigm*, whereby the design of signal processing and communications algorithms and VLSI can addressed in a cohesive manner. Design methodologies based on such a paradigm will be necessary to realize complex VLSI systems for signal processing and communications.

One way to integrate algorithmic concerns (such as SNR) and implementation issues such as area, power dissipation, and throughput is to employ *algorithm transformation techniques* [27] such as pipelining [25], [28], [31], parallel processing [28], unfolding [16], folding [29], retiming [22], etc. Employed traditionally for high-speed applications, pipelined algorithms have found use in low-power applications as well. Furthermore, by combining pipelining with folding, it is possible to trade off area with speed. Thus, it is clear that all the three major parameters of interest in a VLSI implementation, i.e.,

- speed;
- power;
- area;

can be optimized by the design of pipelined algorithms.

Adaptive signal processing is commonly employed in DSL receivers due to the time-varying nature of the channel and channel impairments. Usually, the adaptive component in the receiver functionality dominates the overall complexity. Therefore, it is desirable to have inherently pipelined adaptive filters, which not only enable us to achieve the required SNR but also allow us to optimize area, power, and speed. Pipelined adaptive digital filters have been proposed recently [31] that are hardware efficient and have similar performance as the unpipelined (or serial) filters. These filters have been developed via the technique of *relaxed look-ahead*. This technique is an approximation to the *look-ahead* transformation [28], which had been proposed for fixed coefficient filters. The relaxed look-ahead technique has been successfully employed to pipeline numerous adaptive algorithms such as the adaptive least mean-squared (LMS) algorithm [32] and the adaptive differential pulse-code modulation (ADPCM) coder [32]. Furthermore, silicon implementations of both the look-ahead technique and the relaxed look-ahead technique have been done. In both ATM-LAN and broadband access environments, an adaptive FSLE is employed at the receiver. The FSLE eliminates ISI, suppresses NEXT (in case of ATM-LAN), and provides robustness to timing jitter. In this paper, we will present a pipelined adaptive FSLE architecture employing relaxed look-ahead and study its performance as a function of speedup.

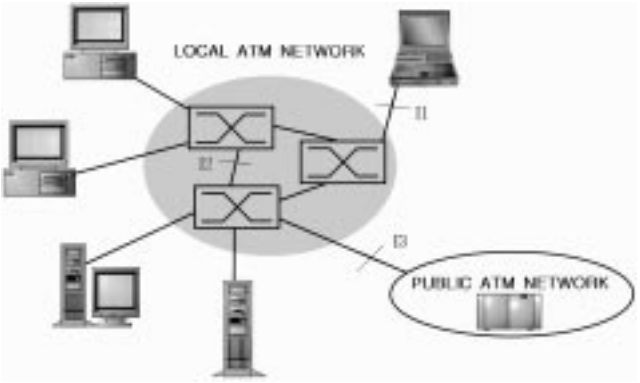


Fig. 1. ATM-LAN network architecture using twisted pair.

The organization of this paper is follows. The characteristics of the LAN environment, the CAP modulation scheme, and the broadband access environment are presented in Section II. In Section III, we illustrate the application of relaxed look-ahead to develop an hardware-efficient pipelined FSLE architecture. Simulation and experimental results for CAP transceivers operating at 51.84 Mb/s for both ATM-LAN and broadband access are presented in Section IV.

II. The Channel

A proper understanding of the physical environment is essential in order to design communications systems that meet the specified performance requirements. In this section, we will describe the physical environment and the CAP modulation scheme for ATM-LAN and broadband access. First, we describe the LAN and then the broadband access environments. Finally, we will present the CAP [17] modulation scheme.

A. The LAN Environment

In Fig. 1, we show a vendor's view of an ATM-based LAN. The environment of interest for the unshielded twisted-pair category three (UTP-3) user network interface (UNI) consists of the "I1" and "I2" interfaces (see Fig. 1). The wiring distribution system runs either from the closet to the desktop or between hubs in the closets. It has been shown elsewhere that the wiring used in these situations consists mostly of either TIA/EIA-568 UTP-3 four-pair cable or the DIW 10 Base-T 25-pair bundle. We proposed the 51.84 Mb/s 16-CAP and the 155 Mb/s 64-CAP line codes to the PHY subworking group of the ATM Forum as candidates for the ATM LAN standard over UTP-3. The 16-CAP modulation scheme became the

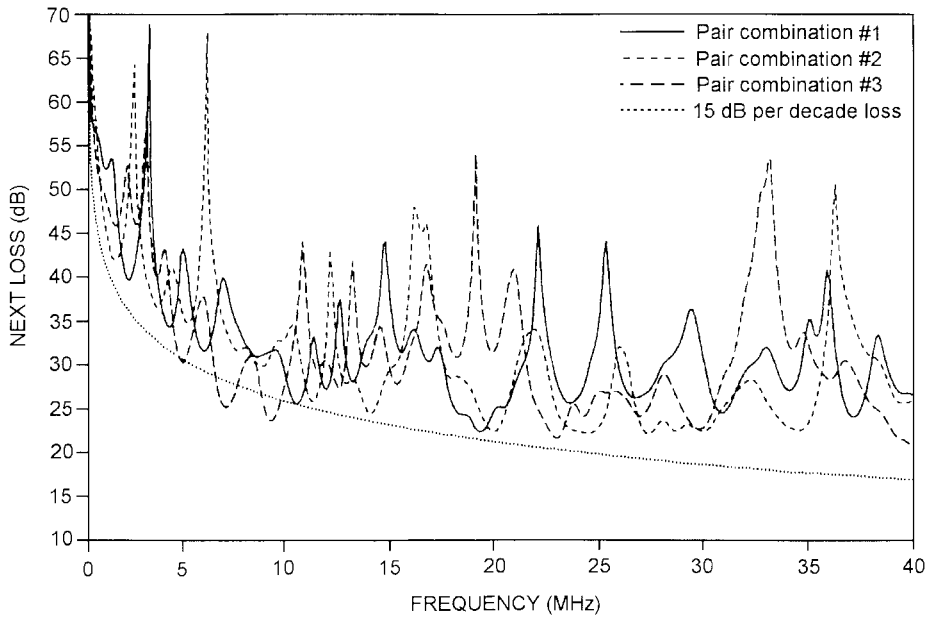


Fig. 2. Measured NEXT loss between pairs of category 3 cable.

standard for ATM-LAN over UTP-3 at 51.84 Mb/s [2], [17] and broadband access [4] over copper wiring. Furthermore, 64-CAP was recently chosen as the standard for ATM-LAN [3] over UTP-3 at 155.52 Mb/s.

In the LAN environment, the two major causes of performance degradation for transceivers operating over UTP wiring are propagation loss and crosstalk generated between adjacent wire pairs. The local transmitter produces a signal with amplitude V, which propagates on a certain wire pair j and generates spurious signals V_N (at the near-end) and V_x (at the far-end) on pair i. The signal V_N appears at the end of the cable where the disturbing source V is located and is called NEXT. The signal V_x appears at the other end of the cable and is called FEXT. In the LAN environment, NEXT is usually much more severe than FEXT, and therefore, we will focus on the former. We will see in Section II-B that the reverse is true for the broadband access application.

When data signals are sent in opposite directions on two different pairs, the communication link can be modeled as a transmitter sending a signal through a loop with transfer function $H(d, f)$. At the output of the loop, an interfering NEXT signal is added to the received signal, and the combination of disturbed and interfering signals is then processed by the receiver. The interfering NEXT is sometimes called self-NEXT in the case where the disturbed and interfering signals are similar (same transmission scheme). In this section, we will discuss the channel and NEXT characteristics for UTP-3 cable.

The propagation loss assumed is the worst-case loss given in the TIA/EIA-568 draft standard for category 3 cable [7]. This loss can be approximated by

$$L_P(f) = 2.320\sqrt{(f)} + 0.238f, \tag{2.1}$$

where the propagation loss $L_P(f)$ is expressed in decibels per kilofoot, and the frequency f is expressed in megahertz. The phase characteristics of the loop's transfer function can be computed from $\sqrt{LC}$, where R, L, G, and C are the primary constants of a cable. These are available in published literature, including [36].

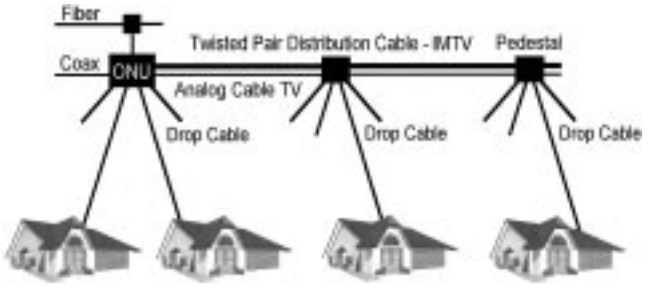


Fig. 3. FTTC network architecture using twisted-pair distribution cable and coaxial drop cable.

The worst-case NEXT loss model for a single interferer is also given in the TIA/EIA draft standard. The squared magnitude of the NEXT transfer function corresponding to this loss can be expressed as

$$L_N(f) = 43 - 15\log f \tag{2.2}$$

where the frequency f is in megahertz. The wavy curves in Fig. 2 give the measured pair-to-pair NEXT loss characteristics for three different combinations of twisted pairs in 100-m category 3 cables. Notice that the minima and maxima usually occur at different frequencies for the three pair combinations. Notice also that the NEXT loss corresponding to the minima decreases with increasing frequency and tends to follow the smooth dotted curve of (2.2), which is also referred to as the 15-dB per decade model.

B. The Broadband Access Environment

In an FTTC network architecture shown in Fig. 3, the optical fiber goes to a curbside pedestal, which serves a small number of homes [15]. At the pedestal, the optical signal is converted into an electrical signal and then demultiplexed for

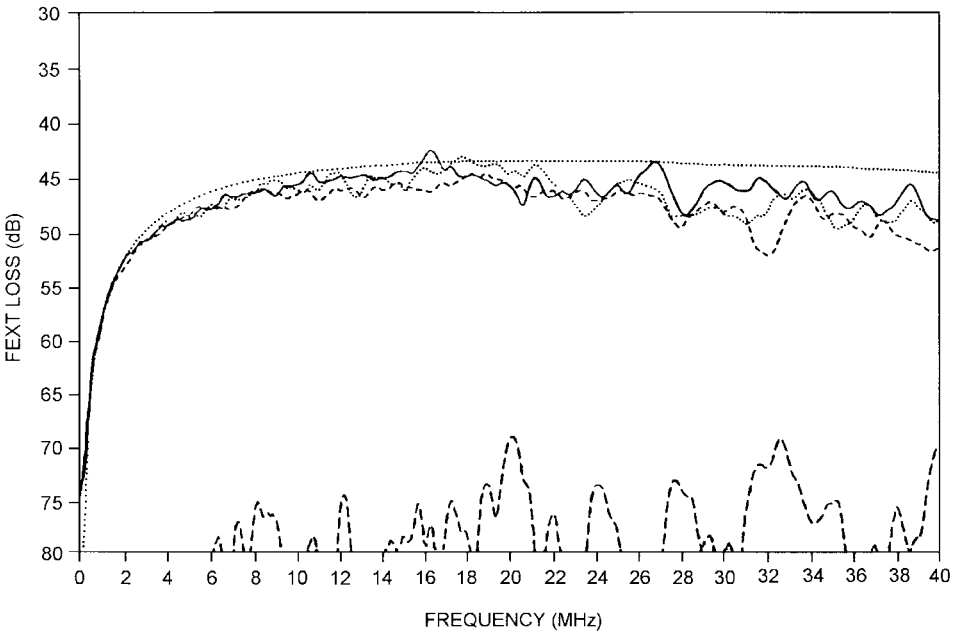


Fig. 4. Measured worst-case FEXT loss between pairs of 600 ft of UTP cable.

delivery to individual homes on copper wiring. These functions are performed in an optical network unit (ONU). The ONU also performs the multiplexing and signal conversion functions required in the opposite direction, i.e., from the homes to the network. The FTTC system considered here makes usage of existing telephone drop wiring or coaxial cable to provide local distribution of interactive multimedia TV (IMTV) to the home. The standard 51.84 Mb/s 16-CAP transceiver becomes a key transport technology for this broadband interactive video service in the FTTC system [4]. In this subsection, we will describe various channel impairments for the broadband access environments. In particular, in Section IV, we will present computer simulation and experimental results of the 16-CAP prototype used for broadband access in the FTTC network architecture.

In the IMTV system considered here, the downstream channel (from the ONU to the home) operates at the STS-1 data rate of 51.84 Mb/s, and the upstream channel (from the home to the ONU) operates at a data rate of 1.62 Mb/s. Both channels carry ATM cells, and the downstream channel uses SONET framing. The transmission scheme used for the downstream channel is a modified version of the 16-CAP encoding scheme that has been standardized by the Technical Committee of the ATM Forum for the ATM LAN physical layer interface at 51.84 Mb/s over UTP wiring [17]. The transmission scheme used for the upstream channel is quadrature phase-shift keying (QPSK).

When the IMTV signals propagate on the UTP distribution cable, they interfere with each other by generating FEXT. The downstream 16-CAP signals interfere with each other, and so do the upstream QPSK signals. However, there is minimal interaction between the downstream and upstream signals because the 16-CAP and QPSK signals use different frequency bands. This is the reason why NEXT is not as significant an issue in broadband applications as FEXT.

In this subsection, we briefly discuss channel and FEXT characteristics of a 600-ft BKMA cable, which is used for UTP distribution cable in Fig. 3. The propagation loss characteristics of a BKMA cable are similar to that of a category 5 cable. The worst-case propagation loss for category 5 cable is specified in the TIA/EIA-568A Standard [7], which can also be expressed as

$$L_P(f) = 3.597\sqrt{(}f) + 0.043f + 0.0914/\sqrt{(}f) \qquad (2.3)$$

where the propagation loss $L_P(f)$ is expressed in decibels, and the frequency f is expressed in megahertz.

In Fig. 4, the wavy curves give the measured pair-to-pair FEXT loss characteristics for the 600-ft UTP cable. The solid line in Fig. 4 represents the worst-case FEXT characteristic amongst the 600 different combinations of twisted pairs in the cable. In case of multiple FEXT interferers, the FEXT power-sum loss can be written as

$$|H(f)_{\mathrm{FEXT}}|^2 \triangleq \frac{V_x^2}{V_t^2} = \Psi f^2 d |H(d,f)|^2 \qquad (2.4a)$$

$$V_x^2 = \sum_{i=1}^{N} V_{xi}^2 \qquad (2.4b)$$

where

$H(d,f)$	transfer function of a loop;
d	length of the coupling path;
N	number of interferers;
V_t	amplitude of the transmit signal;
V_{xi}	amplitude of the ith FEXT signal [36].

Assuming that frequencies are expressed in kilohertz and loop length in kilofeet, the coupling constant Ψ for 1% equal level 49 interferers, is reported to be 10^{-10}. The dotted line in Fig. 4 shows the worst-case FEXT loss model for a single interferer in a 600-ft UTP cable.

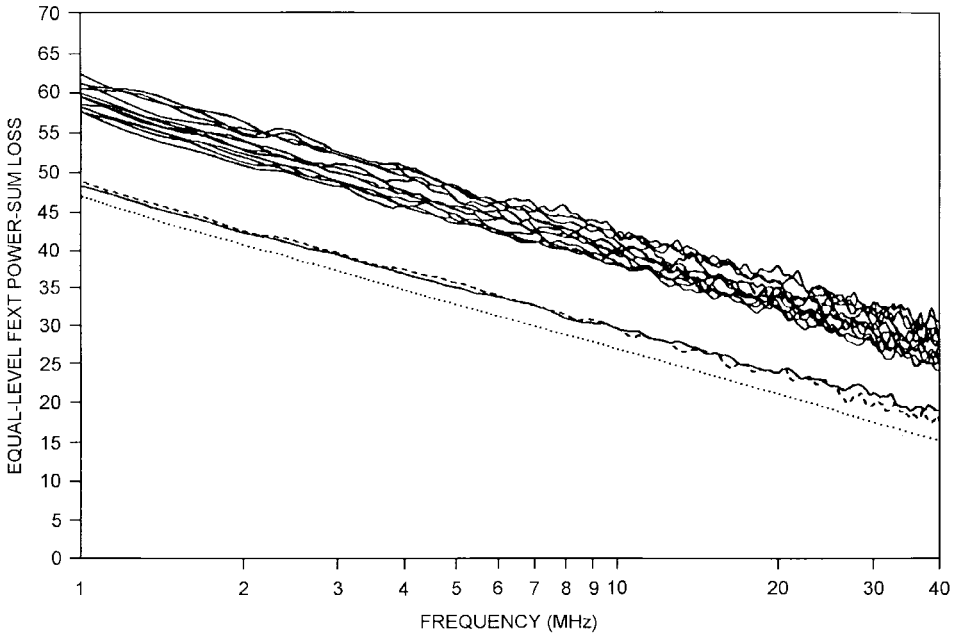


Fig. 5. Equal-level FEXT power-sum loss of eleven interferers.

Another quantity of interest is the ratio V_r^2/V_x^2, where V_r is the received signal. Employing (2.4), this ratio [which is also called equal-level FEXT (EL-FEXT) loss] can be written as

$$\text{EL-FEXT} = \frac{V_s^2}{V_x^2} = \frac{K}{\Psi f^2 d} \qquad K = (49/N)^{0.6}. \tag{2.5}$$

Fig. 5 shows the EL-FEXT power-sum loss of 11 interferers, which is the SNR at the input of receiver when the transmit signal has traversed 600-ft UTP cable with 11 FEXT interferers. It is seen in Fig. 5 that the dotted line representing (2.5) can be considered to be a lower bound and decreases by 20 dB per decade with frequency. Comparing the FEXT loss model with the measured FEXT power-sum loss, we see that the worst-case FEXT model of 11 interferers is about 3 dB worse than the measured power-sum loss. The 12 curves at the top of Fig. 5 show the measured EL-FEXT power-sum loss of 11 interferers when 12 best pairs are selected among 25 pairs UTP cable. It is seen in Fig. 5 that a reduction in FEXT power by at least 8 dB is possible by pair selection.

There are also several other factors that impair channel function, including splitters, terminated and open-ended stubs, light dimmers, and narrowband interferences [15]. Splitters used in the in-house coaxial cabling system introduce a severe amount of propagation loss and deep notches in the channel transfer function at frequencies below 5 MHz. An open-ended stub connected to an output port of a splitter introduces notches in the channel transfer function corresponding to the other output ports of the splitter. RF interference is generated by AM radio and amateur radio is also one of major impairments for the downstream and upstream channel signals. In this case, a decision feedback equalizer (DFE) can be employed at the receiver. Light dimmers generate impulse noise that has significant energy up to 1 or 2 MHz. Reed–Solomon codes with convolutional interleaving are being incorporated to alleviate the effect of this burst noise on the system performance [4].

C. CAP Transceiver Structure

In this subsection, we describe the carrierless amplitude modulation/phase modulation (CAP) transmission scheme and the CAP transceiver structure. The CAP is a bandwidth-efficient two-dimensional (2-D) passband transmission scheme, which is closely related to the more familiar quadrature amplitude modulation (QAM).

1) The CAP Transmitter: The block diagram of a digital CAP transmitter is shown in Fig. 6(a). The bit stream to be transmitted is first passed through a scrambler (which is not shown in the figure) in order to randomize the data. The bit-clock, which is employed to synchronize the scrambler, equals R the desired bit rate. For the applications of interest in this paper, $R = 51.84$ Mb/s, and therefore, the bit clock is equal to 51.84 MHz. The scrambler is usually implemented as as a linear feedback shift register and, hence, can be operated at these speeds quite easily.

The scrambled bits are then fed into an encoder, which maps blocks of m bits into one of $k = 2^m$ different complex symbols $a(n) = a_r(n) + ja_i(n)$. A CAP line code that uses k different complex symbols is called a k-CAP line code. In this case, the symbol rate $1/T$ given by

$$\frac{1}{T} = \frac{R}{m} = \frac{R}{\log_2(k)} \tag{2.6}$$

where R is the bit rate, and m is the number of bits per symbol. The encoder block would accept blocks of m bits and generate symbols $a_r(n)$ and $a_i(n)$ per symbol period. Given that $R = 51.84$ Mb/s and $m = 4$, then from (2.6), we have the symbol rate $1/T = 12.96$ MBd. Therefore, the symbol clock employed in the encoder block would have a frequency of 12.96 MHz. The encoder can be implemented as a table

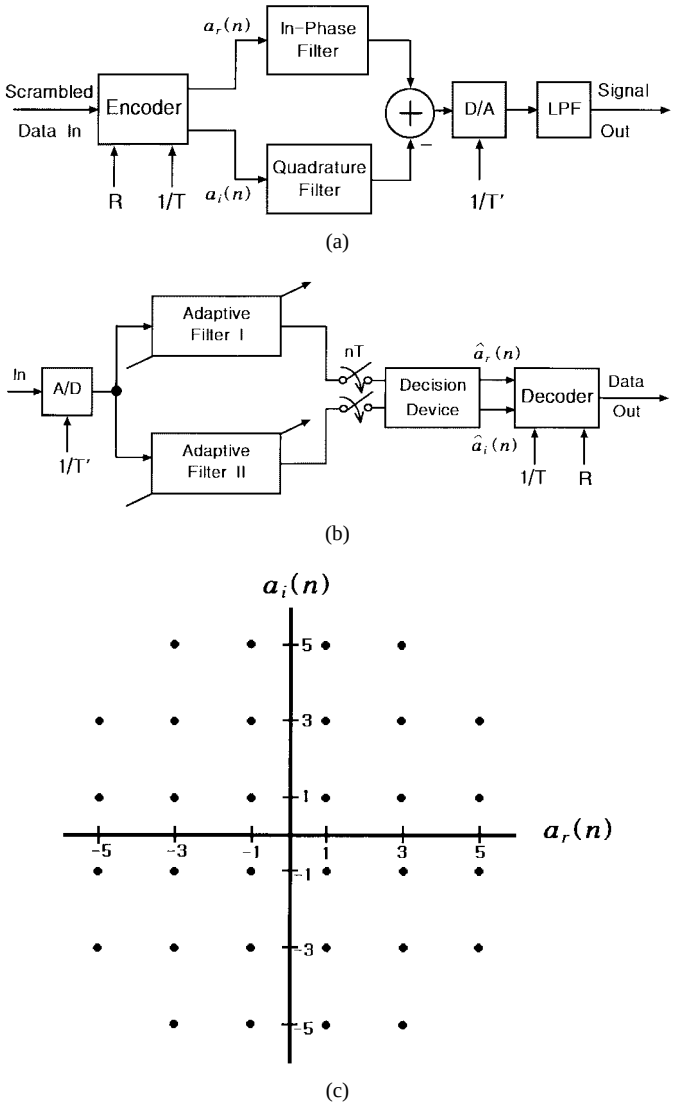


Fig. 6. CAP system. (a) Transmitter. (b) Receiver. (c) 32-CAP signal constellation.

look up. The 2-D display of the discrete values assumed by the symbols $a_r(n)$ and $a_i(n)$ is called a signal constellation, an example of which is shown in Fig. 6(c).

After the encoder, the symbols $a_r(n)$ and $a_i(n)$ are fed to digital shaping filters. The outputs of the filters are subtracted, and the result is passed through a digital-to-analog (D/A) converter, which is followed by an interpolating lowpass filter (LPF). The signal at the output of the CAP transmitter in Fig. 6(a) can be written as

$$s(t) = \sum_{n=-\infty}^{\infty} [a_r(n)p(t-nT) - a_i(n)\tilde{p}(t-nT)] \quad (2.7)$$

where T is the symbol period; $a_r(n)$ and $a_i(n)$ are discrete multilevel symbols, which are sent in symbol period nT; and $p(t)$ and $\tilde{p}(t)$ are the impulse responses of in-phase and quadrature passband shaping filters, respectively.

The passband pulses $p(t)$ and $\tilde{p}(t)$ in (2.7) can be designed in as

$$p(t) \triangleq g(t)\cos(2\pi f_c t) \quad \tilde{p}(t) \triangleq g(t)\sin(2\pi f_c t) \quad (2.8)$$

where $g(t)$ is a baseband pulse, and f_c is called the *center frequency* and is larger than the largest frequency component in $g(t)$. The two impulse responses in (2.8) form a Hilbert pair, i.e., their Fourier transforms have the same amplitude characteristics, whereas their phase characteristics differ by 90°

While the bit rate R and the choice of the signal constellation determine the symbol rate $1/T$ [see (2.6)], the transmit spectrum is generated by the shaping filters. It is well known [14] that the bandwidth of a passband spectrum cannot be smaller than the symbol rate $1/T$. In practice, the transmit bandwidth is made greater than $1/T$ by a fraction α. In that case, the upper and lower edges of the transmit spectrum are given by

$$f_{\text{upper}} = f_c + \frac{(1+\alpha)}{2T} \quad (2.9a)$$

$$f_{\text{lower}} = f_c - \frac{(1+\alpha)}{2T} \quad (2.9b)$$

where

f_c center frequency;
f_{upper} upper edge;
f_{lower} lower edge

of the transmit spectrum. The fraction α is also referred to as the *excess bandwidth*. For reasons to be described later [see Section IV-A], the excess bandwidth was 100% $(\alpha = 1.0)$ for ATM-LAN and 50% $(\alpha = 0.5)$ for broadband access.

The digital shaping filters and the D/A operate at a sampling rate $1/T_s = M/T$, where M is a suitably chosen integer such that the sample rate is greater than $2f_{\text{upper}}$ [see (2.9a)]. In addition to this requirement, the sample rate is also chosen to be an integral multiple of the symbol rate in order to ease the requirements on the clock generation circuitry. Depending on the symbol rate and the integer M, the sample rates can be quite high. For example, in the 51.84 Mb/s ATM-LAN application, the symbol rate is 12.96 MBd and $M = 4$. This results in a sample rate of 51.84 Msamples/s. Usually, the shaping filters are implemented as finite-impulse response (FIR) filters, and hence, operating at high sample rates is not difficult. Nevertheless, some degree of pipelining may be required. The transmitter design requires a tradeoff that encompasses algorithmic and VLSI domains. In particular, this tradeoff balances the rolloff in transmit spectrum band edges and the silicon power dissipation. It can be seen that most of the signal processing at the transmitter (including transmit shaping) is done in the digital domain.

2) The CAP Receiver: The structure of a digital CAP receiver is shown in Fig. 6(b). It consists of an analog-to-digital (A/D) converter followed by a parallel arrangement of two adaptive digital filters. The A/D and the digital filters operate at a sampling rate $1/T_s = M/T$, which is typically the same as the sampling rate used at the transmitter. The parallel arrangement of adaptive filters in Fig. 6(b) will be called a T/M (FSLE) [14].

The received signal consists of the data signal (desired signal), the ISI, and the NEXT/FEXT signal. The performance of a receiver is a function of the input SNR SNR_i, which is

the given by

$$\text{SNR}_i = \frac{\sigma_{ds}^2 + \sigma_{\text{isi}}^2}{\sigma_{\text{noise}}^2} \tag{2.10}$$

where

σ_{ds}^2 data signal power;
σ_{isi}^2 intersymbol interference (ISI) power;
σ_{noise}^2 noise power.

Here, $\sigma_{\text{noise}}^2 = \sigma_{\text{NEXT}}^2$ in the case of ATM-LAN, and $\sigma_{\text{noise}}^2 = \sigma_{\text{FEXT}}^2$ in the case of broadband access. Similarly, the SNR at the output of the equalizer SNR_o is defined as

$$\text{SNR}_o = \frac{\sigma_{ds}^2}{\sigma_{r,\text{noise}}^2 + \sigma_{r,\text{isi}^2}} \tag{2.11}$$

where $\sigma_{r,\text{noise}}^2$ is the residual noise (NEXT/FEXT), and $\sigma_{r,\text{isi}}^2$ is the residual ISI at the equalizer output. Typically, at the input to the receiver (for both ATM-LAN and broadband access), the data signal power σ_{ds}^2 is only 6 dB above the ISI signal power σ_{isi}^2, and hence, ISI is the dominant impairment. Therefore, the equalizer first reduces ISI before it can suppress the NEXT/FEXT signal. Thus, the function of the FSLE is to perform *NEXT suppression* (for ATM-LAN), *FEXT suppression* (for broadband access), and ISI removal (for both).

NEXT suppression greatly reduces the power of the interferer at the sampling instants of the slicer without any need to access the transmitter generating the interferer (this is an alternative approach and is referred to as NEXT cancellation [19]). Instead, the interfering NEXT signal at the receiver is equalized in such a way that it passes through zero at all the sampling instants of the slicer. It has been shown that NEXT suppression is feasible only if the transceiver uses a large excess bandwidth. More specifically, one cyclostationary NEXT interferer can be suppressed perfectly if the CAP transmitter uses an excess bandwidth of at least 100% [13], [17], [30].

Employing an FSLE in the receiver results not only in allowing us to suppress NEXT and remove ISI but also to provide immunity to sampling jitter caused by the timing recovery circuit. However, from a VLSI perspective, implementing a high sample rate adaptive filter is a difficult task. As mentioned before, we can employ pipelining techniques such as relaxed look ahead to develop hardware-efficient high-speed adaptive FSLE architectures. Nevertheless, it is important to incorporate the pipeline delays in the algorithmic simulations in order to verify that there is no significant degradation in performance. In Section III, we will present a relaxed look-ahead pipelined FSLE architecture, which can be employed in these applications.

The two outputs of the FSLE are sampled at the symbol rate $1/T$, and the results are fed to a decision device followed by a decoder, which maps the symbols into bits. The output of the decoder is then passed to a descrambler. It must be noted that the decoder and the descrambler perform the inverse operation of the encoder and the scrambler, respectively. Thus, we see that most of the signal processing in a CAP transceiver is done in the digital domain. This minimality of analog processing permits a robust VLSI implementation. Furthermore, it is easy to operate a CAP transceiver at different bit rates. This can be achieved by altering the signal constellation generated by the encoder without changing the analog front end. Refer to [9] for more details on the design of CAP receivers.

III. The Pipelined Adaptive FSLE Architecture

As described in Section II, the LAN environment has NEXT as the predominant channel impairment, whereas FEXT is present in the broadband access environment. In either case, the characteristics of these interferers is not known *a priori*. Therefore, adaptive techniques have to be incorporated in the receiver design. In both applications, the upper edge of the transmit spectrum is around 26–30 MHz. Assuming that digital shaping and passband equalization is to be employed, sample rates from 51.84 Msamples/s to 60 Msamples/s become necessary. Designing adaptive FSLE's with sufficient number of taps to meet a BER requirement of 10^{-10} at these sample rates is a challenging problem. This problem can be solved via the technique of pipelining, which will be described in the next subsection.

Power dissipation can become a concern, due to the high sample rates and the complexity of the adaptive algorithms. This is especially true in the case of the broadband access applications, where the transmitters are enclosed in an ONU box situated on the curb outside the premises. Extreme temperatures during summer in combination with power dissipation can push the devices beyond their normal operating ranges. Fortunately, the technique of pipelining can also be employed to reduce power dissipation. This can be done by trading off speed with power via scaling of the power supply [8]. This tradeoff can be done either by reducing the power supply without changing the technology (this could impact the noise margins adversely) or by fabricating the design itself in a low-voltage technology. The latter approach was taken in the IMTV chip sets [12].

In this section, we first describe the technique of relaxed look-ahead pipelining for adaptive digital filters [31] and then employ it to design pipelined FSLE architecture.

A. Relaxed Look-Ahead Pipelining

The relaxed look-ahead technique was proposed in [31] as a hardware-efficient pipelining technique for adaptive filters. This technique is obtained by approximating the algorithms obtained via the look-ahead technique [28].

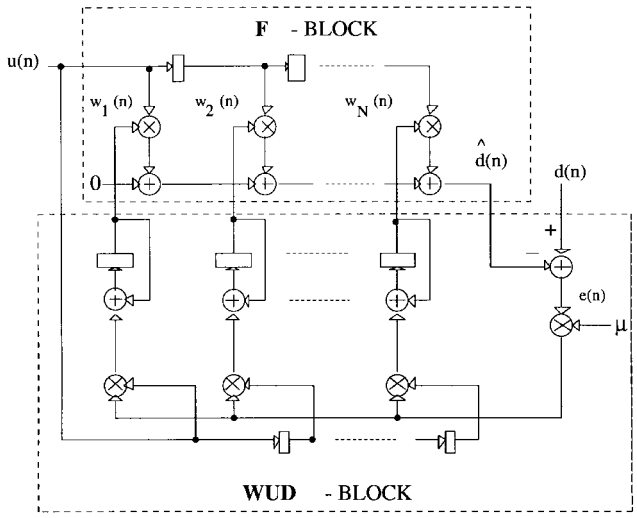
Consider an N-tap serial LMS (SLMS) filter described by

$$e(n) = d(n) - \boldsymbol{W}^T(n-1)\boldsymbol{X}(n) \tag{3.1a}$$

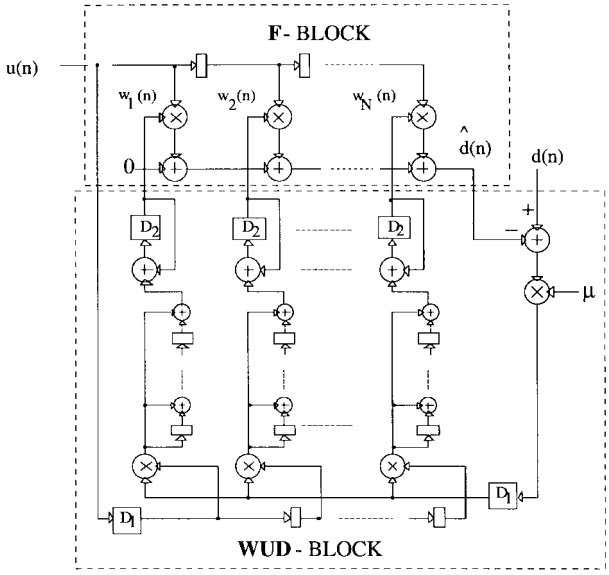
$$\boldsymbol{W}(n) = \boldsymbol{W}(n-1) + \mu e(n)\boldsymbol{X}(n) \tag{3.1b}$$

where $\boldsymbol{W}(n) = [w_0(n), w_1(n), \cdots, w_{N-1}(n)]^T$ is the weight vector, $\boldsymbol{X}(n) = [x(n), x(n-1), \cdots, x(n-N+1)]^T$ is the input vector, $e(n)$ is the adaptation error, μ is the step-size, and $d(n)$ is the desired signal. A direct-mapped architecture for the serial LMS algorithm is shown in Fig. 7(a). Note that the critical path for the serial LMS is given by

$$T_{c,\text{SLMS}} = 2T_m + (N+1)T_a \tag{3.2}$$



(a)



(b)

Fig. 7. LMS architecture. (a) Serial. (b) Relaxed look-ahead pipelined.

where

N equal to the number of taps in the F-block;
T_m computation time of multiplie;
T_a computation time of an adder.

For the LAN and broadband access applications of interest in this paper, the critical path computation time would prove to be too slow to meet the sample rate requirements. Therefore, pipelining of the SLMS is a critical requirement.

While the derivation of the pipelined LMS algorithm is given in [32], we will present only the final result here. The pipelined LMS algorithm is given by (3.3)

$$e(n) = d(n) - \boldsymbol{W}^T(n - D_2)\boldsymbol{X}(n) \tag{3.3a}$$

$$\boldsymbol{W}(n) = \boldsymbol{W}(n - D_2) + \mu \sum_{i=0}^{LA-1} e(n - D_1 - i)\boldsymbol{X}(n - D_1 - i) \tag{3.3b}$$

where D_1 $(D_1 \geq 0)$ and D_2 $(D_2 \geq 1)$ are algorithmic pipelining delays, and LA $(1 \leq LA \leq D_2)$ is referred to as the look-ahead factor. It suffices to mention that the D_1 and D_2 delays have been introduced via the *delay* and *sum* relaxations, respectively. Note that the substitution of $D_1 = 0, D_2 = 1$, and $LA = 1$ in (3.3) results in the serial LMS [see (3.1)]. Furthermore, $D_2 = 1$ and $LA = 1$ in (3.3) gives us the "delayed LMS" [24] algorithm. Convergence analysis of the pipelined LMS algorithm in [32] indicates that the upper bound on the step-size μ is reduced, and the misadjustment $\mathcal{M}$ degrades slightly as the level of pipelining D_1 and D_2 increase. Refer to [32] for details regarding the convergence analysis of the pipelined LMS algorithm.

The architecture corresponding to the pipelined LMS algorithm is shown in Fig. 7(b), where D_1 and D_2 delays can be employed to pipeline all the hardware operators in an actual implementation. Next, we employ the pipelined LMS architecture to develop the pipelined adaptive FSLE architecture.

B. Pipelined FSLE

From Fig. 6(b), we see that the CAP receiver requires two adaptive FSLE's referred to as the in-phase FSLE (IFSLE) and the quadrature-phase FSLE (QFSLE). While the input is sampled at a frequency f_s, the output of the FSLE is computed at the baud-rate $1/T$. For ease of implementation, the sampling frequency f_s is usually made a multiple of the baud-rate $1/T$, i.e., $f_s = M/T$. Clearly, we can save substantial hardware if the FSLE is implemented as an FIR filter. This due to the fact that the outputs that are to be discarded by the baud-rate sampler need not be computed at all. Pipelining of an FSLE can then be easily accomplished by placing latches at the feedforward outsets [20] of the algorithm.

As mentioned in the previous subsection, adaptive FSLE's (AFSLE's) are needed in the applications of interest in this paper. As shown in Fig. 6(b), these two FSLE's are adapted independently employing the in-phase error $e_R(n)$ (for IFSLE) and the quadrature-phase error $e_I(n)$ (for QFSLE). The serial AFSLE (SAFSLE) employs the leaky LMS algorithm for adapting the coefficients as

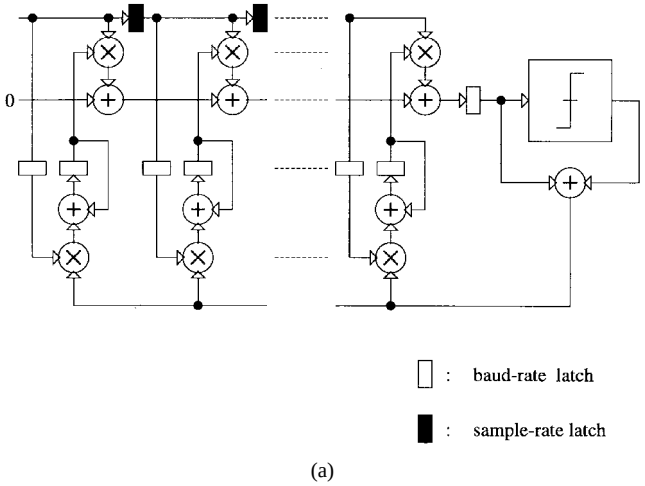
$$\begin{aligned} e_R(nT) &= Q[y_R(nT)] - y_R(nT) \\ &= Q[y_R(nT)] - \boldsymbol{W}_R^T((n-1)T)\boldsymbol{X}(nT) \end{aligned} \tag{3.4a}$$

$$\begin{aligned} \boldsymbol{W}_R(nT) &= (1-\gamma)\boldsymbol{W}_R((n-1)T) \\ &\quad + \mu e_R(nT)\boldsymbol{X}(nT) \end{aligned} \tag{3.4b}$$

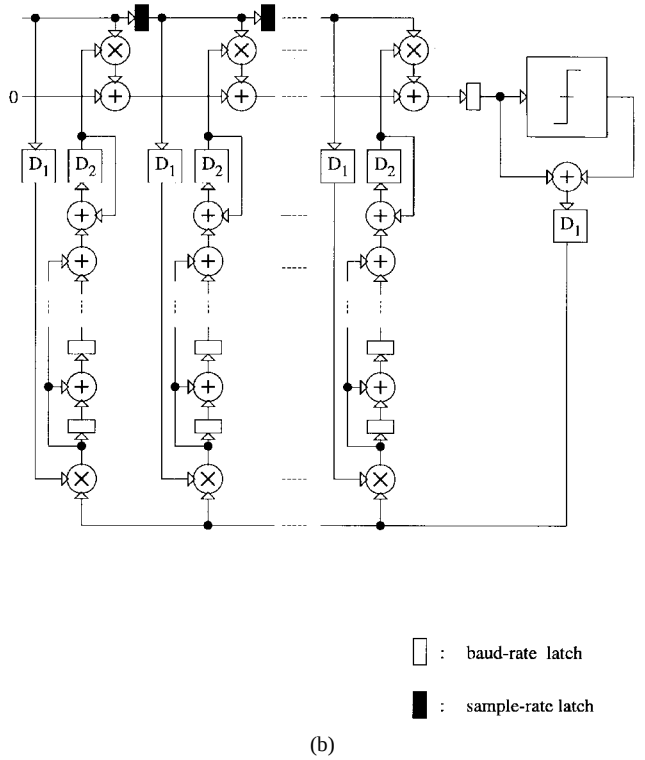
$$\begin{aligned} e_I(nT) &= Q[y_I(nT)] - y_I(nT) \\ &= Q[y_I(nT)] - \boldsymbol{W}_I^T((n-1)T)\boldsymbol{X}(nT) \end{aligned} \tag{3.4c}$$

$$\begin{aligned} \boldsymbol{W}_I(nT) &= (1-\gamma)\boldsymbol{W}_I((n-1)T) \\ &\quad + \mu e_I(nT)\boldsymbol{X}(nT) \end{aligned} \tag{3.4d}$$

where $\boldsymbol{W}_R(nT) = [w_{0,R}(nT), w_{1,R}(nT), \cdots, w_{N-1,R}(nT)]^T$ is the vector of in-phase coefficients, $\boldsymbol{W}_I = [w_{0,I}(nT), w_{1,I}(nT), \cdots, w_{N-1,I}(nT)]^T$ is the vector of quadrature-phase coefficients, $\boldsymbol{X} = [x(nT), x(nT - T_s), \cdots, x(nT - (N-1)T_s)]^T$ is the vector of input samples, μ is the step size, γ is the tap-leakage factor, and $Q[.]$ is the output of the decision device. Note that the output of the decision device



(a)



(b)

Fig. 8. AFSLE. (a) Serial and (b) pipelined algorithms.

is equivalent to the desired signal $d(n)$ in [3.1(a)] under the assumption that the decision errors are very rare. In order to simplify the implementation, the tap-leakage factor γ and the step-size μ can be made equal to appropriate powers of 2.

We can see from (3.4) that apart from the tap-leakage and the fractional input spacing, the SAFSLE equations are identical to that of the LMS algorithm described by (3.1). An architectural representation of (3.4) is shown in Fig. 8(a). Note that in Fig. 8(a), we have not yet exploited the fact that the output of the F-block is being sampled at baud rate, which is $1/M$ times that of the sample rate f_s. This is done in order to facilitate the application of relaxed look-ahead, which applies at the algorithmic level. It needs to be mentioned that there are numerous ways to fold the algorithmic operations in Fig. 8(a) onto a given set of hardware units. By inspection of (3.1) and (3.4), we obtain equations that describe the pipelined AFSLE

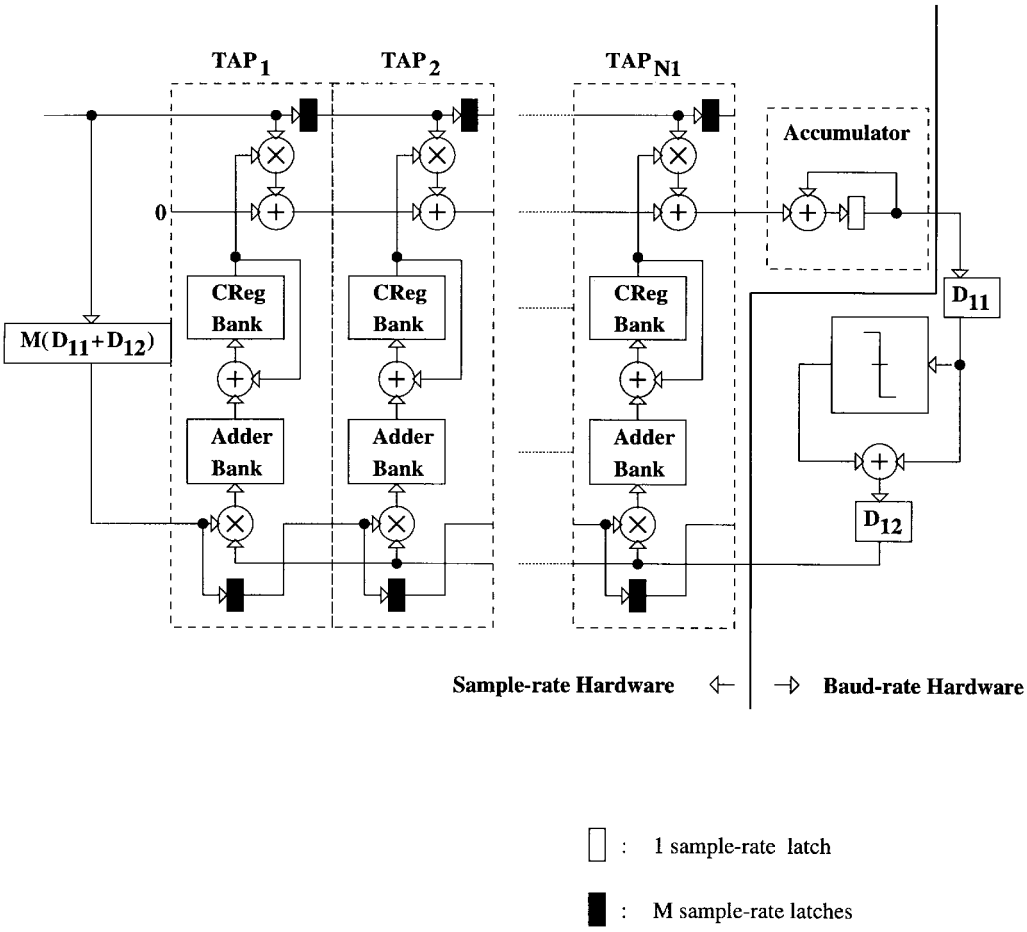
$$\begin{aligned} e_R(nT) &= Q[y_R(nT)] - y_R(nT) \\ &= Q[y_R(nT)] - \boldsymbol{W}_R^T((n-D_2)T)\boldsymbol{X}(nT) \quad (3.5a) \\ \boldsymbol{W}_R(nT) &= (1-\gamma)^{D_2}\boldsymbol{W}_R((n-D_2)T) \\ &\quad + \mu \sum_{i=0}^{LA-1} e_R(nT - iT - D_1T) \\ &\quad \cdot \boldsymbol{X}(nT - iT - D_1T) \quad (3.5b) \\ e_I(nT) &= Q[y_I(nT)] - y_I(nT) \\ &= Q[y_I(nT)] - \boldsymbol{W}_I^T((n-D_2)T)\boldsymbol{X}(nT) \quad (3.5c) \\ \boldsymbol{W}_I(nT) &= (1-\gamma)^{D_2}\boldsymbol{W}_I((n-D_2)T) \\ &\quad + \mu \sum_{i=0}^{LA-1} e_I(nT - iT - D_1T) \\ &\quad \cdot \boldsymbol{X}(nT - iT - D_1T). \quad (3.5d) \end{aligned}$$

Note that the relaxed look-ahead technique allows us to further simplify (3.5b) and (3.5d) by approximating the term $(1-\gamma)^{D_2}$ by $(1 - D_2\gamma)$. This is possible to do because the value of γ is small with unity. This approximation is known as *product relaxation* and has been employed in the past to pipeline the adaptive quantizer [32] and the adaptive lattice filter [31]. Furthermore, the product $D_2\gamma$ can be adjusted to be a power of two so that no multiplications are needed. The pipelined AFSLE architecture is shown in Fig. 8(b), where D_1 and D_2 represent baud-rate delays. The D_1 and D_2 delays can be employed to pipeline the $\boldsymbol{F}$ and the WUD blocks, respectively. Thus, fine-grain pipelining of all the blocks can be achieved.

The relaxed look-ahead technique [31] modifies the input–output mapping of a serial algorithm to obtain a pipelined algorithm. Therefore, a convergence analysis of the pipelined algorithm becomes necessary. In the present context, the pipelined AFSLE needs to be analyzed for convergence. However, as described in the previous section, we have derived the pipelined AFSLE via an inspection of the pipelined LMS algorithm [32]. Therefore, the convergence analysis of the pipelined AFSLE would be identical to that of the pipelined LMS in [32]. Hence, in this paper, we will not analyze convergence behavior of the pipelined AFSLE. Instead, we will study the performance of the proposed architecture in a broadband access environment in Section IV-C.

D. The FSLE Architecture

In this subsection, we will describe a general pipelined FSLE architecture. The final architecture is based on the results of the finite-precision analysis of the algorithm described in (3.5). In case of the pipelined FSLE algorithm, the impact of the look-ahead factor LA on the precision has been studied in [34], where it was found that the product μLA determines the WUD-block precision. Based on the desired SNR_o of about 27 dB (23.25 dB for a BER of 10^{-10} plus a 3 dB margin), the peak-to-average ratio of the received signal and the noise enhancement due to the equalizer, it can be shown that 8 bits of precision is required for the A/D and D/A converters. A finite-precision analysis of the receiver algorithm indicates (similar to [26]) that the F-block requires 10-bit



(c)

Fig. 8 (*Continued*). AFSLE. (c) Pipelined architecture.

coefficient precision, and the WUD-block would need 23 bits for coefficient adaptation. With these precision values, the finite-precision transceiver model was able to achieve an SNR_o that was within 0.1 dB of that of the floating-point model.

The architecture of the FSLE [which is shown in Fig. 8(c)] consists of $N1$ hardware taps, where $N1 = N/M$ and $M = Tf_s$. The number of hardware taps $N1$ is less than N due to the M-fold down sampling at the F-block output. For both applications under consideration, $N1 = 8$ was deemed sufficient via algorithm simulations. However, this value of $N1$ along with the signal precisions (described in the previous paragraph) required a value of $D_1 = 5$ (baud-rate algorithmic latches). Of these, $D_{11} = 2$ and $D_{12} = 3$ latches were employed to pipeline the F-block and the WUD-block, respectively. Note that it is only the D_{11} latches that would result in an increased end-to-end delay due to pipelining. Retiming the D_{11} latches resulted in a pipelining latch at the output of every multiplier and adder in the F-block.

The WUD-block consists of a multiplier [in order to compute the product of the slicer error and data in (3.5b) and (3.5d)], an adder bank [to compute the summation in (3.5b) and (3.5d)] and a coefficient register (CReg) bank to store the coefficients. The CReg bank consists of $D_{22} = MD_2$ latches, where D_2 delayed versions of M algorithmic taps [see Fig. 8(c)] are stored. In case of the in-phase filter, the WUD-block can implement a modified form of (3.5b)

$$\begin{aligned}\boldsymbol{W}_R(nT) &= (1-\gamma)^{D_2}\boldsymbol{W}_R((n-D_2)T) \\ &\quad + \mu \sum_{i=0}^{LA-1} e_R(nT - iT - D_1T) \\ &\quad \cdot \boldsymbol{X}(nT - iT - D_1T) \\ &= (1 - D_2\gamma)\boldsymbol{W}_R((n-D_2)T) \\ &\quad + \mu \sum_{i=0}^{LA-1} e_R(nT - iT - D_1T) \\ &\quad \cdot \boldsymbol{X}(nT - iT - D_1T) \end{aligned} \tag{3.6}$$

which is the result of product relaxation described in the previous subsection. The product $D_2\gamma$ was chosen to be a power of two such that $D_2\gamma\boldsymbol{W}_R((n-D_2)T)$ gives the sign bit of $\boldsymbol{W}_R((n-D_2)T)$. Hence, tap leakage is implemented by adding the sign of the current weight [14] to the least-significant bit in the WUD-block. Thus, the WUD-block adder shown in Fig. 8(c) is in fact two 23-bit additions, which need to be accomplished within a sample period of 19 ns. This is not difficult to do as long as the latches in the CReg bank can be employed to pipeline the additions.

The accumulator at the output of TAP_{N1} is reset after every M sample clocks. This is because the N-tap convolution in Fig. 8(b) is computed $N1 = N/M$ taps at a time by the

architecture in Fig. 8(c). The slicer is a tree-search quantizer that is also capable of slicing with two or four levels. This two-mode capability of the slicer is needed in order to have a blind start-up employing the reduced constellation algorithm [14].

IV. Simulation and Experimental Results

In this section, we describe some quantitative results for the performance of the 16-CAP transceiver. An important quantity for the performance evaluation of transceivers is the "margin," which is the difference between the SNR at the slicer (SNR_o) and at the input to the receiver (SNR_i). The quantity SNR_i [which is defined in (2.10)] is of limited value for performance evaluation purposes. On the other hand, SNR_o [see (2.11)], which is the noise variance at the input of the slicer, is more useful because it is directly related to the BER when the noise samples have a Gaussian distribution. In this case, taking 16-CAP as an example, a value of $\text{SNR}_o = 23.25$ dB corresponds to a BER $= 10^{-10}$. Let SNR_o be the SNR at the slicer for a given experiment, and let $\text{SNR}_{o,\text{ref}}$ be the SNR required to achieve a given BER. The margin achieved by the transceiver with respect to this BER is then defined as

$$\text{margin} \triangleq \text{SNR}_o - \text{SNR}_{o,\text{ref}}. \tag{4.1}$$

A positive margin in (4.1) means that the transceiver operates with a BER that is better than the targeted BER, and a negative margin means that it operates with a BER that is worse.

We provide simulation results in order to verify the performance of the transceivers. In Sections IV-A and B, we consider the serial FSLE and study its performance as a function of the receiver complexity. In Section IV-A, we present simulation results for 51.84 Mb/s ATM-LAN. Results for broadband access are presented in Section IV-B. Finally, the performance of the pipelined adaptive FSLE is verified in Section IV-C.

A. 51.84 Mb/s 16-CAP ATM LAN

In this subsection, we present computer simulation results obtained with the 51.84 Mb/s 16-CAP transceiver over a 100-m category 3 cable for various scenarios of NEXT loss characteristics. First, we will derive the system parameters for this application. The FCC Class-B [7] requirements state that the transmit spectrum be limited to 30 MHz. The excess bandwidth was chosen to be 100%, given our intention to employ the concept of NEXT suppression [30]. This implies that the symbol rate $1/T$ should be less than 15 MHz. For a data rate of 51.84 Mb/s, we can obtain a symbol rate of 12.96 MHz provided 4 bits are encoded per symbol. Hence, we need a 16-CAP constellation with a transmit spectrum having 100% excess bandwidth extending from dc to 25.92 MHz and a symbol rate $1/T$ equal to 12.96 MBd. This required that the D/A (at the transmitter) and the A/D at the receiver to operate at 51.84 Msamples/s. In the simulations to follow, the receiver consisted of the FSLE shown in Fig. 6(b).

In Table I, we show the margin obtained with the ATM-LAN transceiver with 100% excess bandwidth and a transmitter and receiver spans of $32T$ each. This corresponds to 128 multiply-adds per symbol period given that the A/D sample rate is four times the symbol rate. The first four rows of data in Table I were obtained with the TIA/EIA NEXT loss model [7] for category 3 cables. The other entries in the table were obtained using measured NEXT loss characteristics for worst-case category 3 cable. The terms ϕ_i $(i = 0, \cdots, 3)$ refer to the four relative phases that the clock of the transmitter, generating the dominant NEXT signal, can have with respect to the receiver clock. The different phases are obtained by shifting the relative phase of the clocks of the disturbed and disturbing CAP signals by multiples of the sampling period T_s. This relative phase influences the performance because of the cyclostationary nature of the two signals.

TABLE I
Performance of 51.84 Mb/s 16-CAP Transceiver over 100 m Category 3 Cable with One Cyclostationary Next Interferer

NEXT Model	Φ_i (iT/4)	SNR_i (dB)	SNR_o (dB)	Margin † (dB)
TIA/EIA Model	Φ_0	13.8	25.9	2.65
	Φ_1	13.8	27.1	3.85
	Φ_2	13.8	27.0	3.75
	Φ_3	13.8	26.0	2.75
Worst-case Measured	Φ_0	17.8	28.3	5.05
	Φ_1	17.8	27.2	3.95
	Φ_2	17.8	29.7	6.45
	Φ_3	17.8	29.3	6.05

† Margins are with respect to $P_e = 10^{-10}$ for which $SNR_{o,ref} = 23.25$ dB

The quantity of interest in Table I is the margin, which is given in the last column. Notice that all the margins are positive; therefore, the 16-CAP transceiver achieves a BER that is better than 10^{-10} for all cases considered in the table. Notice also in Table I that the values of the SNR at the input of the slicer, i.e., SNR_o, are much larger than the values of the SNR at the input of the receiver, i.e., SNR_i. Thus, the FSLE used in the receiver improves the SNR. This is possible because the FSLE performs NEXT suppression. It should be pointed out that the computer simulation results in Table I are consistent with similar results obtained in the laboratory.

An important VLSI consideration in the design of the receiver is the number of taps in the FSLE. For a given symbol rate $1/T$, it is necessary to reduce the number of multiply-adds per symbol period. In the case of the receiver in Table I, the number of multiply-adds per symbol period is equal to 128. We also studied the effect of the number of equalizer taps on the margin. With a transmitter span of $4T$ and a receiver span of $8T$, noise margins (optimum phase, worst phase) of (3.5 dB, 1.3 dB) were obtained with measured NEXT. Furthermore, increasing the receiver span to $13T$ resulted in an increase in the margin to (4.7 dB, 2.9 dB), which is about a 1.2-dB increase. Yet another way to improve the noise margin is to increase the excess bandwidth to 120% with the transmit spectrum extending from dc to 28.512 MHz. With a receiver span of $8T$ and 120% excess bandwidth, we obtained a noise margin of (3.85 dB, 2.65 dB). This requires that the converters

TABLE II
PERFORMANCE WITH 600-FT UTP CABLE AND FEXT FOR 51.84 MB/S 16-CAP TRANSCEIVER

Worst Case FEXT
16 CAP : $\alpha = 0.39$ $f_c = 14MHz$ $1/T = 12.96Mbauds$ $P_e = 10^{-7}$ †
16 CAP : $\alpha = 0.5$ $f_c = 16.2MHz$ $1/T = 12.96Mbauds$
16 CAP : $\alpha = 1.0$ $f_c = 12.96MHz$ $1/T = 12.96Mbauds$

Excess Bandwidth	FEXT	SNR_i (dB)	SNR_o (dB)	Margin (dB)	Capacity (Mb/s)
0.39	(8,(3,11,24,9,20,22,10,2,16,23,7))	26.8	27.1	5.6	147
0.5	(8,(3,11,24,9,20,22,10,2,16,23,7))	25.6	25.8	4.3	145
1.0	(8,(3,11,24,9,20,22,10,2,16,23,7))	28.1	29.5	8.0	226
0.5	(12,(1,6,7,15,17,19,20,21,22,24,25)) ††	33.1	33.2	11.7	145
0.5	(16,(1,3,6,9,12,13,17,19,21,22,23)) †††	31.0	31.2	9.7	145

† With 16-CAP and Gaussian noise, the required SNR_o for this probability of error is 21.5 dB
†† 12 best pairs amongst 25 pairs
††† 12 short twist pairs amongst 25 pairs

in the receiver and the transmitter operate at a sample rate of at least 57.024 MHz. However, in order to maintain an integral relationship between the sample and symbol rates, we need to employ a sample rate of 64.8 MHz. Therefore, we see that determining the optimum receiver complexity requires one to trade off the algorithm performance (i.e., the noise margin) with the VLSI performance (i.e., power dissipation and area).

These simulation results and the corresponding laboratory experiments were the basis on which the ATM-LAN transceiver chip [33] was designed.

B. Broadband Access

In this subsection, we present the computer simulation and experimental results for a 51.84 Mb/s 16-CAP transceiver in the presence of FEXT. The design considerations for broadband access were similar to that of the ATM-LAN case, except for the following differences. The upstream and downstream channels for this application were on a single wire pair. Furthermore, the frequency band from dc to approximately 5 MHz could not be utilized due to the presence of dimmer noise. Therefore, we chose an excess bandwidth of 50% with a center frequency of 16.2 MHz. This resulted in the transmit spectrum going from 6.48 to 25.92 MHz. Table II gives the performance results for various 51.84 Mb/s 16-CAP transceivers operating over a 600-ft UTP cable, where we have chosen $\text{SNR}_{o,\text{ref}} = 21.5$ dB, which corresponds to the value of SNR_o that provides a probability of error of 10^{-7} for a 16-CAP transceiver. This value of $\text{SNR}_{o,\text{ref}}$ is deemed sufficient for the broadband access environment.

Table II also gives the performance results of the 16-CAP transceiver when we select the 12 best pairs amongst the 25 pairs of the UTP cable. It can be noted in Table II that over 11 dB of margin can be achieved with the 12 best pair selection. The last row in Table III gives the performance results when we select 12 pairs with short twists. Even though

TABLE III
PERFORMANCE OF THE PIPELINED AFSLE ARCHITECTURE IN BROADBAND ACCESS

51.84 Mb/s 16-CAP Eleven Worst-Case Measures FEXT			
16-CAP :	$a = 0.5$	$f_c = 16.2$ MHz	$1/T = 12.96$ Mbauds
γD_2	$D_2 = 1$ $LA = 1$	$D_2 = 3$ $LA = 2$	$D_2 = 5$ $LA = 4$
2^{-13}	21.8 dB	24.3 dB	25.4 dB
2^{-15}	25.4 dB	24.7 dB	25.8 dB
2^{-20}	25.8 dB	25.8 dB	25.8 dB

the performance with short twist length is not necessarily better than that with longer twist length, over 9 dB of margin is achieved by selecting the 12 short twist pairs amongst the 25 pairs of the UTP cable. Comparing SNR_i and SNR_o in Table II, we see that there is almost no noise enhancement in the 16-CAP receiver with $\alpha = 0.5$ and $\alpha = 0.39$, where $\alpha = 1.0$ corresponds to 100% excess bandwidth. Note that the broadband access has a relatively mild loop loss and a flat FEXT loss. Therefore, the performance of the transceiver is not a strong function of the number of equalizer taps. This was verified by comparing the noise margins for an equalizer spans of $8T$ and $32T$.

Table II also shows an upper bound on the achievable data rate, which is given by Shannon's capacity formula

$$C_N(d,W) = \int_0^W \log_2[1 + \text{SNR}(f)]\, df \qquad (4.2)$$

where $\text{SNR}(f)$ is the SNR at frequency f at the input of the receiver, and W is the channel bandwidth that is being utilized. Employing the FEXT and EL-FEXT power-sum loss expressions in (2.3) and (2.4) and substituting into (4.2), we can compute the channel capacity over distribution loop as

$$C_N(d,W) = \int_0^W \log_2\left[1 + \frac{K}{\Psi f^2 d}\right] df. \qquad (4.3)$$

It can be shown that the capacity is greater than 100 Mb/s, indicating that the present data-rates (51.84 Mb/s) are approximately one third of the upper bounds.

Thus far, the FEXT signal was assumed to be stationary. However, simulation results with cyclostationary FEXT have also been done. For cyclostationary FEXT, it is assumed that the disturbed and interfering signals have clocks that are synchronized in frequency (but not necessarily in phase) [18]. Extensive laboratory experiments are presently being conducted in order to verify the simulation results. Preliminary results indicate that the performance obtained in the laboratory is in good agreement (within 2 dB) with that obtained through computer simulations.

As discussed in Section II-B, a DFE is necessary to combat spectral nulls introduced by splitters and narrowband RFI. Fig. 9 shows the transfer function of the feedforward filter when the ISI-DFE is converged in the presence and absence of two narrowband interferers. The dotted and solid lines in Fig. 9 show the transfer function of the feedforward filter of the ISI-DFE in the presence of FEXT only and FEXT and two narrowband interferers, respectively. It is noted from the transfer function (solid line) that the feedforward filter

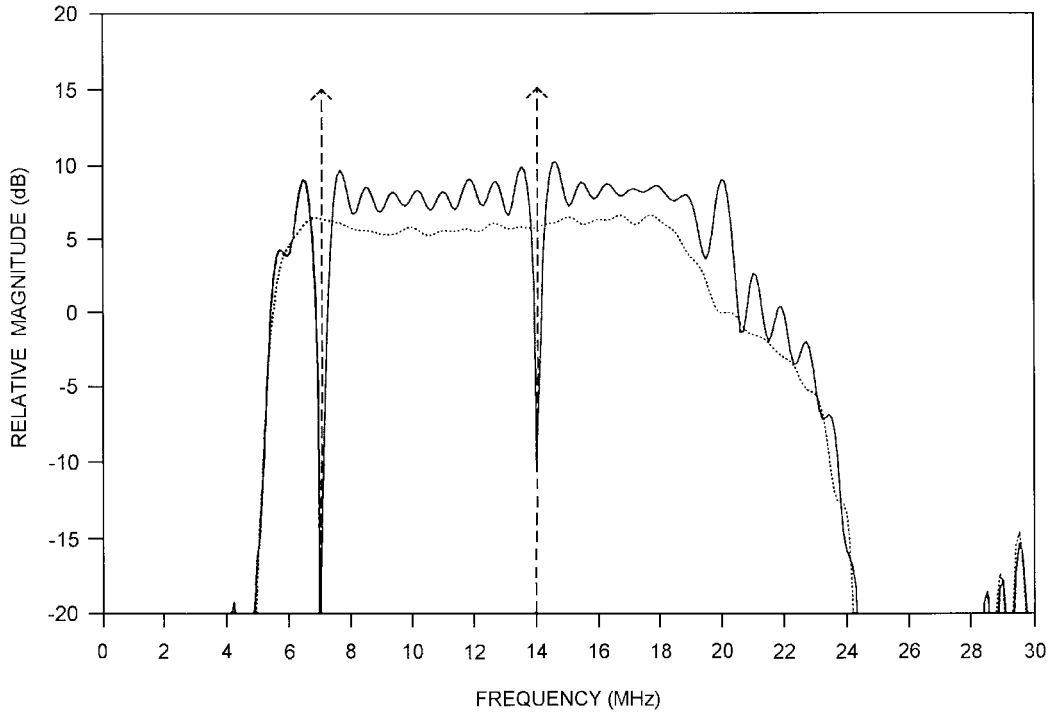


Fig. 9. Transfer function of the feedforward filter in the ISI-DFE in presence of FEXT and FEXT with two narrowband interferers.

simply notches out the two narrowband interferers. Computer simulation and laboratory experiments show that there is no noticeable difference in performance comparing the two cases in Fig. 9.

C. Pipelined Adaptive FSLE

In this subsection, we study the performance of the pipelined AFSLE [see Fig. 8(b)] in the broadband access environment. From (3.5), we see that the adjustable parameters of the pipelined AFSLE architectures are D_1, D_2, LA, and γ. With a receiver span of $8T$, there was no noticeable difference in the performance ($\text{SNR}_o = 25.8$ dB) due to the change in the D_1. This was observed for values of D_1 ranging from 0 to 100, indicating that very fine level of pipelining in the AFSLE was possible via the delay relaxation.

In Table III, we show the effect of the sum and the product relaxations on the performance of the AFSLE. Observing one of the columns, we see that for a given value of D_2, the performance improves as γ is reduced. This is to be expected as the approximation $(1-\gamma)^{D_2} \approx (1-\gamma D_2)$ becomes more accurate for a smaller value of γ. From the values in one of the rows, we find that the performance is not altered as D_2 increases (for small values of γ). Therefore, we conclude that the relaxed look-ahead pipelined AFSLE is quite robust, especially in the broadband access environment.

V. Conclusions

Achieving high bit rates in the range of 50–155 Mb/s over bandlimited channels such as the UTP-3 with a transmit spectrum limited to 30 MHz is indeed a challenging proposition and currently of great interest. A conclusion that we draw here is the critical importance of developing communications algorithms for VLSI rather than just for the sake of BER performance. An integrated methodology is necessary whereby a clear path from algorithm development to silicon implementation is indicated. This integrated VLSI DSP design methodology was employed in the design of 51.84 Mb/s ATM-LAN [33] and broadband access transceivers [12]. A first step in this methodology was to obtain a proper understanding of the channel. Although we have considered NEXT (in ATM-LAN) and FEXT (in broadband access) impairments here, future work needs to be directed toward the development of receiver techniques for handling RFI. We also saw that the channel capacity for these environments was about three times the present data rates. Therefore, efforts are under way to approach data rates far above 100 Mb/s. In all cases, we need to consider power dissipation and area complexity along with algorithm performance. Hence, development of low-power adaptive receiver techniques is currently the focus of our efforts.

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