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| **Authors (contact)** | Hassan Dbouk (hdbouk2@illinois.edu)  
Sujan K. Gonugondla (gonugon2@illinois.edu)  
Charbel Sakr (sakr2@illinois.edu)  
Naresh R. Shanbhag (shanbhag@illinois.edu) |
| **Affiliation** | University of Illinois at Urbana Champaign |

*Article begins on next page*
A 0.44 µJ/dec, 39.9 µs/dec, Recurrent Attention In-memory Processor for Keyword Spotting

Hassan Dbouk, Student Member, IEEE, Sujan K. Gonugondla, Student Member, IEEE, Charbel Sakr, Student Member, IEEE, and Naresh R. Shanbhag, Fellow, IEEE

Abstract—This paper presents a deep learning-based classifier IC for keyword spotting (KWS) in 65 nm CMOS designed using an algorithm-hardware co-design approach. First, a Recurrent Attention Model (RAM) algorithm for the KWS task (the KeyRAM algorithm) is proposed. The KeyRAM algorithm enables accuracy vs. energy scalability via a confidence-based computation (CC) scheme, leading to a 2.5× reduction in computational complexity compared to state-of-the-art (SOTA) neural networks, and is well-suited for in-memory computing (IMC) since the bulk (89%) of its computations are 4b matrix-vector multiplies. The KeyRAM IC comprises a multi-bit multi-bank in-memory computing (IMC) architecture with a digital co-processor. A sparsity-aware summation scheme is proposed to alleviate the challenge faced by IMCs when summing sparse activations. The digital co-processor employs diagonal major weight storage to compute without any stalls. This combination of the IMC and digital processors enables a balanced trade-off between energy efficiency and high accuracy computation. The resultant KWS IC achieves SOTA decision latency of 39.9 µs with a decision energy < 0.5 µJ/dec which translates to more than 24× savings in the energy-delay product (EDP) of decisions over existing KWS ICs.

Index Terms—In-memory computing (IMC), keyword spotting (KWS), machine learning, recurrent attention networks

I. INTRODUCTION

Speech has emerged as a natural mode for humans to interact with intelligent Edge devices including smart phones and personal digital assistants [1]. A full fledged speech recognition system is complex and power hungry making it prohibitive for resource-constrained applications at the Edge. Preceding a speech recognizer with an ‘always-on’ keyword spotting (KWS) system enables such devices to continually sense, detect, and classify speech segments under stringent energy, computational and storage constraints.

A typical keyword spotting (KWS) pipeline (Fig. 1) processes raw audio in two stages: feature extraction and classification. The classification stage, which is often implemented via neural networks, dominates the complexity of the KWS system and presents a challenge for efficient KWS realization. Recently, various deep learning-based KWS classifier algorithms such as deep/convolutional neural networks (DNNs/CNNs) and recurrent NNs (RNNs) have been shown to achieve high (> 90%) accuracies [2] but at the expense of very high computational costs making them unsuitable for deployment on Edge platforms.

To that end, existing KWS ICs [3]–[7] aim at implementing off-the-shelf NN-based classifiers for KWS while focusing on minimizing the power consumption in order to maintain continuous operation. These ICs have mostly been: 1) implemented in digital utilizing low-power techniques such as voltage overscaling [4], [5], [7]; and 2) benchmarked with simple datasets, e.g., TIMIT. One exception is [6] which implements a binarized RNN-based KWS on an in-memory computing (IMC) architecture for the more complex Google Speech dataset [8]. Recently, [7] reported the lowest power consumption of 510 nW for a KWS IC by implementing depth-wise separable convolutional neural networks (DSCNNs) [9]. However, the implementation of [7] is limited to two keywords and requires 64 ms to classify one speech segment. For a ten keyword classification, the power penalty increases to 16 µW [6].

Realistically, speech related events occur infrequently which makes the ‘always-on’ detection of wake words using a KWS IC to be energy sub-optimal. Especially since a voice activity detector (VAD) IC can achieve $P_{\text{VAD}} < 200$ nW [10], which is much less than the KWS system. Therefore, by gating the KWS system with a VAD (Fig. 1), the total system power $P_{\text{tot}}$ can be significantly reduced and the power constraint on the KWS system is relaxed, as long as the audio events occur infrequently. In fact, it can easily be shown that the total system power can be expressed as:

$$P_{\text{tot}} = P_{\text{VAD}} + \alpha E_d$$  \hspace{1cm} (1)

where $\alpha$ is the voice activity rate (activity/s) and $E_d$ is the decision energy of the KWS IC. Expression (1) implies that the traditional viewpoint of minimizing the power of KWS ICs needs to be reconsidered. Instead, designers need to reduce the
energy per decision $E_d$ for a specified decision latency. This can be done by minimizing the decision-level energy-delay product (EDP) of the KWS IC, which is the focus of this work.

With that design goal in mind, this work employs an algorithm-hardware co-design approach to realize KWS for Edge devices with $< 1 \mu J/\text{decision}$ and a latency of $< 50 \mu s/\text{decision}$. To the best of our knowledge, this is the first work to propose using a Recurrent Attention Model (RAM) \cite{kim2018keyram}, previously proposed for image classification, for KWS (KeyRAM algorithm) and the first IC implementation of RAM for KWS (KeyRAM IC). The use of RAM for the KWS task reduces the computational complexity of inference compared to state-of-the-art neural network-based algorithms (Fig. 6) at iso-accuracy. The KeyRAM algorithm is mapped onto an IC consisting of two multi-bit sparsity-aware IMCs and a digital co-processor with a 96 × 512 standard 6T SRAM. The IC stores all model weights on-chip to further increase the energy efficiency. As a result, up to 7.6× savings in energy/decision and $>24\times$ savings in EDP of decisions over state-of-the-art IMC ICs for KWS is achieved, while realizing the lowest reported decision latency of 39.9 $\mu s$. Preliminary measurement results were reported in \cite{kim2018keyram}.

This paper is organized as follows: Section II provides the necessary background on IMC and RNNs. Section III explains the KeyRAM algorithm and demonstrates its effectiveness. The circuit and architectural implementation details of the KeyRAM IC are described in Section IV. Measurement results demonstrating the classifier’s confidence, accuracy, latency, and energy are presented in Section V. Section VII concludes this paper.

II. BACKGROUND

A. In-Memory Computing

In-memory computing (IMC) architectures \cite{kim2018keyram}–\cite{kim2019neural} have drawn much interest due to their ability to reduce the energy and latency cost of memory accesses for machine learning applications. The IMC concept was first introduced in \cite{kim2018keyram} and was later followed by numerous prototype ICs \cite{kim2018keyram}–\cite{kim2019neural} demonstrating its effectiveness. Since then, numerous IMC architectures \cite{kim2018keyram}–\cite{kim2019neural} spanning different bitcell layouts, e.g., 6T, 8T, 10T, and bit-precision support, e.g., binary, ternary, multi-bit, have been proposed. In this section, we focus on the IMC design in \cite{kim2018keyram, kim2019neural}, which is a mixed-signal multi-bit dot-product processor based on embedding the processing into the standard 6T SRAM bitcell array (BCA). This architecture realizes dot products efficiently, while preserving the density of the BCA. The IMC stores $B_w$-bit weights in the BCA in a column major format and computes dot-products between these weights and inputs stored in buffers in three steps: 1) bitcells (BCs) storing digital weights are concurrently accessed via pulse-width modulated word-lines (WLs), such that the voltage discharge $\Delta V_{\text{WL}}$ on each bit-line (BL) is proportional to the multi-bit weight in the memory; 2) the BL discharges are multiplied with the corresponding input data from buffers via column pitch-matched charge redistribution-based multipliers; and 3) the multiplier outputs are summed across the columns via charge sharing across BLs resulting in the final dot product which is converted to digital via ADCs. The accuracy of the IMC computations can be traded off with energy by controlling the word-line voltage $V_{\text{WL}}$. While IMC architectures (Fig. 2) have shown remarkable gains (100×) in the energy-delay product (EDP) over a von Neumann equivalent with minimal loss in inference accuracy \cite{kim2019neural}, they typically are limited to low-precision computations, and lack the flexibility of the von Neumann architecture due to their mixed-signal nature.

B. Recurrent Neural Networks

Recurrent neural networks (RNNs) \cite{hochreiter1997long} are a special type of fully connected (FC) networks characterized by a hidden state vector. RNNs maintain the hidden state vector via a feedback structure, which enables them to store temporal features when processing data sequentially. This makes RNNs suitable for speech related tasks which exhibit strong temporal correlations.

Given a length $T$ sequence of $N$-dimensional input vectors $\mathbf{x}_1, \ldots, \mathbf{x}_T$, at each timestep $t$, an RNN updates its $L$-dimensional hidden state vector $\mathbf{h}_t$ as follows:

$$
\mathbf{h}_t = f_h(\mathbf{h}_{t-1} \parallel \mathbf{x}_t) = \sigma \left( \mathbf{W}_h \cdot (\mathbf{h}_{t-1} \parallel \mathbf{x}_t) + \mathbf{b}_h \right)
$$

(2)

where $\sigma(\cdot)$ is an element-wise non-linearity function (typically a ReLU or a sigmoid), $(\parallel)$ denotes the vector concatenation operation, and $\mathbf{W}_h \in \mathbb{R}^{L \times (L+N)}$ and $\mathbf{b}_h \in \mathbb{R}^{L}$ are the learned weights and bias terms associated with the RNN. The initial hidden state vector $\mathbf{h}_0$ is the all zeros vector. In an $M$-way classification setup, an RNN is also equipped with a classifier that maps the hidden state vector into class probabilities. Specifically, we have

$$
\mathbf{y} = f_y(\mathbf{h}_T) = \text{softmax}(\mathbf{W}_y \cdot \mathbf{h}_T + \mathbf{b}_y)
$$

(3)

where $\mathbf{y} \in [0,1]^M$ is a vector of class scores, $\mathbf{W}_y \in \mathbb{R}^{M \times (L+N)}$ and $\mathbf{b}_y \in \mathbb{R}^M$ are the learned weights and bias terms associated with the classifier. The classifier needs to operate on the final hidden state vector in the sequence $\mathbf{h}_T$, which is a function of all the previous input vectors. During testing,
the pre-softmax output vector \( \tilde{y} \) is sufficient for predicting the associated class \( c \in \{1, \ldots, M\} \), since we have:

\[
c = \arg \max_{i \in [M]} \{y_i\} = \arg \max_{i \in [M]} \{\tilde{y}_i\}
\] (4)

Similar to other network architectures, RNNs can be trained in a supervised learning setup using labeled data and the stochastic gradient descent (SGD) algorithm. The required gradients can be computed using back-propagation through time (BPTT) [25], which is essentially the traditional back-propagation algorithm with the recursive computation of the RNN unrolled.

### III. THE KEYRAM ALGORITHM

This section describes the KeyRAM algorithm and compares its performance against state-of-the-art neural network-based algorithms for KWS. KeyRAM employs the RAM algorithm [11], originally proposed for image classification, for the KWS task. It employs an RNN in a feedback loop to selectively process input subsets (glimpses) in the feature space, as opposed to processing the entire input feature, thereby reducing the computational complexity.

#### A. KeyRAM Algorithm

The KeyRAM algorithm (Fig. 3) employs 6 fully connected layers (\( f_1 \) to \( f_6 \)) to track the informative features across multiple glimpses \( t \) via a hidden state vector \( h_t \). At each glimpse \( t \), KeyRAM combines the previous hidden state vector \( h_{t-1} \) with the glimpse vector \( g_t \) (which is obtained from the input patch vector \( x_t \) and location vector \( l_t \)) to compute \( h_t \):

\[
h_t = f_4(h_{t-1} \parallel g_t) = \text{ReLU} \left( W_4 \cdot (h_{t-1} \parallel g_t) + b_4 \right)
\] (5)

The glimpse vector \( g_t \) combines information from the input patch vector and the location vector via two stages of processing involving three fully connected layers:

\[
g_t = f_3(q_t \parallel p_t) = \text{ReLU} \left( W_3 \cdot (q_t \parallel p_t) + b_3 \right)
\] (6)

where \( p_t \) and \( q_t \) are the processed input patch vector \( x_t \) and location vector \( l_t \) respectively. They are computed as follows:

\[
p_t = f_2(x_t) = \text{ReLU} \left( W_2 \cdot x_t + b_2 \right)
\] (7)

\[
q_t = f_1(l_t) = \text{ReLU} \left( W_1 \cdot l_t + b_1 \right)
\]

Given the updated hidden state vector \( h_t \), the KeyRAM algorithm predicts both the up-to-date class probability scores \( y_t \) and the next location vector to process \( l_{t+1} \) as follows:

\[
y_t = f_5(h_t) = \text{softmax} \left( W_5 \cdot h_t + b_5 \right)
\] (9)

\[
l_{t+1} = f_6(h_t) = \text{hardtanh} \left( W_6 \cdot h_t + b_6 \right)
\] (10)

After training, the class prediction of the KeyRAM algorithm improves in confidence (class score) as more glimpses are processed (Fig. 4). To do so, the location vectors produced over time must correspond to locations in the input feature that are highly informative. This dynamic nature of KeyRAM enables a natural trade-off between complexity and accuracy, which is translates to an energy/latency vs. accuracy trade-off, where the number of glimpses per decision \( n_G \) acts as a tuning knob. In order to train the KeyRAM algorithm, we use the same hybrid supervised loss function from [11], which formulates RAM as a reinforcement learning problem, with the location network acting as an agent whose loss function is based on a reward, whereas the rest of the layers are learned using the standard cross-entropy loss function.

#### B. Enabling Accuracy-Energy Scalability

The decision accuracy of the KeyRAM algorithm is proportional to the class confidence level or the class score, which increases with the number of glimpses \( n_G \) and hence the energy cost. We introduce a confidence-based computation
(CC) strategy to provide a seamless trade-off between accuracy and energy. At each glimpse \( t \), let \( c_t \in [M] \) be the predicted class label obtained from \( y_i, t \) as follows:

\[
c_t = \arg\max_i \{ y_i, t \}
\]

and \( y_i, t \in [0, 1] \) be its associated class score. For a specific threshold \( \tau \in [0, 1] \), the KeyRAM algorithm with the CC strategy (KeyRAM-CC) terminates at glimpse \( t = n_G \) if one of the following conditions holds: \( y_{n_G, n_G} > \tau \) or \( n_G = N_G \), where \( N_G \) is the maximum number of glimpses allowed per decision, i.e., \( n_G \leq N_G \). The choice of the confidence threshold \( \tau \) can be used to trade-off the decision accuracy w.r.t. complexity. A small value of \( \tau \) implies that the classifier isn’t confident about its decision resulting in lower accuracy but also lower energy consumption since decisions are obtained with smaller values of \( n_G \). On the other hand, a large value of \( \tau \) implies a higher value of \( n_G \), i.e., more glimpses per decision, and hence better accuracy at the expense of more energy consumption.

C. Enabling Audio Classification

To enable audio classification, we use Mel-frequency Cepstral Coefficient (MFCC) [26] features as KeyRAM inputs. Since audio features exhibit only temporal invariance, we propose a location vector \( l_t \) that points to the time index of the MFCC feature.

Figure 5 describes the input patch vector generation for a given MFCC feature matrix \( X \in \mathbb{R}^{K \times T} \) where \( K \) denotes the number of Mel-features used and \( T \) is the number of time samples. The location vector \( l_t \) points to a time index, and a rectangular patch of size \( K \times P \) is extracted accordingly. The input patch vector \( x_t \in \mathbb{R}^{PK} \) is therefore obtained by vectorizing the rectangular patch. This process can be described using the patch extractor function \( \phi \):

\[
x_t = \phi(X, P, l_t)
\]

The wider the patch (higher \( P \)), the more information is contained in \( x_t \), and more processing required per glimpse. Note that for 2D images, the location vector \( l_t \) would be two dimensional, where each entry corresponds to a separate image axis. However, for KWS, we are only interested in one axis, and therefore \( l_t \) becomes a scalar \( l_t \).

Table I details both the activation functions as well as the shapes of the 6 fully connected layers as a function of: \( d_t \) the dimension of \( q_t \); \( d_x \) the dimension of \( p_t \); \( d_2 \) the dimension of \( r_t \); and \( d_h \) the dimension of \( h_t \), for using KeyRAM with \( M \) keywords, \( K \) Mel-features, and a patch of width \( P \).

D. Performance of KeyRAM

To benchmark the effectiveness of the KeyRAM algorithm, we use the recent Google Speech [8] dataset. We compare KeyRAM against several classical neural network architectures for KWS reported in [2]. Similar to [2], we use 12 keywords (including ‘silence’ and ‘unknown’ labels) from the Google Speech dataset. Figure 6(a) plots the performance, in terms of classification accuracy, of different network architectures and KeyRAM vs. number of floating-point operations required for a single inference. The complexity of the KeyRAM is varied by changing the number of glimpses and the model size. KeyRAM reduces the number of operations required for inference by \( \sim 2.5 \times \) compared to state-of-the-art neural network-based algorithms from [2] at iso-accuracy. For the same number of operations, KeyRAM is able to achieve a \( \sim 5.6\% \) improvement in the classification accuracy as well. Figure 6(b) shows that KeyRAM remains competitive in terms of storage, which is reflected in the number of model parameters required.

IV. IMPLEMENTATION

This section describes the architecture of the KeyRAM prototype IC in 65 nm CMOS.
A. Architectural Mapping

The main challenges in implementing the KeyRAM algorithm using an IMC-based architecture are threefold: 1) the irregular layer shapes in KeyRAM make it difficult to map onto IMC architectures, where the support for arbitrary length dot products (DPs) is limited; 2) the sparsity of the input activations present a challenge for any IMC implementation employing a charge sharing summation scheme, such as that of [13]; and 3) the precision requirements for different layers vary. In fact it is quite common in DNN quantization [27]–[30] to allocate higher bit-widths for the first and last layers. This presents an issue for IMC architectures, as they are typically meant for low-precision operations, due to the inherent non-idealities associated with mixed-signal computing.

However, we find via precision analysis, that KeyRAM’s early (f₁ and f₂) and final (f₅ and f₆) layers require 8b precision, whereas the intermediate layers f₃ and f₄ require 4b precision (both weights and activations) in order to maintain accuracy. Furthermore, Table II indicates that our design choice of 8b for f₁/f₂/f₃/f₅/f₆ and 4b for f₄/f₆ achieves an accuracy within 0.2% of that of an 8b baseline whereas a fully 4b KeyRAM algorithm would suffer from an accuracy loss of ~ 3% compared to the 8b baseline thereby indicating that extreme quantization, e.g., binarization, is not an option.

The parameters values of the KeyRAM architecture chosen for IC implementation are detailed in Table II. The number of operations of the resultant network architecture is dominated.

B. Architecture and Timing

The KeyRAM architecture (Fig. 7) processes a single glimpse using 5 operating modes (Fig. 8) without the need for off-chip data transfer since all weights are stored on-chip. Internal vector buffers are utilized to transfer data between operating modes. These buffers allow us to swap the output of one stage into the input of the next stage without stalling.

The architecture comprises of: 1) two IMC blocks (IMC0 and IMC1) to implement multi-bit MVMs via temporal folding into a sequence of dot products. The IMC block is based on the single-bank IMC architecture in [13] which implements a single multi-bit dot-product per read cycle. Each IMC block in KeyRAM consists of a standard 6T SRAM 512 × 256 bit-cell array (BCA) with per-column multipliers and a cross-column adder. The two IMC blocks share four 6-b ADCs and implement f₃ and f₄ respectively; 2) a diagonal major MVM kernel (DM²VM) to efficiently implement f₁, f₂, f₅, and f₆ (10.8% of the total complexity) are computed in 8b precision digital using a novel and optimized dataflow. Layers f₅ and f₆ are fused together and implemented using a single matrix-vector multiply (MVM) routine, since they share the same input vector hₚ.

C. IMC Block

The proposed multi-bit IMC architecture (Fig. 9) has two modes of operations: 1) a regular SRAM R/W mode and 2) a DP mode in which it can implement sparse dot-products between a buffered input vector and the weights stored in the BCA as described in Section II. The BCA employs a
standard 6T SRAM bitcell designed with logic rules occupying 1.93 µm². In the DP mode, the IMC can access four (Bₜ = 4) consecutive rows simultaneously via the WL drivers. The resultant voltage drop on each bitline (ΔV_{BL}) is proportional to the 4b digital weight stored in that column. By tuning both the wordline voltage V_{WL} and the minimum pulse width T₀, we can control the maximum bitline discharge voltage ΔV_{BL-max}. In this work, we fix T₀ = 250 ps, and vary V_{WL} between 0.5 V and 0.8 V, which translates to a maximum bitline discharge voltage between 0.32 V and 0.54 V. The energy consumption of the IMC is a strong function of ΔV_{BL-max} and thus V_{WL}. A small ΔV_{BL-max} implies more energy efficiency, at the expense of compute accuracy, as demonstrated in [14]. The presence of PVT variations prohibits the use of extremely small ΔV_{BL-max} values, and thus the value of V_{WL} must be chosen with care. In this work we find that a V_{WL} = 0.7 V is sufficient for maintaining proper operation.

The IMC can realize dot-products between signed weights and unsigned inputs. In each column, the sign of the weight is computed by comparing the BL and BLB voltages, and the absolute value of the weight (ΔV_{BL-abs} = min(ΔV_{BL}, ΔV_{BLB})) is multiplied with the corresponding digital input via a column pitch-matched charge re-distribution-based multiplier (similar to that of [14]). The IMC requires two separate voltage sharing rails that compute the partial-dot-products using the positive weights and the negative weights separately. Therefore, at the end of each DP operation, two output voltages V_p and V_n need to be sampled and converted to digital. This is done via two separate ADCs, one for each rail voltage. The IMC design can be easily modified to support signed inputs by computing the partial product sign instead of the weight sign via a simple XOR gate between the weight sign and the input sign signals in each column. The partial product sign can be used to decide which voltage sharing rail to use, and thereby realize a fully signed DP operation efficiently.

In order for the ADC delay not to bottleneck the DP operation, we ping-pong between two pairs of ADCs in every read cycle. The CTRL block sequences the DP operations in order to realize the full MVM. Figure 10 details the timing information in terms of number of cycles required by each stage in the DP operation, and the ping-pong ADC schedule. The ADC outputs are scaled and shifted to calibrate for offsets followed by a ReLU non-linearity, and are subsequently routed to the input buffers.

The support for input-sparse dot-products is crucial for proper operation while realizing neural networks. This is due to the use of the ReLU activation function, which increases the input activations sparsity to ~ 50%–70%. Sparse input vectors present a challenge for the charge sharing summation scheme used in [13] as the multiplier output voltage spread shrinks. A sparsity-aware summing (SAS) method (Fig. 9(b)) is proposed in which the per-column multiplier output voltages (V_{m,i}) are selectively charge shared based on whether the corresponding input element is zero or not. Th SAS scheme operates in two stages and is synchronized by the CTRL block via the control signals φ₁ and φ₂. When φ₁ switches, all V_{m,i}’s are dumped onto per-column unit capacitors. Next, φ₂ switches to trigger the summation process. In every column, signal φ₃,i is derived from φ₂ to select whether or not V_{m,i} should be dumped onto the charge sharing rail. In the process, the output swing is preserved thereby improving the ADC accuracy. In order for this to work, the number of non-zero elements N_z in the N-dimensional input vector must be known to properly scale the post-ADC output. We compute N_z as the inputs are streamed in thereby incurring minimal latency overhead.

The effectiveness of the proposed SAS scheme is validated via numerical simulations. Ideally, we would like to compute the DP:

\[ y_0 = \sum_{i=1}^{N} x_i w_i \]  

(13)

where \( x_i \in \{0, \ldots, 1-2^{-4}\} \) and \( w_i \in \{-1-2^{-3}, \ldots, 1-2^{-3}\} \) are the quantized inputs (unsigned) and weights (signed), respectively. The charge sharing summation is equivalent to an averaging operation, which results in the following computation of the DP:

\[ y_1 = N \cdot Q \left( \frac{1}{N} \sum_{i=1}^{N} x_i w_i \right) \]  

(14)

where \( Q(\cdot) \) is the \( B_y \)-bit ADC quantization function. In the presence of the SAS scheme, the averaging occurs over the non-zero partial products, which can be expressed as:

\[ y_2 = N_z \cdot Q \left( \frac{1}{N_z} \sum_{i=1}^{N} x_i w_i \right) \]  

(15)
The signal-to-noise ratio (SNR) between the ideal output $y_j$ and the actual output $y_j$ ($j \in \{1, 2\}$) is defined as follows:

$$\text{SNR}_j = 10 \log_{10} \left( \frac{\sigma_{y_0}^2}{\sigma_{y_j - y_j}^2} \right) \quad (16)$$

Figure 11 plots SNR$_1$ (without SAS) and SNR$_2$ (with SAS) against the input sparsity for randomly sampled weights and inputs. As expected, when the inputs are not very sparse (< 20%), the impact of SAS is negligible. However, for the typical input sparsity range observed in KeyRAM, the SAS scheme improves the DP SNR by 5 dB-to-10 dB.

D. $DM^2$VM Block

The $DM^2$VM block is a synthesized digital co-processor operating using a 500 MHz clock consisting of: 1) a 96 × 512 standard 6T SRAM for parameter storage; 2) an array of 64 processing elements (PEs), each implementing an 8b×8b multiply-accumulate (MAC) operation; 3) a local controller to manage the SRAM R/W functionality, synchronize operations with the main clock and manage data buffers. The block digitally computes all MVM operations in $f_1$, $f_2$, $f_5$ and $f_6$, with 8b inputs and 8b weights using three operating modes ($f_5$ and $f_6$ are fused together). The MVM dot-products are computed via the PE array, with weights fetched from the SRAM and inputs streamed in from a dedicated buffer. The 25-b accumulated dot-product outputs are truncated to 8b per algorithmic requirements. The $DM^2$VM processor is designed to minimize idle cycles when inputs/outputs are streamed in/out since the diagonal major architecture is able to complete an $N \times M$ MVM in a fixed number $N + M$ cycles irrespective of whether $N > M$ or vice-versa. In contrast, an input (output) stationary architecture requires between $2N + M$ ($N + 2M$) and $N + M$ cycles, respectively, based on whether the input/output both are streamed or not.

Figure 12 illustrates the principle of the $DM^2$VM kernel for a 4 × 4 FC layer. During the setup phase, the weight matrix is stored in the SRAM in diagonal major format. The $DM^2$VM begins computation as soon as the first input is streamed in and stops exactly when the final output is streamed out without any stalls. Each PE cycle consists of 8 clock cycles, involving fetching one weight diagonal from the SRAM and computing the partial sums using the shifted inputs. Once all the inputs are shifted in, the shift register flips direction and starts streaming out the completed output sums. The bias vector is pre-fetched in a dedicated buffer, and each element is added to the final output term once its streamed out. This makes the $DM^2$VM well-matched to the diverse set of MVM dimensions utilized by the KeyRAM algorithm.

V. Experimental Results

This section describes the measured results from the prototype IC, and compares its performance with existing KWS ICs. The 65 nm CMOS IC is packaged in a 100-pin QFN. Figure 13 shows the die micrograph of the 65nm CMOS IC along with its summary.

A. Setup

Measurements on the IC are performed using the Google Speech dataset [8]. The KeyRAM architecture from Section IV was trained for 7-way classification using 11k data samples each corresponding to a 1s keyword sampled at 16 kHz. The inputs to the classifier on the chip are 8-channel MFCCs extracted within 40 ms windows with 20 ms overlap resulting in a $8 \times 49$-dimensional feature vector ($K = 8$, $T = 49$). The input patch dimension at each glimpse is $8 \times 8$ ($P = 8$) and the locator is a one-dimensional scalar. Figure 14 shows the
Fig. 14. Measurement setup showing data transfer between the PC to the KeyRAM IC via a microcontroller (MCU).

TABLE III
MEASURED CLASSIFIER ACCURACY ACROSS GLIMPSES.

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<th>Glimpses ($n_G$)</th>
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<th>3</th>
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<tr>
<td>Accuracy [%]</td>
<td>60.58</td>
<td>72.12</td>
<td>83.65</td>
<td>90.38</td>
</tr>
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</table>

measurement setup used for testing the KWS IC. MFCC feature extraction of raw audio samples from the Google Speech dataset is performed on the PC. The microcontroller (MCU) transfers the MFCC glimpses from the PC to the IC, and the location and class scores from the IC to the PC. All KeyRAM parameters are stored on-chip. The total I/O requirements is 3.4 Mbps when operating at maximum throughput.

B. Decision Accuracy, Energy, and Latency

Figure 15 shows how the confidence of the classifier IC improves with the number of glimpses processed when the input sample corresponds to the label ‘off’. After two glimpses, the IC is unable to recognize the correct label, but with low confidence. By processing an extra glimpse, the IC makes the correct decision by assigning the label ‘off’ to the sample, and it does so with high confidence. Table III indicates that the measured classification accuracy of KeyRAM improves with the number of glimpses $n_G$ used per decision. Processing more glimpses makes the classifier more confident in its decisions, and hence improves its accuracy. When averaged over the test set, the measured classification accuracy is 90.38% at $V_{WL} = 0.7$ V with $n_G = 4$ glimpses.

The decision energy and latency linearly increase with $n_G$ (Fig. 16). Combined with a tunable WL pulse amplitude $V_{WL}$, the KeyRAM IC incorporates dynamic energy-accuracy trade-offs, e.g., the energy/glimpse varies from 0.19 µJ-to-0.21 µJ as $V_{WL}$ varies from 0.5 V-to-0.8 V. The measured energy breakdown (Fig. 17) shows that layers $f_3$ and $f_4$, which account for 89% of computations, consume 68% of the total energy consumption. These savings are attributed to the use of IMC. The CTRL energy (0.08 µJ/glimpse) gets amortized as the problem increases.

C. KeyRAM with CC Strategy

In Fig. 15, we notice that the classifier need not process the 4th glimpse as the confidence after the 3rd glimpse was very high. This provides some evidence that the CC strategy presented in Section III can be useful to minimize the energy. In this section, we investigate the efficacy of using this strategy.

Figure 18 plots the measured classification error and average energy per decision of KeyRAM with CC (KeyRAM-CC) while varying the threshold parameter $\tau$. The accuracy-energy trade-off is evident, as the average energy per-decision increases with $\tau$, for more glimpses per input sample $n_G$ are required on average, while the classification error generally decreases. For $\tau \geq 0.5$, the test error plateaus around 9.62%, which is the test error associated with a constant glimpse strategy ($n_G = N_G$).
with \( n_G = 4 \). Therefore, KeyRAM-CC achieves an accuracy equal to that achieved by the constant glimpse strategy while consuming \( \sim 2 \times \) less energy per decision on average.

Comparison with a digital architecture implementing a standard RNN with the same model size, Figure [19] shows a 4.1× savings in decision energy of which approximately 1.48× is attributed to the use of the KeyRAM algorithm using constant glimpse strategy with \( n_G = 4 \) and 2.74× is due to IMC. An additional 1.81× savings is achieved on average by employing the CC strategy (\( \tau = 0.5 \)) for a total of 7.3× savings in decision energy.

D. Comparison with Existing KWS ICs

Table [V] compares the KeyRAM IC with state-of-the-art digital [3–5], [7] and in-memory [6] KWS IC implementations. Table [V] shows that the proposed KeyRAM IC requires more MACs per classification compared to current KWS ICs in [3, 7]. The reason being that the KeyRAM IC processes a higher number of keywords (7) on a more challenging Google speech dataset as compared to [5] which considers 4 keywords from the simpler TIMIT dataset and [7] which processes only 2 keywords from the Google speech dataset. KeyRAM, using the CC strategy with \( \tau = 0.5 \), achieves 7.6× reduction in energy/decision compared to the IMC [6]. In addition, KeyRAM achieves > 24× reduction in the decision energy-delay product (EDP) compared to other KWS implementations. It also achieves the lowest reported decision latency of 39.9 µs.

VI. CONCLUSION

This paper illustrates the importance of algorithm-hardware co-design approach in minimizing the energy consumption and latency of decision-making systems in silicon. Specifically, adapting the RAM algorithm [11] from image classification to the KWS task provided \( \sim 2 \times \) reduction in energy-per-decision with no loss in accuracy and enabled on-chip storage of all weights. Combined with selective mapping of RAM layers to IMC [13] enabled this KWS IC to achieve a total of > 24× reduction in the decision-level EDP over SOTA. Such algorithm-hardware co-design approaches will be critical in other applications such as video inference as circuit and system designers seek to pervasively deploy AI-enabled semiconductors.

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Charbel Sakr is a PhD student at the University of Illinois working with Professor Naresh Shanbhag in the Coordinate Sciences Laboratory. He obtained his Engineering degree from the American University of Beirut in 2015 graduating with High Distinction. He then joined the University of Illinois and obtained his Masters degree in 2017 from the Electrical and Computer Engineering Department where he is now a PhD candidate. His research interests are in resource-constrained machine learning, with a focus on analysis and implementation of reduced precision algorithms and models.

Sujan K. Gonugondla received the Bachelor’s and Master’s in Technology degrees in Electrical Engineering from the Indian Institute of Technology Madras, Chennai, India, in 2014 and the Ph.D. degree in Electrical and Computer Engineering from the University of Illinois at Urbana-Champaign, Urbana, IL, USA in 2020. Since June 2020, he has been with Amazon, where he works as a Research Scientist. His research interests are in energy-efficient integrated circuits, and low complexity algorithms for machine learning systems, specifically algorithm hardware co-design for inference under resource-constraints.

Dr. Naresh R. Shanbhag received his B.Tech. (Indian Institute of Technology, New Delhi, 1988), M.S. (Wright State University, 1990), and his Ph.D. degree (University of Minnesota, 1993) all in Electrical Engineering. From 1993 to 1995, he worked at AT&T Bell Laboratories at Murray Hill where he was the lead chip architect for AT&T’s 51.84 Mb/s transceiver chips over twisted-pair wiring for Asynchronous Transfer Mode (ATM)-LAN and very high-speed digital subscriber line (VDSL) chip-sets. Since August 1995, he is with the Department of Electrical and Computer Engineering, and the Coordinated Science Laboratory at the University of Illinois at Urbana-Champaign, where he is presently a Jack Kilby Professor of Electrical and Computer Engineering. He was a visiting faculty at the National Taiwan University (August 2007-December 2007) and Stanford University (August 2014-December 2014). His research interests are in the design of robust and energy-efficient integrated circuits and systems for communications including VLSI architectures for error-control coding, and equalization, noise-tolerant integrated circuit design, error-resilient architectures and systems, and system-assisted mixed-signal design. He has more than 200 publications in this area and holds twelve US patents. He is also a co-author of the research monograph Pipelined Adaptive Digital Filters published by Kluwer Academic Publishers in 1994.

Naresh R. Shanbhag received the 2010 Richard Newton GSRC Industrial Impact Award, became an IEEE Fellow in 2006, received the 2006 IEEE Journal of Solid-State Circuits Best Paper Award, the 2001 IEEE Transactions on VLSI Best Paper Award, the 1999 IEEE Leon K. Kirchmayer Best Paper Award, the 1999 Xerox Faculty Award, the Distinguished Lectureship from the IEEE Circuits and Systems Society in 1997, the National Science Foundation CAREER Award in 1996, and the 1994 Darlington Best Paper Award from the IEEE Circuits and Systems Society. Dr. Shanbhag is serving as an Associate Editor for the IEEE Journal on Exploratory Solid-State Computation Devices and Circuits (2014-16), served as an Associate Editor for the IEEE Transaction on Circuits and Systems: Part II (97-99) and the IEEE Transactions on VLSI (99-02 and 09-11), respectively. He has served as the General Chair of the IEEE Workshop on Signal Processing Systems (2013), and the IEEE International Symposium on Low-Power Design (ISLPED 2012), the Technical Program co-Chair of the 2010 ISLPED, and served on the technical program committee of a number of conferences including the International Solid-State Circuits Conference (ISSCC, 2007-11). Dr. Shanbhag led the Alternative Computational Models in the Post-Si Era research theme, in the DOD and Semiconductor Research Corporation (SRC) sponsored Microelectronics Advanced Research Corporation (MARCO) center under their Focus Center Research Program (FCRP) from 2006-12. Since January 2013, he is the founding Director of the Systems On Nanoscale Information fabricS (SONIC) Center, a 5-year multi-university center funded by DARPA and SRC under the STArNet phase of FCRP. In 2000, Dr. Shanbhag co-founded and served as the Chief Technology Officer of Intersymbol Communications, Inc., a venture-funded fabless semiconductor start-up that provides DSP-enhanced mixed-signal ICs for electronic dispersion compensation of OC-192 optical links. In 2007, Intersymbol Communications, Inc., was acquired by Finisar Corporation, Inc.