Impact of DFE Error Propagation on FEC-Based High-Speed I/O Links

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***Abstract*—Modern state-of-the-art I/O links today rely exclusively upon a high SNR channel and an equalization-based inner transceiver to achieve a BER of 10^{-15}. The equalizer typically consists of a transmit pre-emphasis driver for pre-cursor equalization and a receive DFE for post-cursor cancellation. Recently, forward error-correction (FEC) coding has been proposed to improve the BER and reduce power in high-speed I/O links. However, error-propagation in the DFE is a significant issue affecting code performance. The link performance is also tied to FEC implementation parameters like degree of parallelism. This paper presents a framework for analyzing the impact of DFE burst errors and implementation parameters on end-to-end link performance. For $10.3125\mathrm{Gb/s}$ transmission through a channel with $19\mathrm{dB}$ loss at Nyquist rate and serial FEC implementation, we find that a code rate $r = 0.8$ gives the best ISI penalty vs coding gain trade-off, and a codeword length of 750 bits is necessary to meet target performance. Further, it is observed that the performance of burst error correction codes does not necessarily improve with codeword length, i.e., there is an BER-optimal block length at a given code rate.**

I. Introduction

High-speed serial links operating at multi-Gb/s data rates today suffer from inter-symbol interference (ISI) caused by the band-limiting traces that carry the data. These links operate under stringent specifications - few tens of Gb/s data rates, power efficiencies of the order of $10 - 30\mathrm{mW/Gb/s}$ and a BER target of 10^{-15} and lower. State-of-the-art links employ transmit pre-emphasis (PE) for pre-cursor equalization and receive decision feedback equalization (DFE) to cancel the post-cursor ISI. The IEEE/OIF standards for $6-12\mathrm{Gb/s}$ links specify transmit PE and DFE based transceivers for these links. Hence, they rely exclusively upon an equalization-based inner transceiver to achieve a BER of 10^{-15} [1] [2] [3]. In [4], for a fixed process technology node ($130\mathrm{nm}$), a four-fold increase in power is predicted when the data-rate is increased from $5-12\mathrm{Gb/s}$ to $25\mathrm{Gb/s}$ and higher. As energy scales linearly with process technology, it is predicted that a technology node of $32\mathrm{nm}$ is needed in order to meet the power budgets at these speeds. This clearly implies a need to explore alternative communication techniques to design power-optimal I/O links. Higher size constellations such as 4-PAM help bring down the bandwidth requirement, but are limited by the peak-SNR constraint imposed by a given technology [2] [5] [6].

We proposed [7] the application of forward error-correction (FEC) for multi-Gb/s links to reduce power and improve BER, and studied the pre vs. post-FEC BER improvements, and the power trade-offs involved for binary BCH codes. An evaluation of FEC codes within the standards-framework, i.e., utilizing existing redundancies in the transmitted packet, is presented in [8]. However, we take a broader view of the subject by employing FEC to partition the link design problem into one of designing a low-power high BER inner transceiver followed by a low-power FEC to reduce the BER to meet the specification. Coding provides a whole new range of design variables with which to optimize the link power consumption. For example, in ADC based receivers [9], FEC can potentially reduce the precision requirements resulting in significant power savings. FEC codes can also relax the specifications on the analog components of the links; for example, by enabling higher jitter-tolerance and hence improved resiliency to VCO phase noise. The other strong motivation for looking at FEC-based links is to enable I/O links governed by present day standards to meet performance specs under severe channel conditions. This can be done by nesting a PE-DFE based link in an outer FEC layer.

Past work has focused on link modeling for uncoded I/O links [4] [10]. Not much work has been done in analyzing the performance of FEC in the presence of correlated errors generated in a DFE-based I/O link. This paper focuses specifically on evaluating the performance of binary block codes in a DFE based link. Binary BCH codes offer good error correction at moderate to high code rates, making them an excellent candidate for designing FEC-based low-power I/O links. However, the DFE produces correlated errors because of error propagation, i.e., a decision error leads to bursts of errors. These error bursts become severe when the magnitude of a DFE tap is more than half the main tap (cursor). The impact of DFE errors is even more significant in an FEC-based system. The main contribution of this paper is to develop an accurate model for evaluating FEC for I/O links, and employing this model to evaluate the performance of random and burst error correcting codes for a real I/O link. A rigorous model is necessary, given the very low target BER unique to this

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application. The model consists of: 1) an accurate statistical estimate of the link specific noise sources such as residual ISI and timing jitter, 2) a Markov chain based DFE model to account for error-correlation, and 3) its extension based on the dynamic programming principle to compute random and burst error probabilities in codeword blocks. The fundamental interplay between the code-rate and performance is described in Section II. In the past [11], the effect of DFE error propagation has been modeled using a Markov chain based approach. This is reviewed in Section IV. This Markov chain model is used to compute two types of error statistics - random error and burst error. Based on this approach, the performance of a set of random error correcting codes (RECC) and burst error correcting codes (BECC) is evaluated in Section VI.

II. Forward Error-Control (FEC)

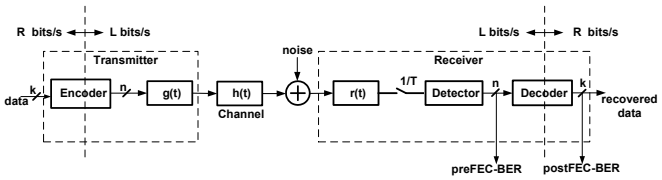

Fig. 1. An FEC-based high-speed I/O link.

The block diagram of an FEC-based I/O link is illustrated in Fig. 1, where the *inner transceiver* includes the shaping filter (e.g., pre-emphasis) $g(t)$ at the transmitter, the physical channel $h(t)$, the receive filter (e.g., equalizer or band-limiting low-pass filter) $r(t)$, followed by a baud-rate sampler and a detector (e.g., slicer). FEC is a well-known technique where blocks of data/information bits of length k (dataword) are mapped to blocks of code bits of length n (codeword) where $n > k$. Such a code is said to have a code-rate of $r = \frac{k}{n}$. If R is the data-rate in bits/s then an FEC link (or coded link) will have a line-rate $L = \frac{R}{r}$ which is greater than R. This is because a coded link needs to transmit redundant bits in addition to the data bits. For uncoded links, $L = R$. As the line-rate is greater than the data-rate, a coded link will suffer from increased ISI than an uncoded link and hence incur an *ISI penalty*.

The mapping from dataword to codeword is chosen such that the minimum Hamming distance (d_{min}) between any two codewords is maximized while the decoder complexity is minimized. Both of these properties are satisfied by linear codes. The error-correction capability of an (n, k, d_{min}) linear code is governed by d_{min} in that the maximum number of correctable errors $t = \lfloor \frac{d_{min}-1}{2} \rfloor$. Thus, a larger d_{min} results in greater error-correction capability and hence a greater *coding gain*, where the coding gain is the difference between the channel SNR of a coded and an uncoded link achieving the same BER.

Another trade-off inherent in the design of coded links is the constraint on d_{min} referred to as the Singleton bound: $d_{min} \leq n-k+1$. Thus, one way to achieve a large d_{min} is to reduce k as compared to n. Doing so will improve the coding gain but at the expense of the ISI penalty. This is because the code-rate $r = \frac{k}{n}$ will reduce thereby necessitating a higher line rate. A way around this problem is to increase the block/code-length n. This however will impact the latency of the design and the complexity of the encoder and decoder. Thus, coded links offer an interesting variety of trade-offs between power consumption, BER, and latency. For I/O links, we expect that the coding gain from specific types of codes will offset the ISI penalty with an acceptable latency and thereby result in a reduced power link.

III. FEC Architecture for High-speed I/O

High-speed serial I/O seeks to transmit incoming parallel data in a serial manner. Typically, a serializer based on a tree type architecture serializes the data in stages, and the received data is deserialized in stages at the receiver as shown in Fig. 2.

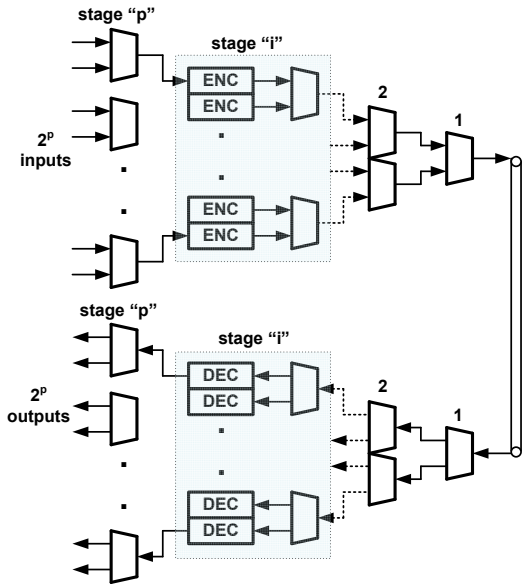

Fig. 2. FEC parallelization.

Given the limitations of technology, it is usually necessary to parallelize the FEC implementation so that the encoder and decoder run at achievable speeds. Besides, a parallel implementation, as shown in Fig. 2, exploits the serializer-deserializer architecture to achieve burst error correction. If each parallel channel is encoded with a t_{rand} random error correcting code, and there are M subchannels, the burst error correction capability $t_{burst} = t_{rand}M$. If encoding and decoding are implemented in stage-i_0 of the serializer and deserializer respectively, $M = 2^{i_0}$. A serial FEC implementation corresponds to $i_0 = 0$ i.e $M = 1$. Hence, there is an inherent trade-off between FEC speed of operation, burst error correction (hence performance), latency and power. The FEC performance evaluation method used in this paper can be used to analyze the implementation trade-offs mentioned above.

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IV. Modeling DFE Error propagation

A DFE cancels out ISI from past bits using past decisions. If a past decision is in error, it propagates in the feedback section for a number of baud periods equal to the DFE length (L_{DFE}). This phenomenon can be modeled using a Markov chain with memory L_{DFE}. The signal at the input to the slicer r_k is given by,

$$r_k = b_k + n_k^{random} + n_k^{dfe-ep} \quad (1)$$

$$n_k^{dfe-ep} = \sum (b_{k-m} - d_{k-m}) * h_m \quad (2)$$

where b_k and d_k are the transmitted and detected bits, respectively, n_k^{random} is the random noise component, n_k^{dfe-ep} is the error propagation component, and h_m are the channel coefficients.

It is assumed that DFE errors are the main source of error correlation i.e., all other noise sources such as residual ISI outside the DFE window, cross-talk, and timing jitter are lumped into one effective uncorrelated noise process. The distribution for n_k^{random} can be computed by convolving the individual noise distributions. An error pattern specifies the DFE error corresponding to the past L_{DFE} decisions. For example, in an M-PAM system with $M = 2$, symbols alphabet $[1, -1]$ and 2 DFE taps, the error patterns are $(-2, 0)$, $(-2, -2)$, $(-2, 2)$, $(2, 0)$, $(2, -2)$, $(2, 2)$, $(0, 2)$, $(0, -2)$, $(0, 0)$, leading to a total of $N_{states} = (2M - 1)^{L_{DFE}} = 9$ error-states. The notation E_k^i represents the DFE being at the i^{th} error-state ($i = 1, \ldots, N_{states}$) at time k. Fig. 3 depicts some of the transitions in the state transition diagram for a 2-tap DFE.

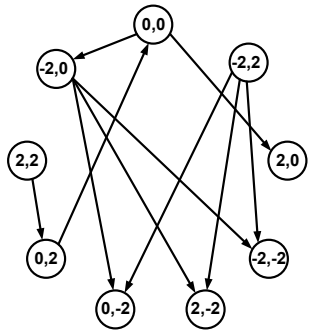

Fig. 3. Markov chain state transitions.

In Fig. 3, for example, a transition from error-state $(0, 0)$ to $(2, 0)$ occurs when the present error-state is $(0, 0)$, i.e., the present and previous decisions are not in error, and in the next symbol-period, a $d_k = 1$ decision is made when actually a $b_k = -1$ was transmitted resulting in error magnitude $1 - (-1) = 2$. Note that in our notation for the error-state, the left value is the most recent. The state transition probabilities $Pr(E_k^i | E_{k-1}^j)$ and steady state probabilities $Pr(E_k^i)$ are given as,

$$Pr(E_k^i | E_{k-1}^j) = \sum_{b_k} Pr(E_k^i | E_{k-1}^j | b_k) * Pr(b_k) \quad (3)$$

$$Pr(E_k^i) = \sum_j Pr(E_{k-1}^j) Pr(E_k^i | E_{k-1}^j) \quad (4)$$

where, $Pr(E_k^i | E_{k-1}^j | b_k)$ can be obtained once the distribution of n_k^{random} is known. The Markov chain model described in this section is validated by comparing the error pattern probabilities predicted by theory with those obtained by simulation. This comparison, shown for a synthetic channel with taps [1 0.5 0.3 0.2 0.1], a 4-tap DFE, transmit symbols [1 -1] and noise variance 0.1 is shown below in Table I. This clearly illustrates excellent agreement between the two.

TABLE I
Markov Model Validation

Error Pattern	log(Pr)-th. (theory)	log(Pr)-sim. (simulated)
0(0000)	-0.0015	-0.0015
1(0001)	-3.1066	-3.1061
2(0010)	-3.2265	-3.2249
3(0011)	-3.7037	-3.7033
4(0100)	-3.2257	-3.2242
5(0101)	-4.5233	-4.5171
6(0110)	-3.7088	-3.7089
7(0111)	-5.5332	-5.4949
8(1000)	-3.1066	-3.1061
9(1001)	-5.0387	-4.9747
10(1010)	-4.508	-4.5031
11(1011)	-6.2165	-6.1549
12(1100)	-3.7060	-3.7055
13(1101)	-5.7747	-5.7696
14(1110)	-5.5332	-5.4949
15(1111)	-6.3904	-6.3010

V. Evaluating FEC performance

The Markov chain model described in the previous section can be used to determine error statistics over codeword blocks. Two kinds of statistics are of interest - random and burst. The former are of interest while evaluating the performance of random error correcting codes. The broad class of binary cyclic codes falls under this category. Another class of codes are designed to correct burst or correlated errors. A subclass of cyclic codes called Fire codes and codes designed in higher Galois fields belong to this category. As it is not feasible to perform simulations at the low BER region (10^{-15}) of interest, it is necessary to accurately model the channel error statistics to get a good estimate of FEC performance. In this section, we describe a method to compute error statistics using a trellis-based approach based on the dynamic programming principle.

A. Random Error Correcting Code (RECC)

The discussions that follow apply to 2-PAM modulation but can be extended easily to higher constellation sizes. For the specific case of 2-PAM and $L_{DFE} = 2$, the state machine depicted in Fig. 3 can be reduced by defining a composite state (i, j), where $i, j = 1$ and $i, j = 0$ imply the presence

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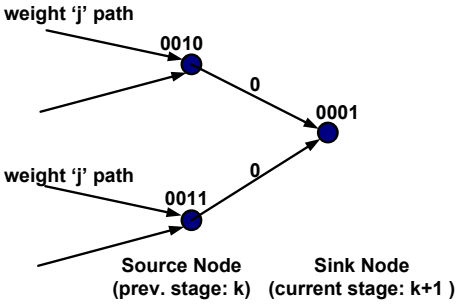
or absence of an error, respectively. The following equations describe the process:

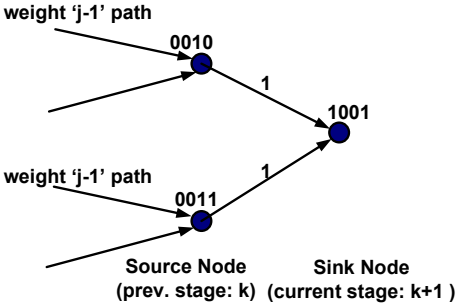
$$\begin{aligned} Pr(1,1) &= Pr(-2,2) + Pr(-2,-2) \\ &+ Pr(2,-2) + Pr(2,2) \quad (5) \\ Pr(1,1|1,0) &= Pr(-2,-2|1,0) + Pr(-2,-2|1,0) \\ &+ Pr(2,-2|1,0) + Pr(2,2|1,0) \quad (6) \\ Pr(-2,-2|1,0) &= Pr(-2,2|2,0) * Pr(2,0|1,0) \quad (7) \end{aligned}$$

where $Pr(1,1)$ is the probability of two successive bits being in error, (6) is employed to to reduce the number of states to $2^{L_{DFE}}$ from $3^{L_{DFE}}$ by discarding information regarding the exact error values in the state definitions and retaining information about whether or not a bit was in error, and (7) illustrates how each term on the RHS of (6) can be computed.

Figures 4(a) and Fig. 4(b) illustrate one section of the trellis used to perform recursive computation of the statistics involved when $L_{DFE} = 4$. Each composite state in the trellis represents a certain sequence of errors in the past L_{DFE} decisions. In the following, we will use the term 'state' to refer to the composite error-state. The random error weight



(a)



(b)

Fig. 4. Trellis paths of weights j.

probabilities are updated at each trellis stage as follows - If the error bit at stage $k+1$ is 0 (Fig. 4(b)),

$$Pr_j^{k+1}(i) = Pr_j^k(to(i,1)) + Pr_j^k(to(i,2)) \quad (8)$$

If the error bit at stage $k+1$ is 1 (Fig. 4(a)),

$$Pr_j^{k+1}(i) = Pr_{j-1}^k(to(i,1)) + Pr_{j-1}^k(to(i,2)) \quad (9)$$

where, $to(i,1)$ and $to(i,2)$ denote the two states leading to state i. $Pr_j^k(i)$ denotes a k bit long path of weight j that passes through state i.

B. Burst Error Correcting Code (BECC)

A burst error is defined by the difference in position between the first error and the last in a codeword block. For example, a burst of length j has its first error at position k and the last error $k+j-1$ bits later. To compute the burst error statistics, we define the event $B_j^k(i)$ as the event that a k bit path ends in state i and has burst length j. $Pr_j^k(i)$ denotes the probability of that event. In order to compute burst pattern probabilities, we also keep track of the event that an error burst that begins at stage m in the trellis, passes through state i at stage k (denoted as $B_{beg-m}^k(i)$).

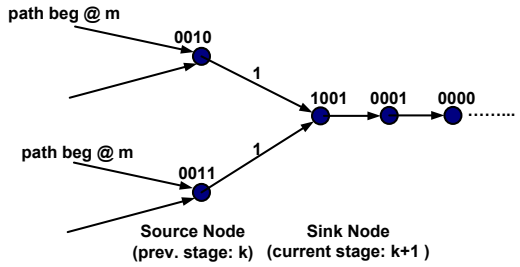


Fig. 5. Trellis paths of burst length j.

The probabilities for error events beginning at a stage m in the trellis are updated as,

$$\begin{aligned} Pr_{beg-m}^{k+1}(i) &= Pr_{beg-m}^k(to(i,1))Pr(to(i,1) \rightarrow i) \\ &+ Pr_{beg-m}^k(to(i,2))Pr(to(i,2) \rightarrow i) \quad (10) \end{aligned}$$

where the terms $Pr(to(i,1/2) \rightarrow i)$ are the transition probabilities leading to state i, and $Pr_{beg-m}^k(i)$ is the probability of the event $B_{beg-m}^k(i)$. At each trellis stage, the error-burst probabilities are updated based on events that have their last error in a codeword in *that* stage. Equation (11) governs this update. If new error bit is 1 (Fig. 5),

$$Pr_j^{k+1}(i) = Pr_{beg-(k+2-j)}^{k+1}(i)Pr(i,0,0,0...0) + Pr_j^k(i) \quad (11)$$

where, $Pr(i,0,0,0...0)$ is the probability of starting at state i at stage k and observing 0s for the remaining part of the codeword. Equations (8), (9) and (11) are used to estimate the bit error rate (BER) according to Equation 12.

$$BER = \sum_{j=t+1}^{n} Pr(j) * \frac{j}{n} \quad (12)$$

We note here that by using the basic Markov model for the DFE and developing a recursive equation connecting error statistics at stage $k+M$ to that at stage k, we can easily analyze the implementation trade-offs mentioned in Section III. Clearly, in (8), (9) and (11), $M = 1$.

C. Error Statistics for an AWGN Channel

The random and burst error evaluation model has been verified by comparing random error weight and burst length

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probabilities through analysis and simulation upto an error probability of 10^{-5} for the synthetic channel considered in Sec. IV. A strong agreement between analysis and simulation is inferred from Table II.

TABLE II
VALIDATION OF ERROR PATTERN STATISTIC COMPUTATION

Errwt/ Burst	log(Pr)-th. random	log(Pr)-sim. random	log(Pr)-th. burst	log(Pr)-sim. burst
1	-1.5695	-1.5659	-1.5739	-1.57
2	-1.9578	-1.9502	-2.043	-2.0495
3	-3.2211	-3.1692	-2.8531	-2.8511
4	-3.9936	-4.0114	-3.3968	-3.3951
5	-5.0903	-5.0706	-3.8486	-3.8083
6	-6.0251	N/A	-4.0844	-4.0122
7	-7.0635	N/A	-4.3835	-4.3444
8	-8.0602	N/A	-4.5253	-4.5465
9	-9.0894	N/A	-4.5782	-4.5613
10	-10.1130	N/A	-4.603	-4.622
11	-11.1492	N/A	-4.6178	-4.6176
12	-12.1888	N/A	-4.63	-4.6258
13	-13.2356	N/A	-4.6413	-4.7224
14	-14.2876	N/A	-4.6526	-4.7368
15	-15.3456	N/A	-4.6641	-4.6511

In this section we focus our attention on the error characteristics of a typical I/O channel, isolating the ISI penalty vs coding gain trade-offs that complicate the FEC evaluation process. To do this, we consider a 7.5Gb/s (fixed) *channel rate* transmission across a channel measured to have a 15dB loss at Nyquist frequency. A 5-tap DFE is assumed. White Gaussian Noise (WGN) is added at the channel output and error probabilities for a 50 bit code block at the slicer output are evaluated. Both random ($errwt > w$, $w = (3, 5, 7, 9)$) and burst error statistics ($burst > l$, $l = (3, 5, 7, 9)$) are computed and plotted in Fig. 6.

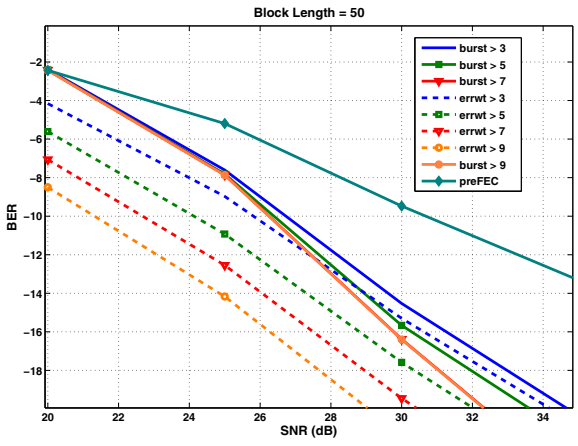

Fig. 6. Error statistics in 50 bit block.

Figure 6 indicates that weight 3 errors are predominantly burst errors, particularly at high SNR. This is inferred from the curves for $errwt > 3$ and $burst > 3$ which are close to each other. The burst length distribution is relatively uniform beyond this length. This explains why the burst error rate drops slowly as l is increased. For random errors, there is a significant distribution of events for the values of w considered in Fig. 6. This is reflected in the rapidly diminishing error rates in this case.

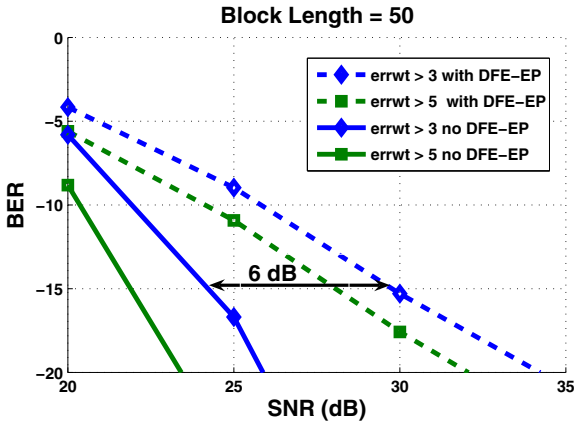

Fig. 7. Effect of error propagation.

Fig. 7 illustrates the effect of DFE error propagation. The two plots in dashed lines are based on error statistics in a codeword of length 50. The two plots in continuous lines are under the assumption that the transmitted bits are used at the DFE i.e there is no error propagation. At $BER = 10^{-15}$, the figure illustrates an SNR loss of 6dB due to error-propagation. This clearly illustrates the potential benefits that interleaving, a technique that augments FEC capability and TX pre-coding, a technique that mitigates error-propagation effects can offer.

VI. RESULTS

In this section, we present the results of evaluating the performance of a set of random and burst correcting codes. This evaluation accounts for the ISI penalty vs coding gain trade-off by fixing the *data rate* to 10.3125Gb/s and evaluating FEC peformance at the corresponding channel rate. The channel is measured to have a 19dB loss at Nyquist frequency. The codes evaluated are listed in Table III. The transmit swing is fixed at 1200mV p-p. The distribution of the link noise sources like residual ISI and timing jitter are convolved to obtain an effective noise distribution. The TX introduces 1ps rms random jitter and 4ps duty-cycle-distortion (DCD), while the RX adds 1.4ps random jitter and 4ps DCD. The RX bandwidth was set at $6 - 7\text{GHz}$. These numbers were obtained from SPICE characterization of the circuits involved in 65nm CMOS. A 5 tap DFE resulting in a uncoded link BER $= 10^{-8}$ is used in the analysis. The RECC chosen are binary BCH codes ($n = 2^m - 1$) while the BECC are Fire codes [12] or interleaved Fire codes.

The performance evaluation results for different codes is partitioned into the two plots in Fig. 8 and Fig. 9. The BER is plotted as a function of the block length, with code-rate (r) as a parameter. Fig. 8 zooms in on the region where the post-FEC BER is worse than the uncoded link-BER. In this region, the performance degradation due to ISI penalty exceeds the coding gain. The $r = 0.88$ and $r = 0.64$ curves show

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TABLE III
CODES EVALUATED

Code Rate	Code						
	Random Error				Burst Error		
0.96		255,2	511,2	750,3	279,5	558,10	1116,20
0.88	127,2	255,4	511,7	750,10	105,4	210,8	315,12
0.80	127,4	255,6	511,11	750,15	35,3	70,6	105,9
0.64	127,6	255,12	511,21	750,28			

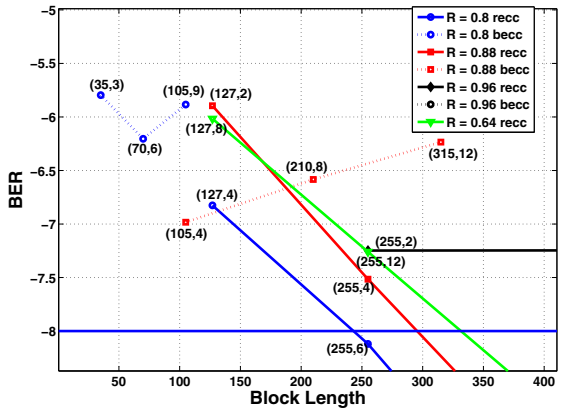

Fig. 8. Performance evaluation of block codes.

worse performance than $r = 0.8$. Of the three code-rates, $r = 0.8$ is optimal. Two distinct trends emerge for RECC and BECC performance. For RECC, the increased codeword length implies higher t and higher code-rate r for a given t. The increase in t outweighs the increase in the number of error events of a given weight, resulting in improving performance with higher n. For example, as we go from RECC $(127, 4)$ to $(750, 15)$ performance improves monotonically. For BECC however, there is an optimal block length. At this block length, the burst error correction capability is matched to the channel burst characteristics, determined by the DFE length. For higher n, the random noise source causes uncorrectable bursts that increase faster than the burst correction capability.

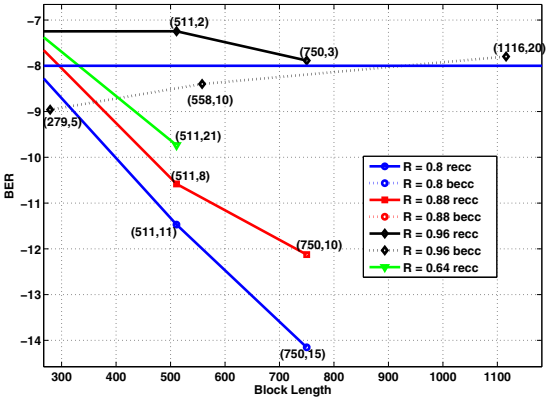

Fig. 9. Performance evaluation of block codes.

For example, as we move from a $(35, 3)$ through $(70, 6)$ to a $(105, 9)$, an optimal is reached at the $(70, 6)$ code. From Fig. 9, it is evident that a codeword length of 750 or more is necessary to meet $BER = 10^{-15}$ for this channel. Simple burst correction codes are not sufficient to meet the performance requirements. While the codes considered so far have been exclusively RECC or BECC, interleaving RECC enables us strike a balance between random and burst error correction. The methodology described in this paper can be easily extended to analyze this systematically.

VII. CONCLUSION

A method to accurately model the effects of DFE error propagation on FEC performance in high-speed serial links is presented. The method first derives the state machine representing the DFE and uses this to compute codeword random and burst error statistics. Two distinct trends were observed for RECC and BECC. The performance of the former improved monotonically with n, whereas the BECC showed best performance at a certain optimum codeword length.

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REFERENCES

[1] N. Krishnapura and M. Barazande-Pour, "A 5 Gb/s NRZ transceiver with adaptive equalization for backplane transmission," in *International Solid-State Circuits Conference*, 2005.

[2] J. Zerbe *et al.*, "Equalization and clock recovery for a 2.5-10 Gbps 2-PAM/4-PAM backplane transceiver cell," in *International Solid-State Ciruits Conference*, 2003.

[3] J. E. Jaussi, G. Balamurugan, D. Johnson, B. Casper, A. Martin, J. Kennedy, N. Shanbhag, and R. Mooney, "8 Gb/s source-synchronous I/O link with adaptive receiver equalization, offset cancellation and clock de-skew," *IEEE Journal of Solid State Circuits*, vol. 40, no. 1, pp. 80–88, 2005.

[4] V. Stojanovic, "Channel-limited high-speed links: modeling, analysis and design," Ph.D. dissertation, Stanford University, U.S.A, 2004.

[5] R. Farjad-Rad, C.-K. K. Yang, M. Horowitz, and T. Lee, "A 0.3 micron CMOS 8 Gbps 4PAM serial link transceiver," *IEEE Journal of Solid State Circuits*, vol. 35, no. 5, pp. 757–764, 2000.

[6] J. T. Stonick, G.-Y. Wei, J. L. Sonntag, and D. K. Weinlader, "An adaptive PAM-4 5 Gbps backplane transceiver in 0.25 micron CMOS," *IEEE Journal of Solid State Circuits*, vol. 38, no. 3, pp. 436–443, 2003.

[7] R. Narasimha and N. R. Shanbhag, "Forward error correction for high-speed I/O," in *Asilomar Conference on Signals, Systems and Computers*, 2008, pp. 1513–1517.

[8] A. Szczepanek, I. Ganga, C. Liu, and M. Valliappan, "10GBASE-KR FEC tutorial," Website, http://www.ieee802.org.

[9] M. Harwood *et al.*, "A 12.5 Gb/s SerDes in 65nm CMOS using a baud-rate ADC with digital RX equalization and clock recovery," in *IEEE International Solid-State Circuits Conference*, 2007.

[10] V. Stojanovic and M. Horowitz, "Modeling and analysis of high-speed links," in *Custom Integrated Circuits Conference*, 2003, pp. 589–594.

[11] J. Ashley, B. M. M. Blaum, and C. Melas, "Performance and error propagation of two DFE channels," *Magnetics, IEEE Transactions on*, vol. 33, no. 5, pp. 2773–2775, 1997.

[12] R. E. Blahut, *Algebraic Codes for Data Transmission*. Cambridge University Press, 2003.

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