

DSP-based Multimode Signaling for FEXT Reduction in Multi-Gbps Links

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Abstract

In order to alleviate the problem of far-end crosstalk induced jitter, signaling techniques based on exploiting the orthogonal property of fundamental transmission modes of multiline system have been proposed, but so far there have been no reports on practical transceiver realization for systems other than for the ones with completely degenerate channels. In this paper, a DSP-based implementation of a multimode transceiver for a bundle of chip-to-chip microstrip lines is investigated in terms of its jitter suppression performance versus design complexity and power.

I. Introduction

In today's high-speed chip-to-chip communication, off-chip interconnect bandwidth is increasingly becoming the system bottleneck. In order to keep up with the data throughput needed, high edge rates are being used for signaling and the interconnects are being routed at an increased density. However, this also increases the electromagnetic coupling between the lines, resulting in augmented levels of both near-(NEXT) and far-end crosstalk (FEXT). In particular, for most parallel-terminated microstrip interconnects, FEXT is the dominant noise source, causing crosstalk-induced jitter (CIJ). This in turn limits the system performance and enforces the data rates to be well below the Shannon limit of the channel capacity [1]. Various approaches have been suggested in order to mitigate the effects of FEXT, including channel coding [1], [2], active cancelation [3], adaptive equalization [4], and crosstalk-aware channel design [5], but at the expense of area overhead, power or design complexity.

A promising signaling scheme for dense interconnects called *multimode signaling* was suggested by [6], which takes advantage of the multiconductor transmission line theory [7] to encode the parallel signals as the linear combination of fundamental transmission modes. Due to mode orthogonality, the signals are decoupled; such signaling is theoretically free of crosstalk, and therefore could allow the data transfer at channel capacity. It has been demonstrated [8] that this method allows line spacing similar to conventional differential signaling for the same performance, with the density of a single line per signal. However, the issue of practical realization of the encoder/decoder system for a general channel remains open. For a completely degenerate multiconductor transmission line system (e.g. stripline), an implementation using analog circuits was suggested in [9]. The complexity of such a system for non-degenerate channels (e.g. microstrip) would grow quadratically with the number of signals [10], forcing the bus to be divided into bundles, thus limiting the usability of the multimode signaling technique. In this paper, we analyze the feasibility of implementing the multimode encoder in the digital domain, in order to take advantage of the power and throughput benefits provided by the scaling down of CMOS technology.

II. Example Channel and Encoder/Decoder

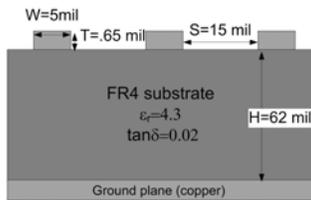


Figure 1. Cross-section of the multiconductor channel

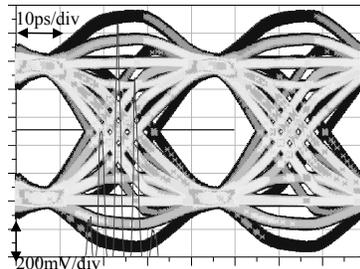


Figure 2. Eye diagram and jitter histogram using uncoded single-ended signaling

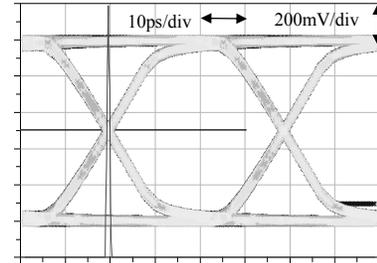


Figure 3. Eye diagram and jitter histogram with multimode signaling

To analyze the tradeoffs associated with the digital encoder design, an example multiconductor transmission line system has been set up in a form of three strongly coupled microstrip lines on FR4 substrate; the physical dimensions are as shown in Fig. 1. Line length was chosen to be 2 inches at the data rate of 12.8Gb/s, in order to ensure FEXT was the dominant noise source (as opposed to the inter-symbol interference (ISI), channel dispersion and attenuation). Matrices of impedance and admittance per unit

length, \mathbf{Z} and \mathbf{Y} , were first extracted using a quasi-static 2-D EM solver. Next, assuming that the channel loss is low compared to the reactive effects, encoder \mathbf{T} and decoder \mathbf{S} matrices were obtained following the well-known method [11] for diagonalizing \mathbf{ZY} and \mathbf{YZ} using frequency independent associated eigenvectors, thus achieving the total decoupling of the telegrapher's equations for the system. Note that, for this experimental setup, voltage signaling was chosen, however the same principles would still hold in the case of current-based signaling, which may be more suited to particular applications. From the characteristic impedance matrix \mathbf{Z}_C of the system, an appropriate resistive matching network was constructed to parallel-terminate the lines at the far end and minimize reflections, thus reducing ISI and FEXT¹.

To explore the potential gains that could be obtained by multimode signaling, the encoder and decoder were initially implemented as ideal. The lines were first excited by uncoded single-ended PBRs sequences of length $2^{10}-1$, with rise and fall times of 45 ps. The eye diagram and jitter histogram of the received signal on the central line are plotted in Fig. 2, clearly showing a five-modal distribution with peak-to-peak jitter J_{pp} of 37 ps. Next, the same input sequences were applied to the system with the encoder/decoder in place, resulting in the eye diagram and jitter histogram as plotted in Fig. 3. As expected, the CIJ is significantly reduced, with residual J_{pp} of 4.5 ps attributed to the effect of frequency-independent terminations [11].

III. DSP-based Transmitter Requirements

This section will discuss some of the issues connected with a DSP-based implementation of a multimode transmitter. The digital implementation of the encoder was proposed in [12], however there are practical issues with either of the two suggested methods. If the signals to be sent from the transmitter are in analog form, the digital processing block would have to perform sampling and processing at a Nyquist rate in order to preserve the signal shape. In case of a high-speed transmitter with a multi-Gb/s data rate, the digital block would have to run at a prohibitively high frequency, both from speed and power standpoint. However, in case of binary NRZ signaling this is also unnecessary, because the information to be transmitted is in essence digital, therefore we can assume that the digital block has at its inputs the digital bits (for example, obtained by a 1-bit slicer).

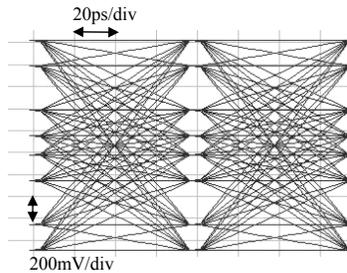


Figure 4. Transition diagram for ideal multimode signaling at line near-end

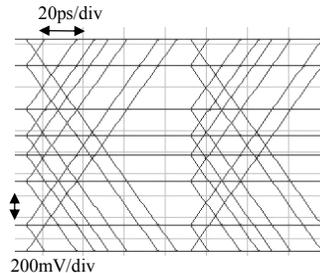


Figure 5. Transition diagram for an ideal slew-rate limited DAC

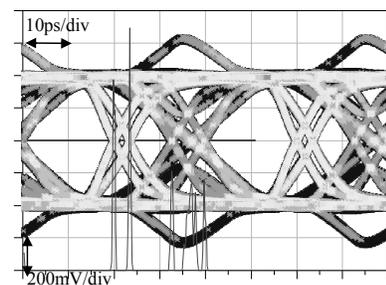


Figure 6. The effect of incorrectly generated analog transitions on multimode signaling

In case of digital information to be encoded, a simple DSP block performing matrix multiplication is not sufficient, due to the inherently analog nature of the multimode signaling. Let us revisit the ideal scenario from Section II. Assuming that the input word consists of three signals with equal rise and fall times t_r (in this example 75 ps), the linear combination of the three signals will also transition from the previous state in time t_r , regardless of the actual calculated values, as shown on the transition diagram in Fig. 4. On the other hand, the digital encoder performing matrix multiplication sends the new modal voltage values to the D/A converters at each bit interval. Modeling the D/A converter and line driver as being limited only by the slew rate of the driver, it is clear that the transition time on each line will depend on the previous and new voltage values, as shown in Fig. 5. In the modal space, this causes the decoded signals to exhibit different rise/fall times, or to change the slope during transition, all resulting in deviations from the orthogonal transmission modes and CIJ which is increased by a factor of 2 even compared to the uncoded case, as shown in Fig. 6.

In order to control the transition time and preserve the modal content of the coded signals, one option is to digitally control the slew rate of output drivers, by adjusting the biasing current depending on the previous and current transmitted bits. The physical realization of this can vary depending on the driver layout; one possible implementation would be to use a combinational network to multiplex the appropriate

¹ For this theoretic exploration, a fully matched resistive network was implemented. Depending on the system complexity and the amount of reflections that can be tolerated, a simpler M-terminating network or a parallel termination to ground may also be chosen.

current for each output symbol to be sent. The system diagram is shown in Fig. 7. Due to multi-Gb/s data rate, it's expected that deserialization of the data stream before data processing will be necessary.

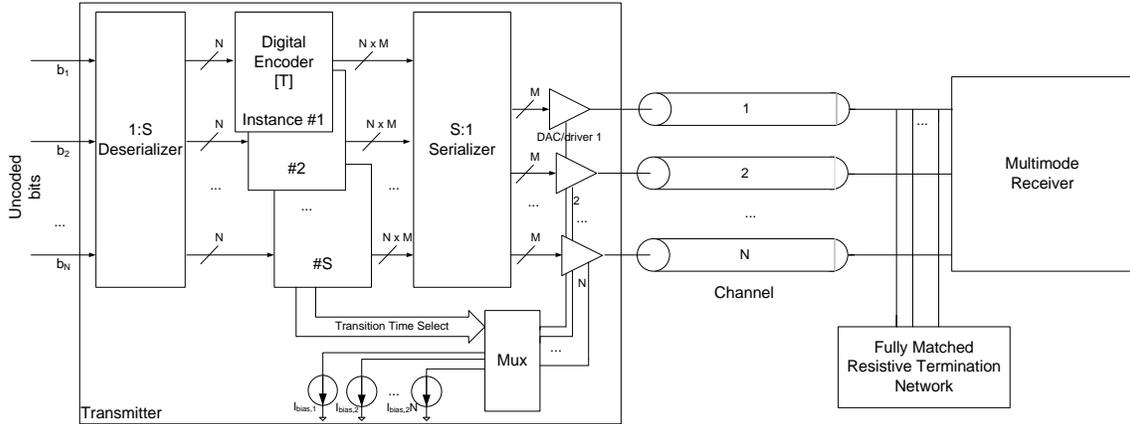


Figure 7. Block diagram of the proposed DSP-based transmitter system

In general, for a N -line system there exist N fundamental modes of propagation, and each line is driven by a linear combination of N input signals. In the case of digital input signals, there are 2^N values possible as the inputs to each D/A converter (refer to Fig. 4 for the case $N=3$). However, the exact values are in general nonuniformly spaced, and furthermore are functions of the physical configuration of the channel (since the encoder matrix T is derived from the Z and Y parameters p.u.l.). Therefore, instead of designing a N -bit DAC with nonuniform output levels for each line of the channel (and to investigate the finite resolution of adders and multipliers in the DSP block as well), it is assumed that the output DAC's are M -bit with uniform output levels, where $M \geq N$.

In order to determine the required resolution M of the DSP block, a series of simulations in Agilent's ADS/Ptolemy mixed-signal environment was next performed with different values of M , observing the jitter of the received decoded signals. As expected, choosing $M=N=3$ resulted in only a moderate jitter reduction to $J_{pp}=29$ ps (22% improvement compared to the uncoded signal transmission), due to the coefficients and generated voltages deviating from their ideal values, as shown in Fig. 8. Increasing the value of M helps better approximate the ideal transition levels, with $M=5$ improving CIJ by 70% compared to the uncoded case, as shown in Fig. 9. A plot of the RMS and peak-to-peak jitter values reveals the exponential improvement to both metrics with increasing resolution, with the ideal values being approached rapidly, as shown in Fig. 10. However, increasing the resolution adds to encoder area, design complexity and ultimately transmitter power, so a compromise must be made depending on the overall specifications of the system being designed.

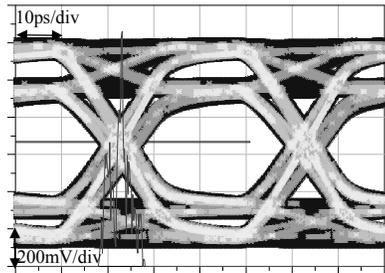


Figure 8. Eye diagram and jitter histogram of the decoded received signal for the case $N=3, M=3$

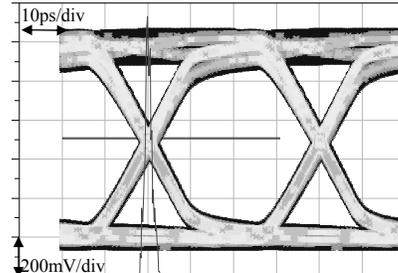


Figure 9. Eye diagram and jitter histogram of the decoded received signal for the case $N=3, M=5$

IV. Power Budgeting of the Digital Block

To explore the feasibility of the digital transmitter, the power of the DSP system (including the serializer/deserializer, but excluding ADC/DAC) was estimated for various combinations of number of lines N and DSP resolution M . For the assumed data rate of 12.8 Gb/s per line in 0.18 μm CMOS technology, serialization factor S of 16 was assumed. With no pipelining, the digital core runs at 800 Mb/s. In each DSP block, there are N additions of M -bit numbers for each of N channels. The main critical path delay is dominated by 1-bit adders. To achieve the required delay of 1.25 ns, the unit 1-bit full adder is first

scaled so that its delay does not exceed $1.25/(N \cdot M)$ ns, and its power P_{IFA} was extrapolated accordingly. Assuming the multiplier (1-bit AND gate) power P_{IAND} to be approximately $\frac{1}{4}$ of P_{IFA} , and with total serializer/deserializer power estimated at $P_{serdes}=100\text{mW}$ for every bit, the total DSP power is then:

$$P_{DSP} = S \cdot (P_{mult} + P_{add}) + N \cdot P_{serdes},$$

$$\text{where: } P_{mult} = N^2 \cdot M \cdot P_{IAND}, \quad P_{add} = N \cdot \log(N) \cdot M \cdot P_{IFA}$$

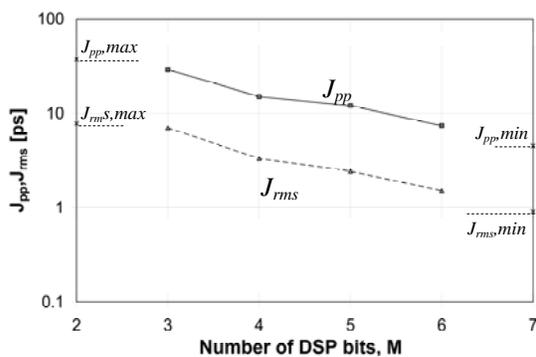


Figure 10. Jitter as a function of DSP precision M ; uncoded (maximum) and ideal (minimum) limits also shown

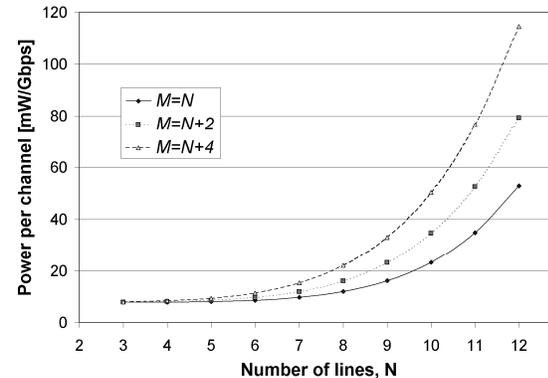


Figure 11. Estimated power of the DSP Tx block as a function of number of lines N and DSP precision M (normalized to 1 Gb/s)

The power consumption of the transmitter's digital core per Gb/s is shown in Fig. 11, for various combinations of the number of lines N and DSP precision M . As expected, for low values of N the dominant factor is the serializer/deserializer power, while with increasing N the power grows quadratically with the number of lines, eventually limiting the bundle size. Increasing the number of DSP bits also adds to the power, but not as drastically, and its effect could be minimized with custom DAC levels for each line. A DSP-based receiver is estimated to have comparable levels of performance and complexity.

V. Conclusion

Based on an example three-line microstrip conductor channel exhibiting strong coupling, the tradeoffs inherent in a DSP-based transmitter for multimode signaling have been investigated. Depending on the target level of jitter, the transmitter power for bundle sizes of up to 10 lines is comparable to the 25mW/Gbps achieved by XTC equalization [4], with a greater level of FEXT cancellation and with $\frac{1}{2}$ of the line density, but with no pre-emphasis and therefore shorter line length range. A fairer comparison with existing FEXT equalization solutions and a more universal encoding system could be achieved by shaping the transmitted waveform to mitigate ISI as well. Due to its mainly digital nature, this implementation is expected to take advantage of the power and performance benefits that the advanced submicron technology nodes provide.

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