Dual-Sampling Skewed CMOS Design for Soft-Error Tolerance

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***Abstract*—Presented is a circuit technique that mitigates the impact of single-event transient (SET) in deep submicrometer circuits with minimal speed, power, and area penalty. The technique combines a novel dual-sampling flip-flop (DSFF) and the skewed CMOS (SCMOS) circuit style. The DSFF and SCMOS are designed to eliminate SETs with the polarity of $1 \rightarrow 0$ and $0 \rightarrow 1$, respectively. We study inverter chain circuits as well as sum-of-products implementation of random logic circuits in a typical 0.18-μm process under the influence of radiation induced soft errors. We quantify the SET tolerance of the proposed technique by using an error map and a recently developed tool soft-error rate analyzer (SERA). The results show that the DSFF incurs no speed penalty, if no SETs have reached the input of DSFF. Otherwise, the DSFF alone eliminates the $1 \rightarrow 0$ SETs while incurring a worst case speed and power penalty of 310 ps and 39 μW, respectively. The SCMOS eliminates the $0 \rightarrow 1$ SETs when the skewing factor is greater than four. Thus, the proposed technique potentially eliminates the impact of SETs with both polarities.**

***Index Terms*—Combinational logic circuit, flip-flop, integrated-circuit reliability, latch, single-event transient (SET), soft-error rate (SER).**

I. Introduction

SOFT errors are radiation-induced transient errors caused by neutrons generated from cosmic rays and alpha particles from packaging material [1]. Soft-error protection is very important for enterprise computing and communication applications since the system-level soft-error rate (SER) has been rising with technology scaling and increasing system complexity [2].

A radiation event causes soft errors via two effects: single-event upset (SEU) and single-event transient (SET), as illustrated in Fig. 1. An SEU occurs in a memory cell or a flip-flop (FF) in its hold state when the contents of the storage element are flipped. An SET generates a transient noise pulse in a combinational circuit that may propagate to a FF input and manifest as a bit error. Prior work has shown that the soft errors, if uncorrected, result in a failure rate higher than all the other reliability mechanisms combined [3]. Results in [4] show that nearly 90% of the SER at a center bit of an 8×8 array multiplier is contributed by SETs originated from inside the combinational circuit. Error-tolerance has been stated as one of the key design challenges in International Technology Roadmap for Semiconductors (ITRS) 2003. It is vital to develop soft-error tolerant design techniques.

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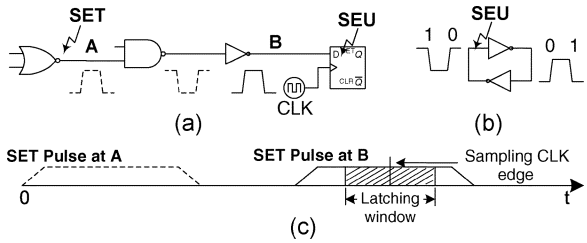

Fig. 1. Illustration of: (a) SET and SEU, (b) SEU in the storage element of a FF, and (c) timing diagram for propagation and capture of an SET.

Associated power and performance overheads are the biggest barriers to the adoption of classical fault tolerance techniques for soft-error protection. These techniques include chip-level duplication used in HP-Tandem machines [5], block-level duplication used in IBM Z-Series machines [5], and triple modular redundancy (TMR) [6]. Circuit level hardening techniques such as dual-interlocked storage cell (DICE) [7] protects the data from SEU only and does not help in mitigating soft errors caused by SETs. The dual-port gate (DPG) technique [8] mitigates both SEU and SET but would require a process that supports isolated body contacts. The transistor sizing technique described in [9] can reduce the SER of combinational logic circuits by selectively sizing the most sensitive nodes. The temporal sampling latch (TSL) proposed in [10] mitigates SETs by using latch-level TMR and time redundancy. It exploits the fact that a radiation induced SET has a pulsewidth typically less than a fixed value $\tau_{\max}$ (assumed to be 200 ps in [10]). The large power and area overheads caused by the redundant latches and the four phase clock would make multi-gigahertz designs complex and tricky. The three-input majority gate not only introduces additional delay in the data path but also causes glitching (dynamic hazard) at the output of the TSL due to the voting mechanism with delayed clocks even if there are no soft errors, which in turn translates into increased dynamic power consumption in TSL and in the subsequent logic circuits.

This brief presents a simple and robust circuit design technique that mitigates the effect of SET with minimal speed, area and power penalty. The technique combines a novel dual-sampling FF (DSFF) and skewed CMOS (SCMOS) combinational circuit to mitigate the impact of SETs with either polarity. The DSFF eliminates any $1 \rightarrow 0$ SETs while introducing a timing penalty that is slightly more than the maximum SET pulsewidth $\tau_{\max}$. The SCMOS can be tuned to eliminate $0 \rightarrow 1$ SETs. We show case studies of inverter chain circuits and sum-of-products implementation of logic circuits in a typical 0.18-μm process under the influence of radiation induced soft errors. The SET tolerance of the proposed technique is quantified by analyzing its SER using soft-error rate analyzer (SERA) [4].

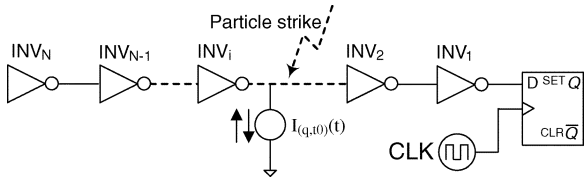

Fig. 2. Simulation setup for studying the impact of SETs on logic circuits.

Preliminary results from this work were presented in [11]. The rest of this brief is organized as follows. The soft-error simulation methodology is introduced in Section II. Details of the SET-tolerant design are described in Section III. Conclusions are discussed in Section IV.

II. SERA and Error Map

We employ SERA and error map in this work to validate the proposed SET-tolerant design techniques. SERA is based on a modeling and analysis approach that employs a judicious mix of probability theory, circuit simulation, graph theory and fault simulation [4]. SERA takes a circuit netlist and attaches time dependent pulse current source to possible particle strike nodes in a circuit. The overall SER is then computed based on a well-constructed probability space, after the circuit responses are simulated and combined with logic simulation results. Fig. 2 illustrates a simple circuit for quantifying the effect of SETs on logic circuits, where a FF is driven by an N-inverter chain circuit. SERA emulates a neutron hit by inserting the pulse current source with either polarity at one of the N possible locations, as shown in Fig. 2. The current source has the following form [12]:

$$I_{(q,t_0)}(t) = \begin{cases} 0, & t < t_0 \\ \pm\frac{2q}{\tau\sqrt{\pi}}\sqrt{\frac{t-t_0}{\tau}}e^{-\frac{t-t_0}{\tau}}, & t \geq t_0 \end{cases} \quad (1)$$

where q is collected charge, t_0 is the time instant at which a particle hits the node, and τ is a process technology-dependent time constant [13]. Note that the polarity of the current source is determined by whether the charge is collected by the drain of a pMOS or nMOS, as a drain node can collect only the minority carriers from the substrate or a well [13]. SERA observes the value latched by the FF with both parameters q and t_0 swept in the range $[0, Q_{\max}]$ and $[0, T_{\text{clk}}]$, respectively. The parameter $Q_{\max}$ is the maximum amount of collected charge and is assumed to be 100 fC in this work [4]. The parameter T_{clk} is the clock period. SERA estimates the SER while taking into account the statistical distributions of relevant physical parameters. For simplicity, we show only the probability of soft error given a particle hit on any of the inverter drain nodes, denoted as $P(\text{SE})$. Note that $P(\text{SE})$ is proportional to SER [4].

Error maps are employed to improve visibility into the designs. An error map, shown in Fig. 3 for a 4-inverter chain connected to a semidynamic FF (SDFF) [14], is a two-dimensional plot showing error generating combinations of q and t_0. A black pixel in the error map corresponds to an error. The error maps in Fig. 3 indicate: 1) errors occur if the collected charge at a specific node is large enough (e.g., $q > 30$ fC for INV_4) and the particle hit time t_0 lies between two specific values (e.g., 120 ps $< t_0 <$ 300 ps for INV_4) for a SET to be captured by an FF; and 2) neutron hits at drain nodes closer to the FF are more likely to cause errors.

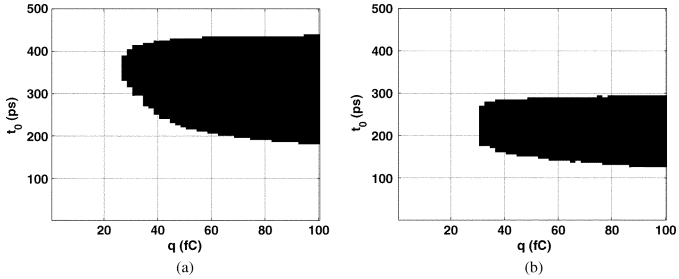

Fig. 3. Error maps for a neutron hit at the output of: (a) INV_1 and (b) INV_4.

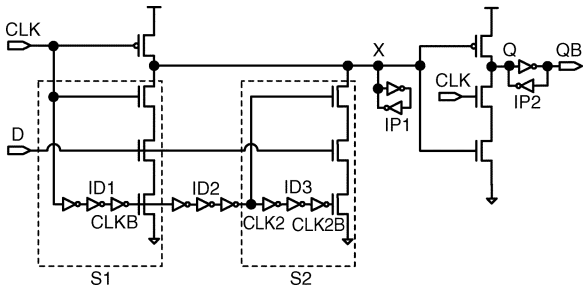

Fig. 4. Circuit schematic of the proposed DSFF.

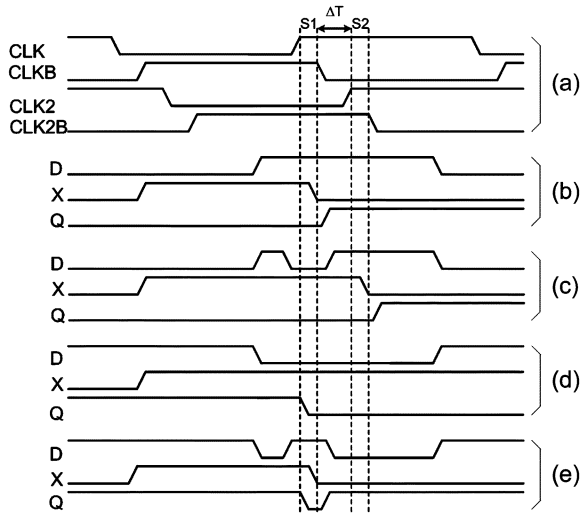

Fig. 5. DSFF timing diagram. (a) CLK signal and delayed CLK signals. (b) Latching a one. (c) Latching a one with a $1 \rightarrow 0$ SET. (d) Latching a zero. (e) Latching a zero with a $0 \rightarrow 1$ SET.

III. SET-Tolerant Techniques

In this section, we present the proposed circuit techniques for mitigating the impact of SETs. These techniques are based on a novel DSFF and SCMOS circuit style.

A. DSFF

We propose a DSFF as shown in Fig. 4. It is a pulsed FF operating on the same principles as the hybrid latch FF (HLFF) [15] and the SDFF [14]. Unlike HLFF and SDFF, the DSFF has two samplers $S1$ and $S2$.

When CLK is low, node X is precharged high, as illustrated in Fig. 5. The DSFF then utilizes a brief transparency period, determined by an integrated one-shot derived from the rising clock edge, to latch the data. This provides DSFF its edge-triggered nature as illustrated in Fig. 5(b) and (d).

TABLE I
COMPARISONS OF FFS

FF type	Worst-case latency (ps)	Power (μW)
SDFF	$t_{\mathrm{CLK-Q}} = 150$	226
TSL	$2 \cdot t_{\mathrm{h}} + 2\tau_{\max} + t_{\mathrm{CLK-Q}} + t_{\mathrm{voter}} = 1020$	955
DSFF	$t_{\mathrm{h}} + \tau_{\max} + t_{\mathrm{CLK-Q}} = 460$	265

The DSFF gets its SET tolerance as a result of the dual-sampling feature. As shown in Fig. 4, the transistors in box $S1$ constitute the first sampler with a sampling window defined by signals CLK and CLKB [see Fig. 5(a)]. The second sampler $S2$ is identical to $S1$ except that it is controlled by a delayed version of CLK. Note that each sampler has the same hold time t_{h}. The circuit configuration is such that the results of the two samplers are logically ORed. If the separation ΔT between the two sampling windows is made greater than the maximum SET duration $\tau_{\max}$ by sizing the inverter delay chain ID2, the DSFF will completely filter out SETs with $1 \rightarrow 0$ polarity at the input D of DSFF. This is because the signal at input D is high during at least one of the sampling windows and node X is always pulled low. Hence, correct latching of a one in the presence of a $1 \rightarrow 0$ SET is guaranteed.

However, the DSFF becomes more susceptible to a $0 \rightarrow 1$ SET than a SDFF. This is because the SET pulse overlapping with either of the two sampling windows would cause the voltage at node X to become low and stay there until the next precharge phase. This event is illustrated in Fig. 5(e).

We compare DSFF, SDFF, and TSL in Table I. This comparison is justified because SDFF is a representative high-speed FF, while TSL is the state of the art in SET-tolerant FF design. The worst case delay for each FF is written in terms of the hold time t_{h}, maximum SET duration $\tau_{\max}$, and voter gate delay t_{voter}. The power is measured by applying a 1-GHz clock and assuming a data activity factor of one. Note that all the FFs can be designed such that the setup times are zero due to the implicit pulsed clocking. Compared to TSF, the speed penalty of the DSFF is smaller by $2.2\times$ while consuming $3.6\times$ less power. Specifically, the DSFF has the following advantages over TSL: 1) compact structure and hence low power; 2) simple clocking; 3) a lower speed penalty; and 4) the voltage change at node X is unidirectional during evaluate phase and hence glitching is minimized. Compared to SDFF, DSFF has a $3\times$ increase in worst case latency and a $1.2\times$ increase in power. We shall see later that the gain in SET tolerance by using DSFF more than compensates for its speed and power penalties over SDFF.

Another notable feature of DSFF is that it does not cause any speed penalty when no SET has reached its data input terminal or when a $1 \rightarrow 0$ SET reaches its input and overlaps the second sampling window. This feature has an important indication. Let us compare the performance of two logic paths with the same cycle time. The combinational circuits in both paths are identical. One path uses DSFF while the other uses SDFF. Timing violation will never occur in the path with DSFF in absence of SET although the worst case latency of DSFF is larger than that of the SDFF. Even if the worst case latency of DSFF is reached as the result of an SET reaching its data input, timing violation still may not occur if the critical path of the next pipeline stage is not sensitized.

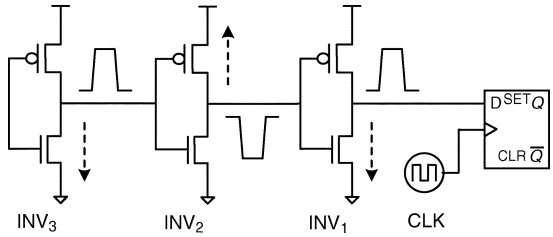

Fig. 6. SCMOS circuit style that attenuates $0 \rightarrow 1$ SET pulses at the FF input.

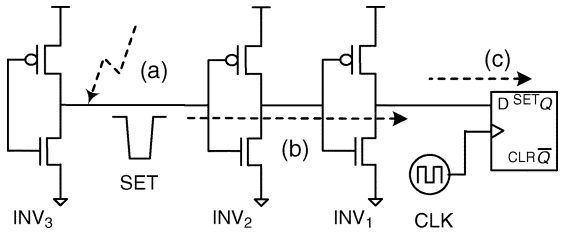

Fig. 7. (a) The generation, (b) the propagation, and (c) the capture of an SET in a static balanced CMOS circuit with SDFF.

B. SCMOS

As DSFF is susceptible to $0 \rightarrow 1$ SETs, we propose to employ the SCMOS circuit technique [16] so that a $0 \rightarrow 1$ SET is heavily attenuated at the FF input. In SCMOS (see Fig. 6), either the nMOS or the pMOS transistors (indicated by an adjacent arrow) are sized up by a factor of k_{skew}. Note that we do not precharge the intermediate nodes as in [16].

Fig. 7 shows the three processes that jointly determine whether an SET pulse will be latched: (a) pulse generation, (b) pulse propagation and (c) pulse capture. Pulse generation and pulse propagation is determined by the transistor sizes and the supply voltage. As the sizes increase, pulse generation is weakened but pulse propagation is strengthened. Pulse capture process depends on the propagated SET pulse magnitude, duration, and relative position with respect to the latching window [4].

We define k_{bal} to be the balanced scaling factor with respect to a minimum-sized inverter with balanced pull-up and pull-down paths. Figs. 8 and 9 show that balanced scaling of inverter chain circuit (connected to an SDFF) reduces the error probability by a factor of $10\times$ when $k_{\mathrm{bal}} = 5$. This is because increasing transistor sizes weakens the pulse generation process much more than it strengthens the pulse propagation process.

Fig. 10 shows the error maps for both $0 \rightarrow 1$ and $1 \rightarrow 0$ SETs before and after the skewed scaling. The $1 \rightarrow 0$ transients get slightly stronger after the skewed scaling because the propagation process is strengthened while the generation process is weakened. The impact of skewed scaling is also shown in Fig. 11. The $0 \rightarrow 1$ error probability decreases by a factor of $10\times$ when k_{skew} is greater than 3 and becomes zero when it is 4 or greater. The $1 \rightarrow 0$ error probability increases by a factor of $1.8\times$ at a skewing factor of 5. Simulations also show that only the last three stages of the inverter chain need to be skewed by the factor of 4 to eliminate $0 \rightarrow 1$ errors caused by SETs generated at the output of any inverter. This is because the weakening of pulse propagation process alone is sufficient to attenuate the SETs generated at an inverter far away from the FF input.

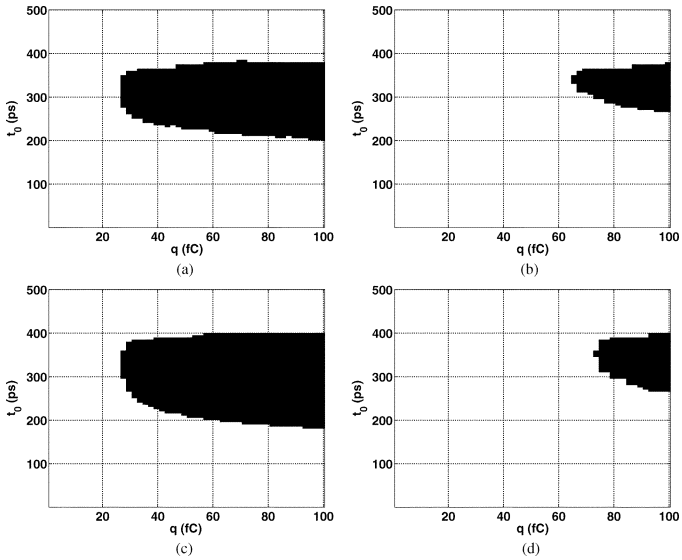

Fig. 8. Error maps for a neutron hit at the output of INV_2 in a static balanced CMOS circuit with SDFF for: $0 \rightarrow 1$ SET when k_{bal} is (a) one and (b) three, and $1 \rightarrow 0$ SET when k_{bal} is (c) one and (d) three.

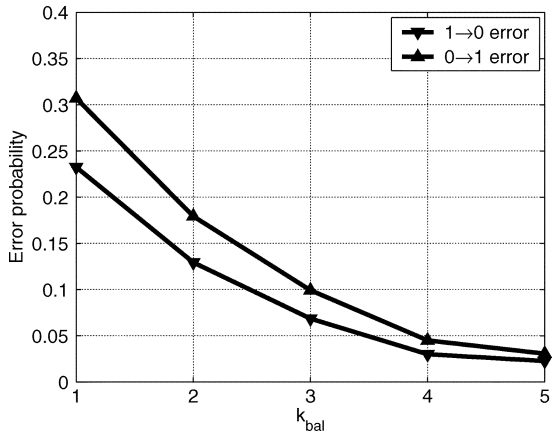

Fig. 9. Error probability as a function of k_{bal} in a 4-inverter balanced CMOS circuit with SDFF.

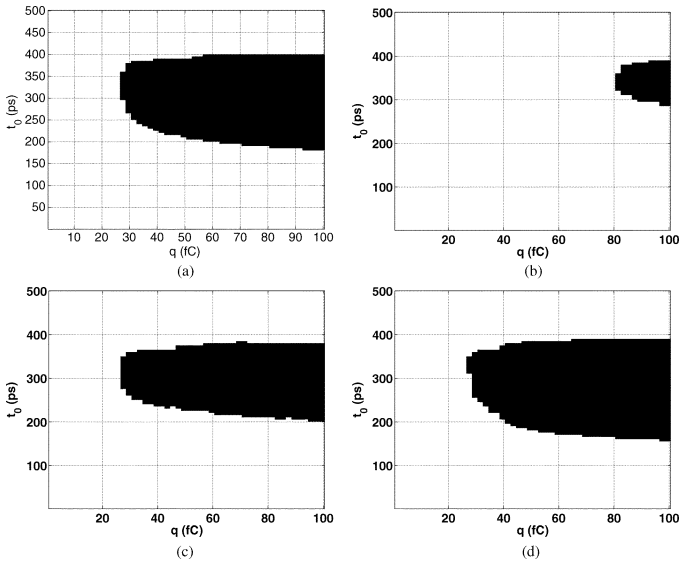

Fig. 10. Error maps for a neutron hit at the output of INV_2 in SCMOS circuit (with SDFF) for: $0 \rightarrow 1$ SET when k_{skew} is (a) one and (b) three, $1 \rightarrow 0$ SET when k_{skew} is (c) one and (d) three.

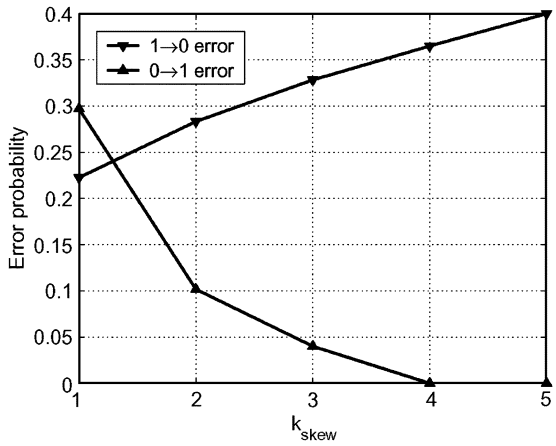

Fig. 11. Error probability as a function of k_{skew} in a 4-inverter SCMOS circuit (with SDFF).

TABLE II
COMPARISONS OF INVERTER CHAIN CIRCUITS

circuit type	Worst-case delay (ps)	Power (μW)
balanced ($k_{\mathrm{bal}} = 1$)	153	33
skewed ($k_{\mathrm{skew}} = 4$)	261	57

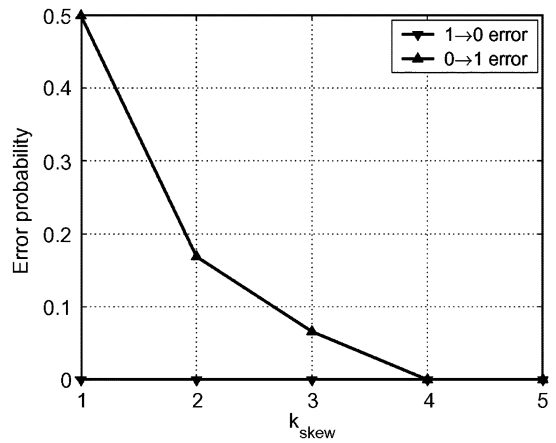

Fig. 12. Error probability versus k_{skew} in a 4-inverter chain for the proposed circuit (DSFF with $t_{\mathrm{h}} = 110$ ps, $\Delta_T = 200$ ps).

We compare balanced minimum-sized and skewed 4-inverter chains in Table II. Power is measured by applying a rising input between 0 and 1 ns and a falling input between 1 and 2 ns. It can be seen that the SCMOS style induces penalties of 108 ps and 24 μW in delay and power, respectively.

C. Dual-Sampling SCMOS

The DSFF and SCMOS mitigate or eliminate $1 \rightarrow 0$ and $0 \rightarrow 1$ SETs, respectively. As a result, their combination, denoted as dual-sampling SCMOS (DSSC), mitigates or eliminates SETs with both polarities. This fact is verified via the simulation results in Fig. 12, where a skewed 4-inverter chain circuit with a DSFF is employed. The $1 \rightarrow 0$ SETs are inherently tolerated by the DSFF. When the skewing factor $k_{\mathrm{skew}} = 4$, all $0 \rightarrow 1$ SETs are eliminated.

Simulation results in Fig. 13 further show that the proposed technique is very robust when the supply voltage is reduced. The error probability remains bounded below 0.05 even when the supply voltage is as low as 1.4 V. Note that this slight increase in

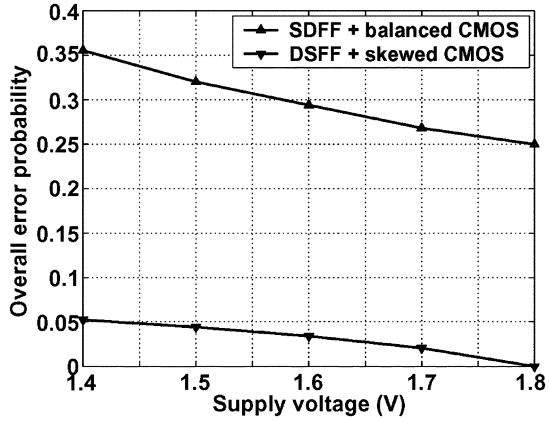

Fig. 13. Overall error probability (average of $0 \rightarrow 1$ and $1 \rightarrow 0$ error probabilities) as a function of the supply voltage in a 4-inverter CMOS circuit.

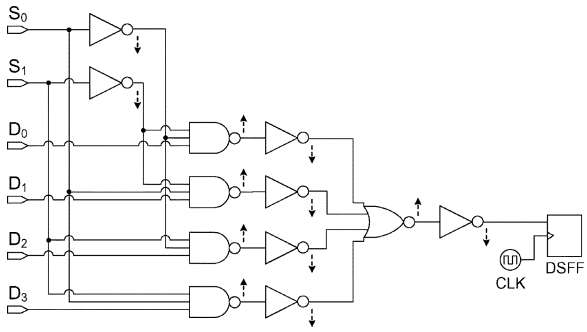

Fig. 14. Skewed 4-to-1-line multiplexer connected to DSFF.

TABLE III
COMPARISONS OF DSSC AND BALANCED STATIC CMOS CIRCUITS

circuit type	Worst-case delay (ps)	Power (μW)
balanced 4-inverter chain with SDFF	303	259
balanced 4-inverter chain with TSL	1173	988
skewed 4-inverter chain with DSFF	721	322
balanced 4-to-1-line mux with SDFF	424	271
balanced 4-to-1-line mux with TSL	1294	1000
skewed 4-to-1-line mux with DSFF	949	343

error probability at low supply voltage can be eliminated by increasing the ΔT parameter of the DSFF and the skewing factor of the CMOS circuit.

A sum-of-products implementation of a 4-to-1-line multiplexer circuit designed in DSSC style is illustrated in Fig. 14. We do not use the two-level implementation of the multiplexer circuit because it is much easier to observe the propagation of SETs in multi-level logic circuits. We compare DSSC circuits with balanced static CMOS circuits in Table III. Note that $k_{\rm bal} = 1$ for all balanced circuits while $k_{\rm skew} = 4$ for all skewed circuits. The DSSC technique, if used in a 4-inverter chain or multiplexer circuit, provides 27–39% speedup and 65–67% power savings, compared to the TSL technique.

IV. CONCLUSION

This brief describes a novel DSSC technique, which combines a DSFF and SCMOS combinational circuit style to mitigate radiation-induced SETs . Results have shown that the DSSC technique is much more efficient than employing TMR at the latch level. The SCMOS circuit style, similar to domino, is difficult to be implemented in circuits with reconvergent fanout and trapped inversions. A future research area is to investigate how to efficiently employ the DSSC technique in such complex circuits.

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