Soft-Error-Rate-Analysis (SERA) Methodology

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***Abstract*—We present a soft-error-rate analysis (SERA) methodology for combinational and memory circuits. SERA is based on a modeling and analysis approach that employs a judicious mix of probability theory, circuit simulation, graph theory, and fault simulation. SERA achieves five orders of magnitude speedup over Monte Carlo-based simulation approaches with less than 5% error. Dependence of the soft-error rate (SER) of combinational logic circuits on a supply voltage, clock period, latching window, circuit topology, and input vector is explicitly captured and studied for a typical 0.18-μm CMOS process. Results show that the SER of logic is a much stronger function of timing parameters than the supply voltage. Also, an SER peaking phenomenon in multipliers is observed where the center bits have an SER that are orders of magnitude greater than those of the LSBs and the MSBs. An increase of up to 25% in the SER for multiplier circuits of various sizes has been observed as technology scales from 0.18 to 0.13 μm.**

***Index Terms*—Combinational logic circuits, integrated-circuit reliability, single-event transient (SET), single-event upset (SEU), soft error, soft-error rate (SER).**

I. Introduction

SOFT ERRORS caused by particle hits are a serious problem for modern static random access memory (SRAM) designs due to reduced feature size and supply voltage [1], [2]. An empirical soft-error rate (SER) model has been proposed for SRAMs [3]. It predicts SER from a critical charge $Q_{\rm crit}$, drain area, neutron flux, and other empirical parameters. Researchers have shown that SER in logic is posing a threat now [4] and may increase by orders of magnitude within the next few years [5].

Modeling and analysis of the SER in logic is an inherently more complex problem than in memory. A single $Q_{\rm crit}$ value is not sufficient to describe the SER in logic circuits, as both the storage nodes (e.g., D-flip-flops (DFFs) or registers) and the combinational-circuit nodes are susceptible to particle hits. A single-event transient (SET) generated by a particle hit at a combinational-circuit node may experience electrical, timing, and logical maskings before it reaches the next pipeline stage and cause a bit error [5]. Electrical masking is a strong function of the sizing of gates in the logic chain, timing masking mainly depends on the DFF design, and logical masking is mostly determined by the input vectors. The abovementioned masking mechanisms pose a major challenge for a modeling SER in a combinational logic. A wide body of research is available that addresses the combinational logic SER problem from different perspectives.

Tools such as the soft-error Monte Carlo modeling (SEMM) program [6] employed in a industry provides the best level of accuracy that can be achieved by simulations but is quite expensive because time-consuming Monte-Carlo (MC) simulations are used. The soft error simulation algorithm developed by Kaul *et al.* [7] uses parameterized closed form expressions to represent the responses of each gate to an SET. The generation, propagation, and capture of the SET is modeled without running time-consuming circuit-level simulations, and hence the speed of the tool is greatly improved. However, this alogrithm does require a database of parameters to fit the analytical expressions. The complexity of such equations is expected to increase dramatically for newer fabrication processes as a result of increasing complexity of the device models [8].

The fault simulator for transients (FAST) [9] uses a gate-level timing fault simulator (TIFAS) to model the SETs and a zero-delay parallel fault simulator to track bit errors. Loss in accuracy due to the nature of the logic-level simulator has been noted. Other examples of logic-level tools include accurate soft-error tolerance analysis (ASERTA) [10], [11] and automatic soft spot analyzer (ASSA) [12]. They are not computationally intensive for the same reason. However, loss in accuracy is inevitable due to the simplifying assumptions made such as the "linear ramp glitch" assumption [11] and "effective noise window" assumption [12].

The transient fault simulator developed by Yang and Saleh [13] utilizes an efficient dynamic mixed-mode simulation approach, where the various portions of the circuit may switch between the different levels of abstraction during the simulation. Time-consuming circuit-level simulations are used only when deemed necessary by the tool. This approach provides better accuracy than the logic-level tools at the price of longer run times. SEUTool [14] analyzes soft-error phenomenon in combinational and sequential CMOS logic circuits. This technique can identify problematic regions within the circuit and predict the overall circuit reliability. However, the effect of reconvergent fanout on the SER of a combinational logic is not accounted for.

The SEU analysis approach proposed by Baze *et al.* [15], [16] is a tool at an even higher level of abstraction. It is a mathematical model rather than a simulator. It endeavors to reduce execution time by avoiding simulations at both the circuit and logic level. However, the inaccuracy in predicting an SER for a combinational logic can be as high as 30% [16]. Such high level of inaccuracy is caused by its simplified treatment of transients. For example, it does not consider

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transient pulse shapes, treating all transients as square pulses of a fixed width. It also ignores pulse attenuation and simply assigns zero propagation probability to all generated pulses with widths narrower than the minimum setup and hold time of the receiving DFF. Prior work [5], [17] has also attempted the modeling of SER of combinational logic from a system perspective. These approaches also use simplifying assumptions such as the concept of the "vulnerability window." These assumptions limit the accuracy, although they are justified by speedups required to analyze large designs such as a microprocessor.

The soft-error-rate-analysis (SERA) methodology presented in this paper is designed specifically to avoid the limitations of existing soft-error analysis methods. SERA has the following properties.

1) **Systematic**: It is built-upon a rigorously derived probabilistic framework, which connects different layers of the soft-error phenomenon nearly seamlessly. It outputs an error rate (in terms of number of errors per unit time) for any given circuit based on environmental factors (e.g., particle flux and probability-density function of injected charge), circuit structure (e.g., logic topology and DFF circuit design), and usage model (e.g., input vectors). Many of the existing tools (e.g., [6] and [13]) rely extensively on simulations and lack a mathematical framework. Some of the existing logic-level tools [9]–[12] can only estimate a soft-error "likelihood" in the relative sense, instead of the absolute error rate as SERA does, because these do not have a systematic framework linking the higher level abstractions to the physical layers (e.g., particle interaction with silicon atoms). The probabilistic nature of the injected charge is also not accounted for thereby resulting in considerable inaccuracy.
2) **Efficient**: It employs a judicious mix of probability theory, circuit simulation, graph theory, and fault simulation. Various SERA tasks are judiciously divided into groups and handled by different methods. Graph theory and fault simulation are used to analyze the logical-masking mechanism for a given circuit as well as to extract logic paths consisting of equivalent inverters. Circuit simulations are then preformed on such selected logic paths to analyze the electrical and timing masking mechanisms. An experimentally verified accurate current-pulse model is employed to emulate a particle hit at the device level. By employing this divide-and-conquer approach, a high level of accuracy is maintained while keeping a low-computational complexity. SERA has been shown to provide five orders of magnitude speed advantage over MC-based methods [6] with a comparable level of accuracy. Other fast simulators such as those based on logic-level simulations [5], [9]–[12], [17] are less accurate due to the simplifying assumptions on the pulse shape, vulnerability window, and other physical parameters.
3) **Versatile**: It is designed to be very transparent to developers and users because we emphasize a methodology instead of a tool. A unique advantage of SERA is that it can be easily extended to analyze the other transient-error phenomenon without modifying the theoretical framework. For example, alpha-particle-induced soft errors can be studied with SERA by a simple modification of the current-pulse model, hit rate, and probability-density distribution of injected charge, although the derivation in this paper is in the context of cosmic ray soft errors.

The impact of the transistor sizes, logic depth, circuit topology, clock speed, DFF speed, supply voltage scaling, and input-vector values on the SER of logic circuits has been studied using SERA. Several interesting results are derived such as the following.

1) The SER of combinational circuits is a much stronger function of the clock period and DFF latching window than supply voltage. This implies that the supply voltage reduction for energy efficiency will not make SER significantly worse. For example, the SER of a 32×32 parallel carry-save array multiplier in a Taiwan Semiconductor Manufacturing Company (TSMC) 0.18-μm technology increases by more than $50\times$ when the latching window is decreased by 20% from 120 ps, while it increases by only 28% when the supply voltage is decreased by 20% from 1.8 V.
2) SER analysis of multipliers shows an SER peaking phenomenon where the SERs of MSBs and LSBs are three orders of magnitude lower than those of the center bits.
3) SER of certain combinational circuits can be comparable to or exceed that of SRAMs with similar area. The SER of a 32×32 multiplier in 0.18-μm technology is higher than that of a 1-kb SRAM in the same technology.
4) An increase of up to 25% in SER for multiplier circuits of various sizes has been observed as technology scales from 0.18 to 0.13 μm.

Preliminary results from this work were presented in [18]. The rest of this paper is organized as follows. A probabilistic model is developed in Section II, which relates soft-error-rate and soft-error probability conditioned on an effective particle hit. Techniques for analyzing complex combinational circuits are presented in Section III. Results from SERA are shown and compared with the empirical model and the MC simulation in Section IV. Conclusions and future work are discussed in Section V.

II. Probabilistic Model for Soft Errors

We consider a canonical clocked logic circuit (CCLC) composed of a combinational circuit with latched primary inputs and outputs, as shown in Fig. 1. Note that a memory array is a special case of CCLC where only storage elements are present. A chip can then be treated as a network consisting of CCLCs.

Definition 1: A soft error is said to have occurred in the CCLC if a DFF captures the SET generated by a particle hit.

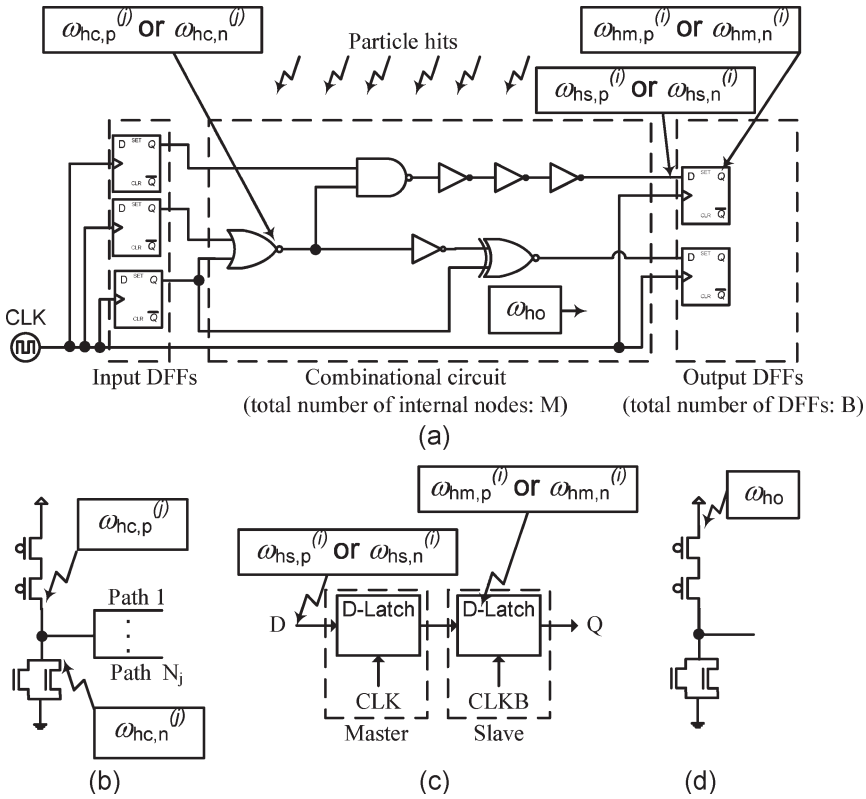

Fig. 1. Illustration of particle hits in CCLC: (a) overall structure of circuit with possible locations of particle hits and zoomed-in versions of outcomes, (b) $\omega_{\mathrm{hc,p}}^{(j)}$ and $\omega_{\mathrm{hc,n}}^{(j)}$, (c) $\omega_{\mathrm{hs,p}}^{(i)}$, $\omega_{\mathrm{hs,n}}^{(i)}$, $\omega_{\mathrm{hm,p}}^{(i)}$, and $\omega_{\mathrm{hm,n}}^{(i)}$, and (d) ω_{ho}.

A. SER

The upper bound on the SER (number of soft errors per unit time) of a chip is given by

$$\mathrm{SER_{chip}} \leq \sum_{k=1}^{N_\mathrm{C}} \mathrm{SER_{CCLC,k}} \tag{1}$$

where N_C is the number of CCLCs on the chip. Equation (1) becomes an equality only if the CCLCs are independent. The SER of a memory array, for example, is the sum of the SER for each memory cell. The modeling of various system-level derating mechanisms in a microsystem, which results in reduction in the overall SER, has been explored in [17]. We focus on the modeling of SER in a CCLC in this paper.

The SER of a CCLC is defined as

$$\mathrm{SER_{CCLC}} = R_\mathrm{PH} \cdot \alpha \cdot P(\mathrm{SE}) \tag{2}$$

where R_PH is the particle-hit rate, α is the fraction of particle hits that result in charge generation, and $P(\mathrm{SE})$ is the probability of a soft error conditioned on an effective particle hit. Note that the product $(R_\mathrm{PH} \cdot \alpha)$ denotes the rate of the effective particle hits. The concept of the effective particle hit is an abstraction of several physical processes in which particles interact with the semiconductor substrate to produce bursts of charge [2]. It is beyond the scope of this paper to discuss the physical nature of this phenomenon, which has been modeled in a prior work such as the neutron cross section method [19] and the burst generation rate model [20]. In this paper, we will derive the rate of the effective particle hit from an empirical model [3].

The hit rate of the various particle types such as alpha particles or neutrons are available from experiments [2]. The particle-hit rate R_PH caused by cosmic ray neutrons, for example, is given by

$$R_\mathrm{PH} = \int_{E_\mathrm{n,min}}^{E_\mathrm{n,max}} F_\mathrm{n}(E_\mathrm{n}) dE_\mathrm{n} \cdot A_\mathrm{t} \tag{3}$$

where $F_\mathrm{n}(E_\mathrm{n})$ is the altitude and location-dependent neutron flux [21] defined between neutron energies $E_\mathrm{n,min}$ and $E_\mathrm{n,max}$, and A_t is the total silicon area of the CCLC. We will derive $P(\mathrm{SE})$ and α in Sections II-B and III-A, respectively.

B. Soft-Error Probability

In this section, we define the probability space over which the probability of a soft error conditioned on an effective particle hit will be estimated. We assume that there will be one effective particle hit within a clock period resulting in a single-event upset (SEU). This assumption is justified by the typically small value of a particle flux (total neutron flux at sea level is 56.5 $\mathrm{m^{-2}s^{-1}}$) [21], a small chip area, and a short clock period. The probability experiment, probability space, and events of interest are defined as follows.

Definition 2: With reference to Fig. 1, an effective particle hit in a CCLC with B output DFFs and M internal circuit nodes have the following outcomes.

1) $\omega_{\mathrm{hc,p}}^{(j)}$: the generated charge q is collected by the p-type drain of the jth circuit node.
2) $\omega_{\mathrm{hc,n}}^{(j)}$: the generated charge q is collected by the n-type drain of the jth circuit node.
3) $\omega_{\mathrm{hs,p}}^{(i)}$: the generated charge q is collected by the p-type drain of the ith DFF sample stage.
4) $\omega_{\mathrm{hs,n}}^{(i)}$: the generated charge q is collected by the n-type drain of the ith DFF sample stage.
5) $\omega_{\mathrm{hm,p}}^{(i)}$: the generated charge is collected by the p-type drain of the ith DFF hold stage.
6) $\omega_{\mathrm{hm,n}}^{(i)}$: the generated charge is collected by the n-type drain of the ith DFF hold stage.
7) ω_{ho}: the generated charge is not collected by a circuit node, DFF sample stage, or hold stage.

$j \in \{1, 2, \ldots, M\}$ and $i \in \{1, 2, \ldots, B\}$.

Definition 3: The sample space Ω is

$$\Omega = \Big\{\omega_{\mathrm{hc,p}}^{(1)}, \omega_{\mathrm{hc,n}}^{(1)}, \ldots, \omega_{\mathrm{hc,p}}^{(M)}, \omega_{\mathrm{hc,n}}^{(M)}, \omega_{\mathrm{hs,p}}^{(1)}, \omega_{\mathrm{hs,n}}^{(1)}, \ldots, \omega_{\mathrm{hs,p}}^{(B)}, \omega_{\mathrm{hs,n}}^{(B)}, \omega_{\mathrm{hm,p}}^{(1)}, \omega_{\mathrm{hm,n}}^{(1)}, \ldots, \omega_{\mathrm{hm,p}}^{(B)}, \omega_{\mathrm{hm,n}}^{(B)}, \omega_{\mathrm{ho}}\Big\}.$$

The triple $(\Omega, \mathcal{B}, P)$ is the probability space, where $\mathcal{B}$ is the corresponding σ-field and P is a probability measure.

Definition 4: The events of interest are:

1) $\mathrm{SE}^{(i)}$: soft error at ith output bit;
2) SE: soft error at any output bit; $\mathrm{SE} = \bigcup_{i=1}^{B} \mathrm{SE}^{(i)}$;
3) $\mathrm{HC}_{\mathrm{p}}^{(j)} = \{\omega_{\mathrm{hc,p}}^{(j)}\}$; $P(\mathrm{HC}_{\mathrm{p}}^{(j)}) = A_{\mathrm{c,p}}^{(j)}/A_{\mathrm{t}}$;
4) $\mathrm{HC}_{\mathrm{n}}^{(j)} = \{\omega_{\mathrm{hc,n}}^{(j)}\}$; $P(\mathrm{HC}_{\mathrm{n}}^{(j)}) = A_{\mathrm{c,n}}^{(j)}/A_{\mathrm{t}}$;
5) $\mathrm{HS}_{\mathrm{p}}^{(i)} = \{\omega_{\mathrm{hs,p}}^{(i)}\}$; $P(\mathrm{HS}_{\mathrm{p}}^{(i)}) = A_{\mathrm{s,p}}^{(i)}/A_{\mathrm{t}}$;
6) $\mathrm{HS}_{\mathrm{n}}^{(i)} = \{\omega_{\mathrm{hs,n}}^{(i)}\}$; { $P(\mathrm{HS}_{\mathrm{n}}^{(i)}) = A_{\mathrm{s,n}}^{(i)}/A_{\mathrm{t}}$;
7) $\mathrm{HM}_{\mathrm{p}}^{(i)} = \{\omega_{\mathrm{hm,p}}^{(i)}\}$; $P(\mathrm{HM}_{\mathrm{p}}^{(i)}) = A_{\mathrm{m,p}}^{(i)}/A_{\mathrm{t}}$;
8) $\mathrm{HM}_{\mathrm{n}}^{(i)} = \{\omega_{\mathrm{hm,n}}^{(i)}\}$; $P(\mathrm{HM}_{\mathrm{n}}^{(i)}) = A_{\mathrm{m,n}}^{(i)}/A_{\mathrm{t}}$;
9) $\mathrm{HO} = \{\omega_{\mathrm{ho}}\}$

$$P(\mathrm{HO}) = \frac{1}{A_{\mathrm{t}}}\left[A_{\mathrm{t}} - \sum_{j=1}^{M}\left(A_{\mathrm{c,p}}^{(j)} + A_{\mathrm{c,n}}^{(j)}\right) - \sum_{i=1}^{B}\left(A_{\mathrm{s,p}}^{(i)} + A_{\mathrm{s,n}}^{(i)} + A_{\mathrm{m,p}}^{(i)} + A_{\mathrm{m,n}}^{(i)}\right)\right]$$

where $A_{\mathrm{c,p}}^{(j)}$, $A_{\mathrm{c,n}}^{(j)}$, $A_{\mathrm{s,p}}^{(i)}$, $A_{\mathrm{s,n}}^{(i)}$, $A_{\mathrm{m,p}}^{(i)}$, and $A_{\mathrm{m,n}}^{(i)}$ are the sensitive p- or n-type drain areas of corresponding circuit nodes, respectively.

Events 1 and 2 are the soft-error events of interest and will be further quantified in the succeeding sections. Events 3–9 are elemental effective particle-hit events. Event 3 and 4 are illustrated in Fig. 1(b). Events 5–8 acknowledge the fact that the commonly used master-slave DFFs have two stages: sample and hold, both of which are susceptible to particle hits [see Fig. 1(c)]. Event 9 is associated with a particle hit occurring at an irrelevant location, e.g., in the substrate far away from a drain node or at the source terminal of a transistor connected to a supply rail [see Fig. 1(d)]. Event 9 does not cause soft errors, i.e., $P(\mathrm{SE}^{(i)}|\mathrm{HO}) = 0$. The charge released by an incoming particle can be collected by a circuit node only if the particle hit occurs within a sensitive area around the node [22], [23]. This property is quantified by the definitions of probabilities of elemental events, as shown above. These will be evaluated in Section III-A.

The probability of soft error at the ith output bit is derived from the theorem of total probability as

$$\begin{aligned} P\left(\mathrm{SE}^{(i)}\right) = &\sum_{j=1}^{M}\Big[P\left(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{p}}^{(j)}\right)P\left(\mathrm{HC}_{\mathrm{p}}^{(j)}\right) + P\left(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{n}}^{(j)}\right)P\left(\mathrm{HC}_{\mathrm{n}}^{(j)}\right)\Big] \\ &+ \sum_{j=1}^{B}\Big[P\left(\mathrm{SE}^{(i)}|\mathrm{HS}_{\mathrm{p}}^{(j)}\right)P\left(\mathrm{HS}_{\mathrm{p}}^{(j)}\right) + P\left(\mathrm{SE}^{(i)}|\mathrm{HS}_{\mathrm{n}}^{(j)}\right)P\left(\mathrm{HS}_{\mathrm{n}}^{(j)}\right)\Big] \\ &+ \sum_{j=1}^{B}\Big[P\left(\mathrm{SE}^{(i)}|\mathrm{HM}_{\mathrm{p}}^{(j)}\right)P\left(\mathrm{HM}_{\mathrm{p}}^{(j)}\right) + P\left(\mathrm{SE}^{(i)}|\mathrm{HM}_{\mathrm{n}}^{(j)}\right)P\left(\mathrm{HM}_{\mathrm{n}}^{(j)}\right)\Big]. \end{aligned} \tag{4}$$

As the CMOS gates are unidirectional, we assume that an effective particle hit at the sample or hold stage of one DFF does not introduce soft errors in another DFF. Hence, (4) can be simplified to

$$\begin{aligned} P\left(\mathrm{SE}^{(i)}\right) = &\sum_{j=1}^{M}\Big[P\left(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{p}}^{(j)}\right)P\left(\mathrm{HC}_{\mathrm{p}}^{(j)}\right) + P\left(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{n}}^{(j)}\right)P\left(\mathrm{HC}_{\mathrm{n}}^{(j)}\right)\Big] \\ &+ P\left(\mathrm{SE}^{(i)}|\mathrm{HS}_{\mathrm{p}}^{(i)}\right)P\left(\mathrm{HS}_{\mathrm{p}}^{(i)}\right) \\ &+ P\left(\mathrm{SE}^{(i)}|\mathrm{HS}_{\mathrm{n}}^{(i)}\right)P\left(\mathrm{HS}_{\mathrm{n}}^{(i)}\right) \\ &+ P\left(\mathrm{SE}^{(i)}|\mathrm{HM}_{\mathrm{p}}^{(i)}\right)P\left(\mathrm{HM}_{\mathrm{p}}^{(i)}\right) \\ &+ P\left(\mathrm{SE}^{(i)}|\mathrm{HM}_{\mathrm{n}}^{(i)}\right)P\left(\mathrm{HM}_{\mathrm{n}}^{(i)}\right). \end{aligned} \tag{5}$$

Fan-outs from a particular gate, as illustrated in Fig. 1(b), make it possible for one effective particle-hit event to cause soft errors at more than one output bit and hence the following inequality holds:

$$\max_{i} P\left(\mathrm{SE}^{(i)}\right) \le P(\mathrm{SE}) \le \sum_{i=1}^{B} P\left(\mathrm{SE}^{(i)}\right). \tag{6}$$

III. SERA

In this section, we develop the SERA framework for complex combinational circuits. We first describe the methodology

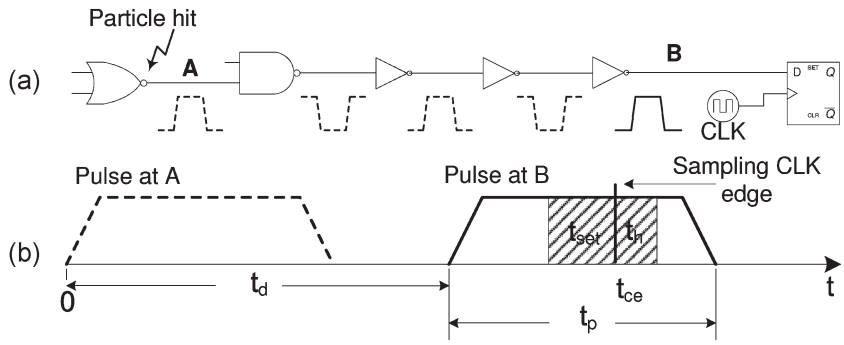

Fig. 2. Illustration of SET propagation and capture. (a) Path in CCLC that is not logically masked. (b) Timing diagram of SET and clock.

and extract important model parameters in Section III-A. The conditional probabilities in (5) are extracted from an inverter-chain circuit via circuit simulations in Section III-B. In Section III-C, these results are utilized together with a graph theory and a fault simulation to analyze the SER of complex combinational circuits. A generalized SERA framework that can be employed to analyze other transient-noise problems is discussed in Section III-D.

A. Methodology

The quantities defined in (1) and (3) can be extracted from cosmic ray data [2], [21] and chip layout. In this section, we describe the methodology to obtain the conditional probabilities appearing in (5).

The impact of an effective cosmic ray neutron hit on a circuit node is modeled by a time-dependent pulse-current source at a drain node [24]

$$I_{(q,t_{\rm PH})}(t) = \begin{cases} 0, & t < t_{\rm PH} \\ \pm\frac{2q}{\tau\sqrt{\pi}}\sqrt{\frac{t-t_{\rm PH}}{\tau}}e^{-\frac{t-t_{\rm PH}}{\tau}}, & t \geq t_{\rm PH} \end{cases} \quad (7)$$

where q is the amount of collected charge, $t_{\rm PH}$ is the time instant at which a particle hits the node, and τ is a process technology-dependent time constant [3]. Note that the polarity of the current source is determined by whether the charge is collected by a p- or n-type drain, as a drain node can collect only the minority carriers from the substrate or a well [25]. A particle hit occurring at a p-type drain would, for example, induce a current pulse with negative sign in (7), which means a positive charge is being injected to the node and the voltage may increase momentarily as a result.

The conditional probabilities in (5) can be determined by applying the current waveform in (7) to the various nodes of the circuit in Fig. 1(a). The polarity of the current source together with the logic state of victim node determines whether the logic state is corrupted. If, for example, the logic value of a node is 1 and the current source attached to that node has a positive polarity due to a particle hit at a n-type drain, a 1-0-1 SET may occur. On the other hand, a particle hit at a p-type drain will only reinforce the logic state 1. The outputs of DFFs are observed to determine whether the SET will be captured. The sampling clock edge arrival time $t_{\rm ce}$ is defined relative to the instant a particle hit occurs which is assumed to be at time $t = 0$ for convenience (see Fig. 2). Three conditions must be satisfied for a soft error to occur.

1) Logical masking must not occur.
2) SET pulse arriving at DFF input B must be wide enough.
3) Pulse amplitude at DFF input must be large enough.

Condition 1 is illustrated in Fig. 2(a). Condition 2 is satisfied if the pulse delay $t_{\rm d}$ is close to $t_{\rm ce}$ and if the pulse duration $t_{\rm p}$ is comparable to or greater than the sum of DFF setup time $t_{\rm set}$ and hold time $t_{\rm h}$, as illustrated in Fig. 2(b). Attenuation of a noise pulse when it propagates through cascading gates may cause the violation of condition 3. The proposed SERA methodology accurately models all the three effects to compute the SER.

The expressions for conditional probabilities corresponding to effective particle hits at p-type drains are given by (those at n-type drains are similar)

$$P\left(\mathrm{SE}^{(i)}|\mathrm{HC}_{\rm p}^{(j)}\right) = \int\int_{(q,t_{\rm ce})\in S_{\rm c,p}^{(j)}} f_Q(q) f_T(t_{\rm ce}) dt_{\rm ce} dq \quad (8)$$

$$P\left(\mathrm{SE}^{(i)}|\mathrm{HS}_{\rm p}^{(i)}\right) = \int\int_{(q,t_{\rm ce})\in S_{\rm s,p}^{(i)}} f_Q(q) f_T(t_{\rm ce}) dt_{\rm ce} dq \quad (9)$$

$$P\left(\mathrm{SE}^{(i)}|\mathrm{HM}_{\rm p}^{(i)}\right) = \int_{Q_{\rm crit,m,p}^{(i)}}^{\infty} f_Q(q) dq \quad (10)$$

where $S_{\rm c,p}^{(j)}$ and $S_{\rm s,p}^{(i)}$ are sets of soft-error-inducing $(q, t_{\rm ce})$ combinations corresponding to effective particle hits at the p-type drain of the jth internal circuit node and the ith DFF sample stage, respectively. The parameter $Q_{\rm crit,m,p}^{(i)}$ is the critical charge for the ith DFF hold stage, if the effective particle hit occurs at the p-type drain. The functions $f_Q(q)$ and $f_T(t_{\rm ce})$ are the probability-density functions (PDF) of the collected charge and the sampling clock edge arrival time, respectively. Because a particle hit is independent of the clock edge arrival, we assume $f_T(t_{\rm ce})$ to be a uniform distribution in the range $[0, T_{\rm clk}]$, where $T_{\rm clk}$ is the clock period. We show next that $f_Q(q)$ is an exponential distribution.

The hold stage of a DFF is similar to a 6-T SRAM cell and can be characterized with a single critical charge value $Q_{\rm crit}$

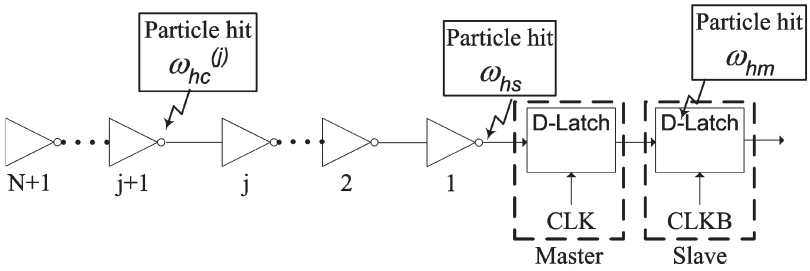

Fig. 3. Circuit-simulation setup for conditional probabilities extraction from inverter chain.

[26]. Its SER is derived from (2), (3), (5), (10) and the equations in Definition 4

$$\mathrm{SER}_{\mathrm{hold}}^{(i)}=\left(A_{\mathrm{m,p}}^{(i)}\cdot\int_{Q_{\mathrm{crit,m,p}}^{(i)}}^{\infty}f_Q(q)dq+A_{\mathrm{m,n}}^{(i)}\cdot\int_{Q_{\mathrm{crit,m,n}}^{(i)}}^{\infty}f_Q(q)dq\right)\times\int_{E_{\mathrm{n,min}}}^{E_{\mathrm{n,max}}}F_{\mathrm{n}}(E_{\mathrm{n}})dE_{\mathrm{n}}\cdot\alpha \quad (11)$$

where the first term in the parentheses corresponds to a $0\rightarrow 1$ error if a particle hit occurs at the p-type drain. The second term is for a $1\rightarrow 0$ error if a particle hit occurs at the n-type drain. Prior work on the SER of the DFF [26] or SRAM [23] typically assumes $Q_{\mathrm{crit,m,p}}^{(i)}=Q_{\mathrm{crit,m,n}}^{(i)}=Q_{\mathrm{crit,m}}^{(i)}$, which is justified by a proper design of a static CMOS gate so that the pull-up and pull-down paths have equal strengths. Under this condition, (11) is simplified to

$$\mathrm{SER}_{\mathrm{hold}}^{(i)}=\left(A_{\mathrm{m,p}}^{(i)}+A_{\mathrm{m,n}}^{(i)}\right)\cdot\int_{Q_{\mathrm{crit,m}}^{(i)}}^{\infty}f_Q(q)dq\cdot F\cdot\alpha \quad (12)$$

where F is the total neutron flux within the whole energy spectrum.

Now, the SER of a single SRAM cell is given by the empirical model in [3] as

$$\mathrm{SER}_{\mathrm{SRAM}}=F\cdot(A_{\mathrm{d,p}}+A_{\mathrm{d,n}})\cdot K\cdot e^{-\frac{Q_{\mathrm{crit}}}{Q_{\mathrm{s}}}} \quad (13)$$

where $A_{\mathrm{d,p}}$ and $A_{\mathrm{d,n}}$ are the p-type and n-type drain diffusion areas, K is a technology-independent fitting parameter, and Q_{s} is the collection slope which varies with technology.

A comparison of (12) and (13) indicates that

$$\alpha=K \quad (14)$$

$$A_{\mathrm{m,p}}^{(i)}=A_{\mathrm{d,p}} \quad (15)$$

$$A_{\mathrm{m,n}}^{(i)}=A_{\mathrm{d,n}} \quad (16)$$

$$f_Q(q)=\frac{1}{Q_{\mathrm{s}}}e^{-\frac{q}{Q_{\mathrm{s}}}}. \quad (17)$$

As both K and Q_{s} have been characterized in [3], and $A_{\mathrm{d,p}}$ and $A_{\mathrm{d,n}}$ are available from circuit layout, we will utilize (14)–(17) in the rest of this paper. Note that the sensitive areas of an internal circuit node and DFF sample stage node are assumed to be the corresponding drain areas. This is justified because the sensitive area is related to the charge collection mechanism and should not differ if the circuit node belongs to a DFF or logic gate [22], [25].

B. Extraction of Conditional Probabilities

Consider an inverter-chain circuit with $(N+1)$ inverters and a DFF at the final output, as shown in Fig. 3. Two conditions are implied: 1) no fan-ins or fan-outs and 2) no logical masking. Both conditions will be relaxed in Section III-C.

The current waveform in (7) is applied at one of the $(N+2)$ locations (N internal circuit nodes, one DFF sample and one DFF hold stage). The effect of the current waveform is determined by the value of q and t_{ce}, as illustrated previously in Fig. 2. We choose equally spaced data points in the set Λ defined as

$$\Lambda=[0,Q_{\max}]\times[0,T_{\mathrm{clk}}] \quad (18)$$

with step sizes of Δq and Δt, respectively.

For every particle-hit location, a flag function $F(q,t_{\mathrm{ce}})$, defined to equal one when there is a soft error and zero when no error occurs, is obtained from HSPICE simulations. The discretization of (8)–(10) as applied to the inverter-chain circuit results in

$$P\left(\mathrm{SE}|\mathrm{HC}_{\mathrm{p}}^{(j)}\right)=\sum_{(q,t_{\mathrm{ce}})\in\Lambda}f_Q(q)\Delta q f_T(t_{\mathrm{ce}})\Delta t_{\mathrm{ce}}F_{\mathrm{HC}_{\mathrm{p}}^{(j)}}(q,t_{\mathrm{ce}}) \quad (19)$$

$$P(\mathrm{SE}|\mathrm{HS_p})=\sum_{(q,t_{\mathrm{ce}})\in\Lambda}f_Q(q)\Delta q f_T(t_{\mathrm{ce}})\Delta t_{\mathrm{ce}}F_{\mathrm{HS_p}}(q,t_{\mathrm{ce}}) \quad (20)$$

$$P(\mathrm{SE}|\mathrm{HM_p})=\begin{cases}\sum_{q=Q_{\mathrm{crit}}}^{Q_{\max}}f_Q(q)\Delta q, & Q_{\mathrm{crit}}<Q_{\max}\\ 0, & Q_{\mathrm{crit}}\geq Q_{\max}\end{cases} \quad (21)$$

where a finite value $Q_{\max}$ is used as the upper limit in the summation in (21). This reduces the simulation run times. The error caused by this approximation is less than 2% if $Q_{\max}=4Q_{\mathrm{s}}$ due to the exponential distribution in (17).

While analyzing or simulating circuits that include sequential elements such as the one in Fig. 3, initial states of the

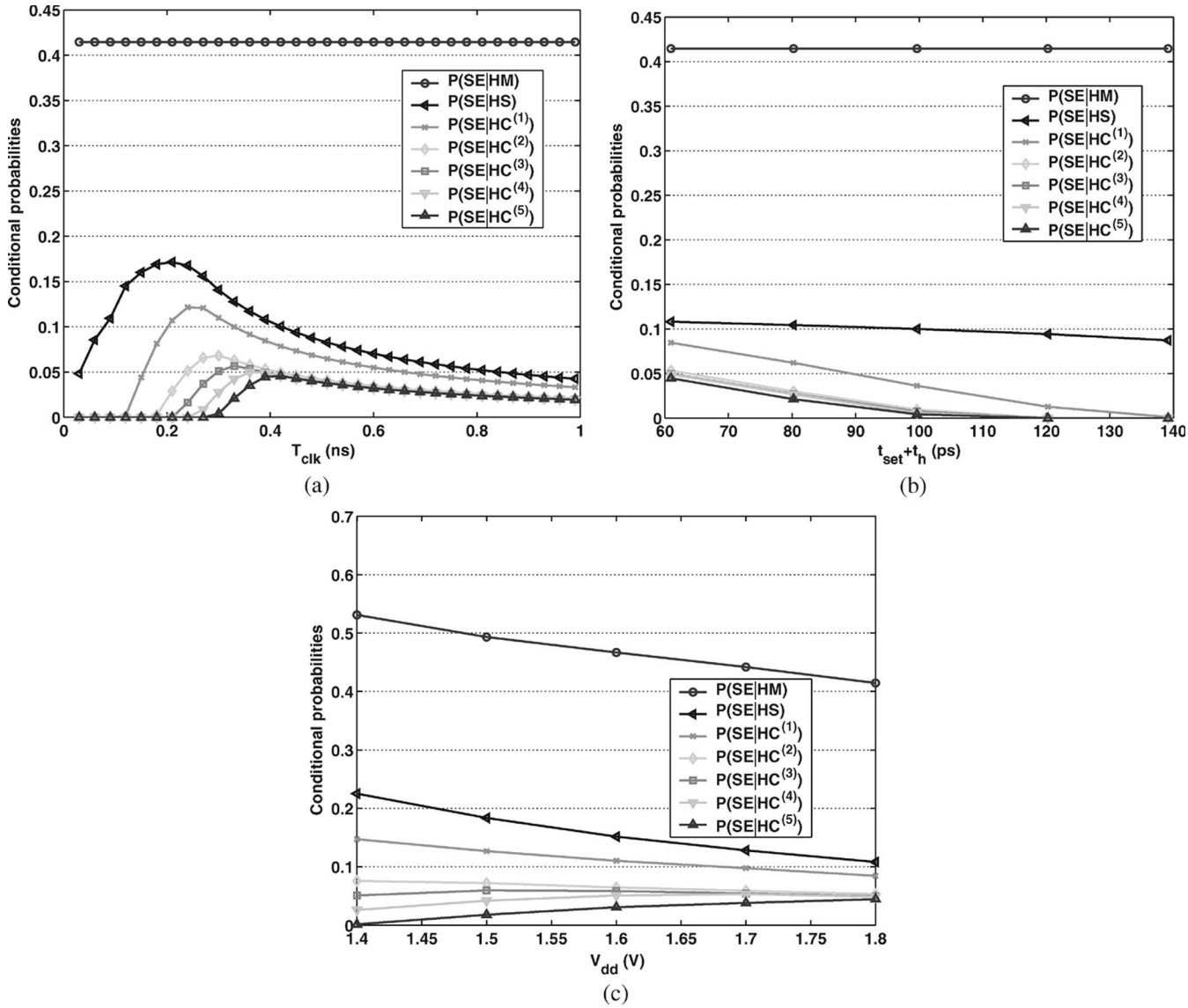

Fig. 4. Conditional probabilities (a) plotted as a function of $T_{\rm clk}$ ($V_{\rm dd} = 1.8$ V, $t_{\rm set} + t_{\rm h} = 61$ ps), (b) plotted as a function of $t_{\rm set} + t_{\rm h}$ ($V_{\rm dd} = 1.8$ V, $T_{\rm clk} = 0.4$ ns), and (c) plotted as a function of $V_{\rm dd}$ ($t_{\rm set} + t_{\rm h} = 61$ ps, $T_{\rm clk} = 0.4$ ns).

sequentials have to be dealt with properly. There are two possible scenarios when a DFF latches an input value from the preceding logic.

1) The initial state of the DFF and the next state after the clock edge are identical. In this scenario, the only way an SET can manifest itself is to have itself latched by the DFF and hence upset the correct initial state of the DFF. This qualitatively suggests that the smaller the setup and hold times are, the more likely the SET pulse can be latched into the DFF.
2) The initial state of the DFF and the next state after the clock edge are different. In this scenario, the presence of an SET will reduce the time available for the correct input to get latched. This would qualitatively suggests that larger setup and hold times result in higher SERs.

Of the two, the first scenario is more likely to occur than the second because: 1) a large fraction of the path delay in a high-performance microprocessor is significantly less than the clock cycle time, which means the correct data value has already propagated into the master stage of the DFF before the clock edge [29] and 2) data activity factor at a DFF input in a high-performance microprocessor is usually very small (e.g, less than 10%), which means the data to be latched into the DFF during the current clock cycle is most likely the same as the data stored in the DFF from the last clock cycle. We assume the initial state of the DFF and the next state are the same in the rest of this paper.

The conditional probabilities in (19)–(21) and those corresponding to particle hits at n-type drains (similarly derived) are evaluated in a TSMC 0.18 μm technology. In order to save space, we only show the average of conditionals corresponding to the p- and n-type drains in Fig. 4. Note that these two types of conditionals will be employed separately in Section III-C while analyzing the SER of complex combinational circuits.

As shown in Fig. 4(a), the conditionals are nonmonotonic functions of clock period $T_{\rm clk}$. The conditionals are zero when $T_{\rm clk}$ is small because the uniformly distributed sampling clock

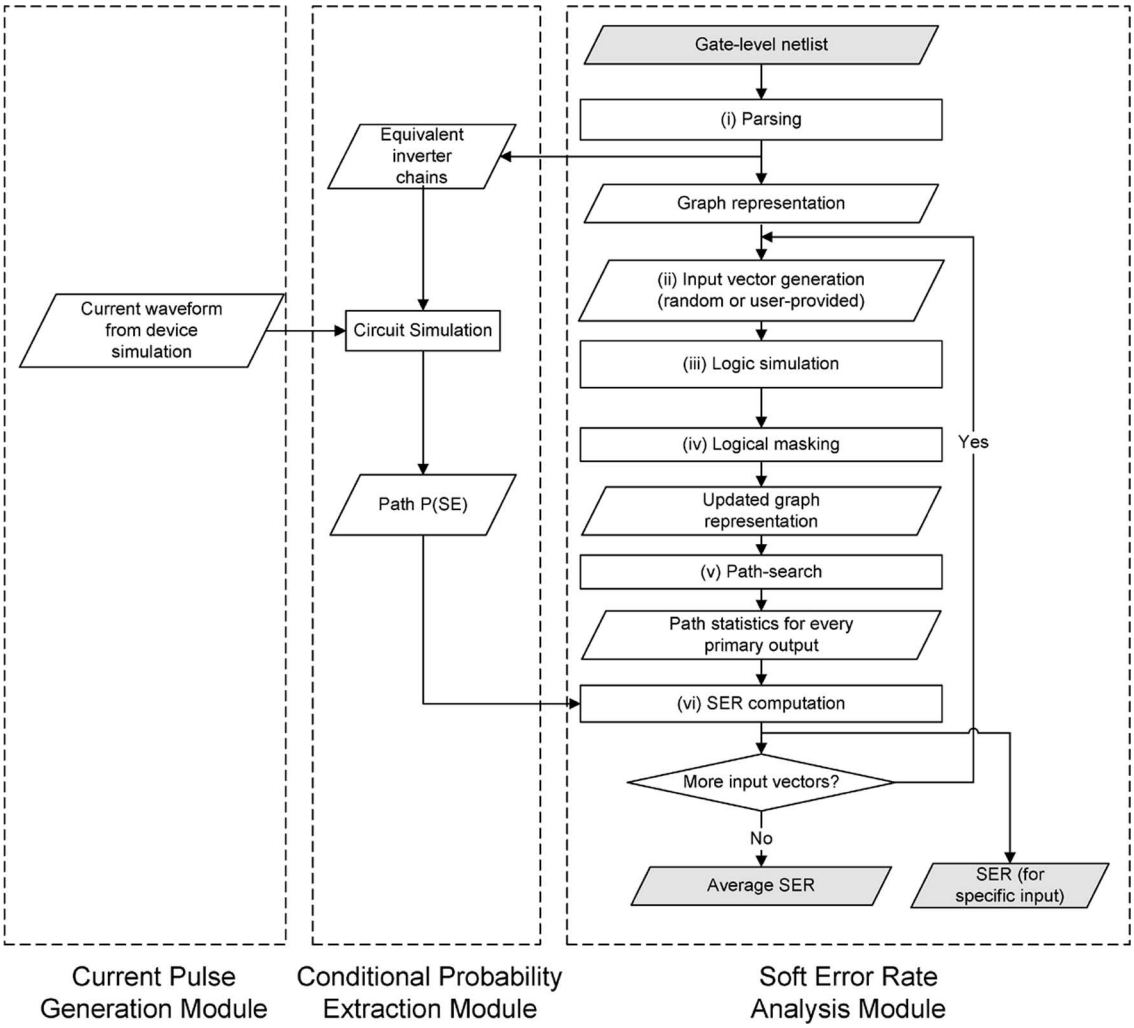

Fig. 5. SERA for combinational circuits.

edge always arrives before the SET arrival at the DFF input. The conditionals start to increase when $T_{\rm clk}$ is large enough such that the propagated SET starts to encompass the DFF latching window [see Fig. 2(b)]. The curves in Fig. 4(a) peak when $T_{\rm clk}$ is approximately equal to the pulse delay $t_{\rm d}$. The conditionals drop when $T_{\rm clk}$ becomes so large that the fraction of the clock edges arriving later than the SET arrival keeps increasing with $T_{\rm clk}$. In the 0.18-μm process, the conditional probability $P({\rm SE}|{\rm HM})$ is at least two times greater than the other conditionals. The other conditionals though small have significant impact on the overall SER because a logic circuit usually has many more combinational-circuit nodes than memory nodes (DFF hold stages). It is also observed that $P({\rm SE}|{\rm HC}^{(j)}) > P({\rm SE}|{\rm HC}^{(i)})$ if $j < i$. This is due to the attenuation of SET in both amplitude and duration when it propagates through the inverter chain.

Fig. 4(b) shows an increasing DFF latching window duration $(t_{\rm set} + t_{\rm h})$ results in a reduction of conditional soft-error probabilities. This is because a master–slave DFF with a wider latching window is less sensitive to the fast-switching SETs. Other DFF styles, such as those with a semidynamic front end, can be used in this simulation setup as well to obtain the corresponding conditional probabilities. Fig. 4(c) shows that different conditionals vary differently with supply voltage $V_{\rm dd}$. The conditionals $P({\rm SE}|{\rm HS})$, $P({\rm SE}|{\rm HC}^{(1)})$, and $P({\rm SE}|{\rm HC}^{(2)})$ decrease with the $V_{\rm dd}$ because the SET generation mechanism, which dominates for nodes closer to the DFF, becomes weaker at higher $V_{\rm dd}$ due to a stronger active pull-up or pull-down path in the gates. The conditionals $P({\rm SE}|{\rm HC}^{(4)})$ and $P({\rm SE}|{\rm HC}^{(5)})$ increase with $V_{\rm dd}$ because the delay between SET generation and SET arrival at DFF input plays a dominant role for nodes farther away from the DFF. The delay decreases as $V_{\rm dd}$ increases and hence it is more likely for the pulse to get latched. The conditional $P({\rm SE}|{\rm HC}^{(3)})$ happens to sit in the transition region between two regimes and is nonmonotonic with $V_{\rm dd}$.

C. SERA for Combinational Circuits

The procedure of SERA for combinational circuits is illustrated by the flow chart in Fig. 5. The current-pulse generation module is responsible for providing a circuit-simulation compatible transient-noise source to emulate the effect of a particle strike. In this paper, we use the current-pulse model published in [24], as shown in (7). The conditional probability extraction module operates on the principles described in Sections III-A and B. More specifically, we decompose a circuit

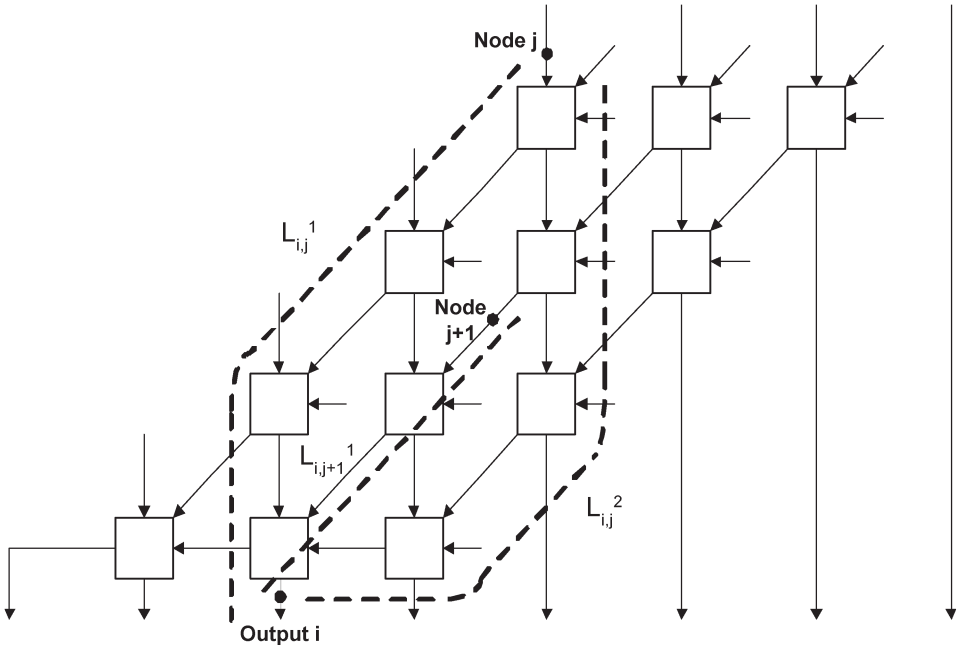

Fig. 6. Illustration of SER contribution from internal circuit nodes.

into a collection of circuit nodes with a gate between each pair of nodes. The gate is modeled as an equivalent inverter. This results in multiple inverter chains and thus the results in the previous section can be employed. For accuracy, three new factors are accounted for: 1) transistor sizing and multiple fan-ins are reflected by changing the size of equivalent inverter; 2) extra load due to fan-outs is modeled by adding a capacitor to the output of each inverter; and 3) logical masking is emulated.

The soft-error-rate-analysis module computes the SER of a combinational circuit based on results from the first two modules. Step (i) in the module converts a gate-level netlist to a graph where vertices and edges correspond to the internal circuit nodes and gates, respectively. In this context, a path length denotes the number of gates between the two circuit nodes. This step only needs to be done once for a given circuit. Note that the gate-level netlist also contains a transistor-sizing information so that an equivalent inverter chain can be extracted to obtain soft-error probabilities on a path. User-provided or randomly generated input vectors are used in step (ii), making an effort to average out variations in the SER for different input vectors. Logical-masking mechanism is accounted for in steps (iii) and (iv). The logic values of all vertices are first computed based on the input vectors. For every vertex, its logic value is temporarily flipped to see whether the value can propagate through an edge to an adjacent vertex [27]. The adjacency list representation of the circuit is then updated to emulate the logical-masking mechanism. More specifically, the element in the adjacency list that corresponds to a path between the ith and jth nodes will be removed if flipping the logic value at the ith node does not change the value at the jth node. In step (v), a path-search algorithm based on the well-known depth-first search algorithm is used to find all the paths between a given pair of primary output bit and internal circuit node. The length of each path is also recorded. If multiple paths exist between a pair of nodes (reconvergent fan-out), circuit simulation shows that the noise pulse generated by a particle hit can propagate along various paths and arrive at DFF input at different instants with small or no overlap due to different path delays. Hence, the following approximation holds for the soft-error probability at ith primary output bit conditioned on an effective particle hit at jth internal circuit node (see Fig. 6):

$$P\left(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{p}}^{(j)}\right) \simeq \begin{cases} \min\left(1, \sum_{k=1}^{N_{i,j}} P^{\left(L_{i,j,\mathrm{p}}^{k}\right)}\right), & V(j)=0 \\ 0, & V(j)=1 \end{cases} \tag{22}$$

$$P\left(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{n}}^{(j)}\right) \simeq \begin{cases} 0, & V(j)=0 \\ \min\left(1, \sum_{k=1}^{N_{i,j}} P^{\left(L_{i,j,\mathrm{n}}^{k}\right)}\right), & V(j)=1 \end{cases} \tag{23}$$

where $V(j)$ is the logic value of node j, $N_{i,j}$ is the number of unique path lengths between the jth internal circuit node and the ith primary output bit, $L_{i,j,\mathrm{p}}^{k}$ is the kth path length corresponding to a particle hit at p-type drain, $L_{i,j,\mathrm{n}}^{k}$ is the kth path length corresponding to a particle hit at n-type drain, and $P^{(L_{i,j,\mathrm{p}}^{k})}$ or $P^{(L_{i,j,\mathrm{n}}^{k})}$ is the corresponding conditional soft-error probability for the inverter-chain circuit shown previously in Fig. 3. Note that only paths with unique lengths are accounted for. This approximation results in a slight over estimation of the conditional probabilities because the propagation of a noise pulse along two paths with the same length may weaken, if not cancel, each other. We show in Section IV-A that this approximation does not result in significant degradation in estimation accuracy for most circuits.

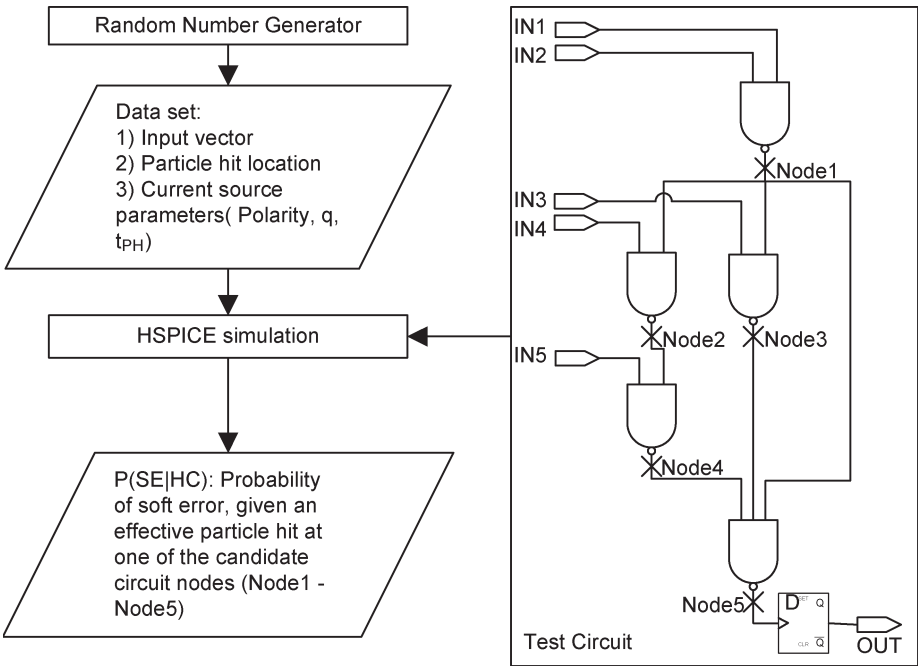

Fig. 7. MC simulation flow for SERA verification.

TABLE I
COMPARISON OF MC AND SERA APPROACHES

Test circuit	t_{MC} (min)	t_{SERA} (min)	$\frac{\Delta SER}{SER}$	Speed-up
#1 (5 gates)	1830	0.02	1.5%	91500×
#2 (8 gates)	3954	0.03	3.8%	131800×
#3 (11 gates)	9146	0.05	1.8%	182920×
4×4 mult.	-	0.1	-	-
8×8 mult.	-	1.3	-	-
16×16 mult.	-	41.2	-	-
32×32 mult.	-	593.3	-	-

Substituting (5) and equations from Definition 4 in (2) yields the soft-error probability and hence SER of the ith bit

$$\begin{aligned}\mathrm{SER}^{(i)} &= F\cdot\alpha\cdot\Bigg[\sum_{j=1}^{M}\Big(P\Big(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{p}}^{(j)}\Big)A_{\mathrm{c,p}}^{(j)}+P\Big(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{n}}^{(j)}\Big)A_{\mathrm{c,n}}^{(j)}\Big)\\ &\quad+P\Big(\mathrm{SE}^{(i)}|\mathrm{HS}_{\mathrm{p}}^{(i)}\Big)A_{\mathrm{s,p}}^{(i)}+P\Big(\mathrm{SE}^{(i)}|\mathrm{HS}_{\mathrm{n}}^{(i)}\Big)A_{\mathrm{s,n}}^{(i)}\\ &\quad+P\Big(\mathrm{SE}^{(i)}|\mathrm{HM}_{\mathrm{p}}^{(i)}\Big)A_{\mathrm{m,p}}^{(i)}+P\Big(\mathrm{SE}^{(i)}|\mathrm{HM}_{\mathrm{n}}^{(i)}\Big)A_{\mathrm{m,n}}^{(i)}\Bigg]\end{aligned} \tag{24}$$

where the conditionals $P(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{p}}^{(j)})$ and $P(\mathrm{SE}^{(i)}|\mathrm{HC}_{\mathrm{n}}^{(j)})$ are calculated from (22) and (23), while the other conditionals are calculated from (20) and (21).

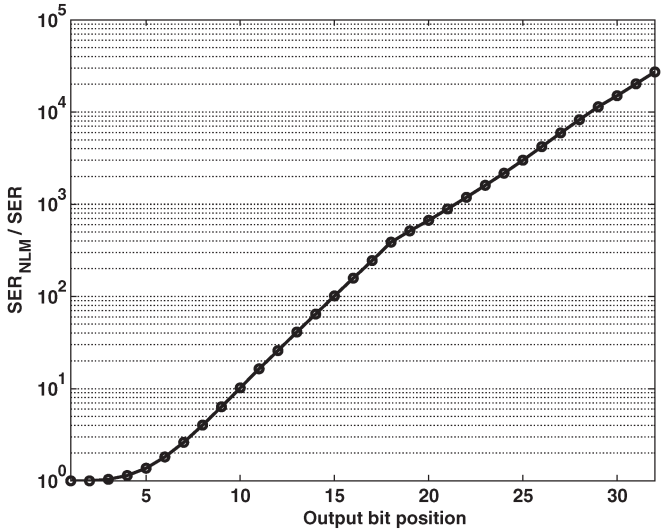

Fig. 8. Normalized SER ($\mathrm{SER_{NLM}}$: ignoring logical masking; SER: considering logical masking) of 16×16 multiplier's individual bit. Note that bit 1 is LSB while 32 is MSB.

D. Generalized SERA Framework

As described before, SERA employs a judicious mix of probability theory, circuit simulation, graph theory, and fault simulation. Referring back to Fig. 5, SERA takes a hierarchical divide-and-conquer approach in modeling the SER of a combinational circuit.

1) The effect of a particle strike is modeled by a current pulse as described in Section III-A. The current-pulse model is derived from 3-D device simulations and can be calibrated with experiments. It can be easily integrated into circuit simulations.

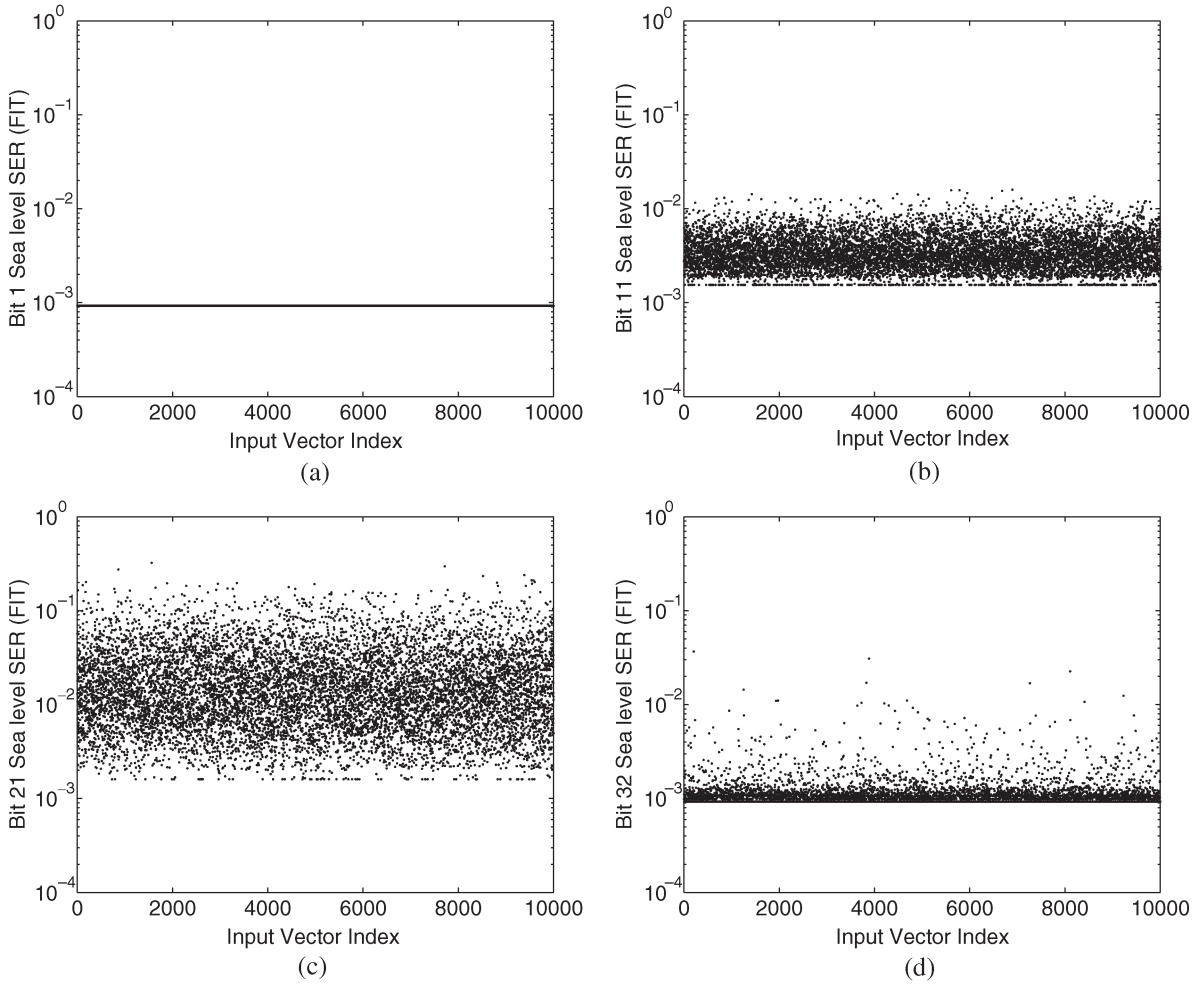

Fig. 9. SER of 16 × 16 multiplier as function of input vector for (a) bit 1, (b) bit 11, (c) bit 21, and (d) bit 32. Horizontal axis shows index of randomly generated input vectors.

2) Circuit simulations are employed in the conditional probability extraction module to provide conditional soft-error probabilities. The current-pulse model is used in the simulations to maintain the best possible accuracy. Simulation times will not be prohibitive because such simulations are run on a selected set of inverter chains. Electrical and timing masking mechanisms are accounted for in this step, as described in Section III-B.
3) Fault simulations and graph theory are employed in the soft-error-rate-analysis module. This takes logic masking into account while keeping the simulation time manageable because these algorithms are orders of magnitude faster than a device or circuit-level simulations. Details have been provided in Section III-C.
4) Finally, the probability theory outlined in Section II is the foundation of SERA and brings the above three pieces of information together and yield the end product of our analysis, the SER at any output bit of a given circuit, as illustrated by (24).

Therefore, the SERA methodology has been described in the context of cosmic ray soft errors. However, the SERA methodology can be extended to analyze any transient-noise problem. For example, alpha particle induced soft error can be analyzed by replacing the current-pulse model in (7) with the following [28]:

$$I(t) = I_0 \left(e^{-\frac{t}{\tau_1}} - e^{-\frac{t}{\tau_2}} \right) \tag{25}$$

where I_0 is the approximate maximum current, τ_1 is the collection time constant for junction, and τ_2 is the ion-track establishment time constant. The probability-density function of injected charge and particle-hit rate can also be updated. The soft-error-rate-analysis module will not need to be changed, except now that it will utilize a new conditional soft-error probability based on the above changes.

IV. Results

In this section, we compare the results of SERA with those of empirical model and MC simulation. We show that the SERA achieves an excellent accuracy with orders of magnitude reduction in run times. We show the effect of a logical-masking and an input-vector value on SER of combinational

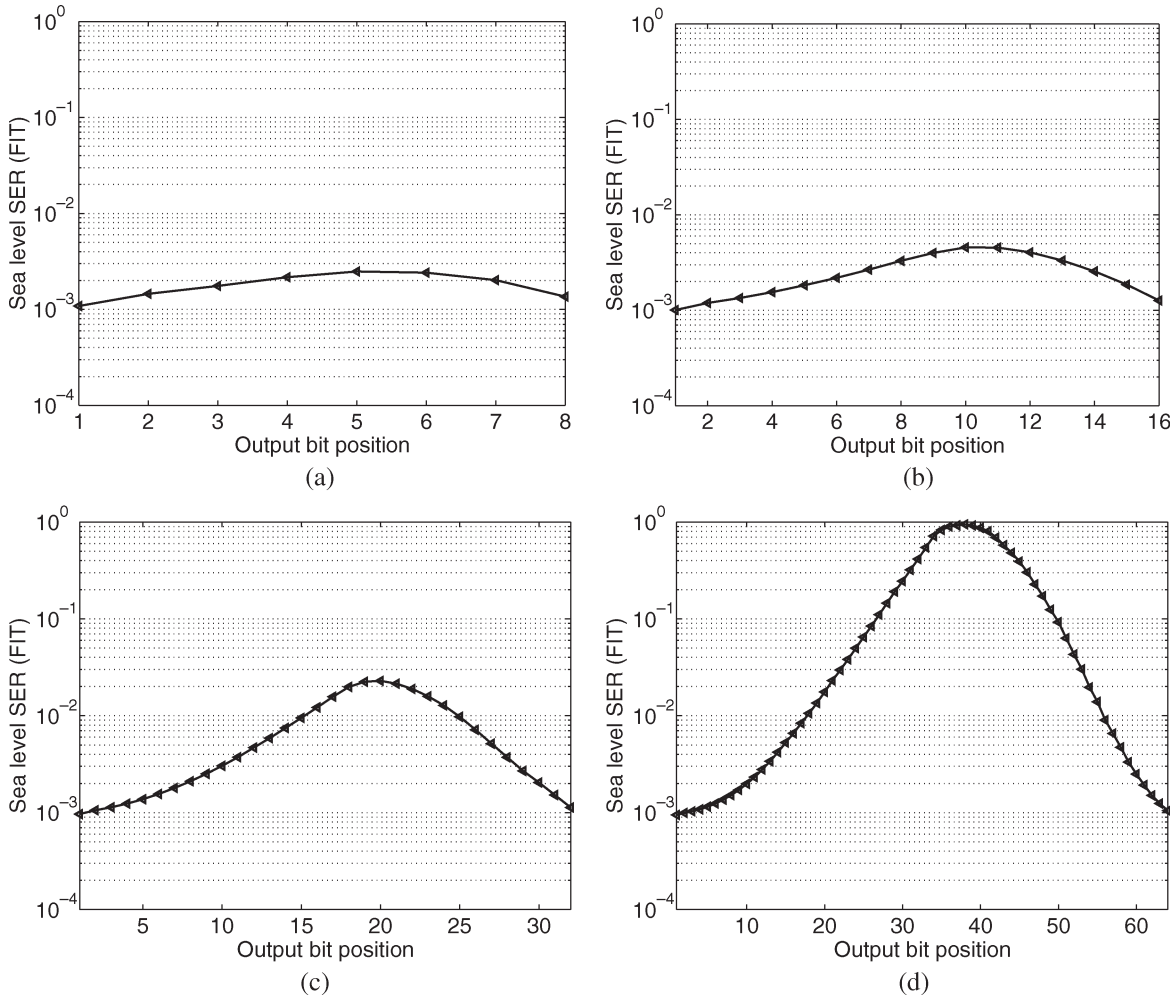

Fig. 10. SER at individual bits of multipliers of various sizes: (a) 4 × 4, (b) 8 × 8, (c) 16 × 16, and (d) 32 × 32.

logic circuits. We also present the estimated SER for multipliers of various size as an example. The dependence of the SER on a supply voltage and a DFF latching window is explicitly shown.

A. Comparison With Empirical Model and MC Simulations

To our best knowledge, empirical SER data for combinational circuits are not available in an open literature. Therefore, we validate the proposed SERA methodology by a two-step approach. We first compare the results from the SERA with existing empirical SER data for SRAMs [3], [25], knowing that an SRAM cell is nothing but a special case of CCLC. Study of SER as a function of supply voltage for 6-T SRAM cells in 0.35- and 0.6-μm processes shows consistent results. The worst case difference is 8% and can be well attributed to the difference in process parameters.

Secondly, we propose to use MC circuit simulations to verify the SER of a few small test circuits predicted by the SERA. The number of simulated random events required in an MC simulation for statistically significant predictions of the SER depends inversely on the actual error rate. For example, if the failure rate expected from simulation is 10^{-16} errors/s, which is a typical SER value for a single SRAM cell [3], the order of 10^{18} simulated events would be appropriate to achieve a statistical significance. Evidently, the huge sample sizes typically needed in the SER MC simulation preclude the direct use of a nuclear interaction or a semiconductor device simulation program. As shown in Fig. 7, we propose a methodology to run the MC simulations using HSPICE. A data set is generated pseudorandomly, each entry of which is composed of input vectors, particle-hit location, and pulse-current-source parameters. This data set is then provided to the HSPICE to perform data-driven transient simulations.

We conducted comparisons on a Dell Precision Workstation 650n (with Intel Xeon 2.8 GHz CPU and 1 GB RAM) running Redhat Linux. Table I shows the run times of SERA (t_{SERA}) and one million MC simulations (t_{MC}), as well as the difference between their SER results (ΔSER/SER) and run time speedup. We observe excellent matching (less than 4% difference) with 90 000×–180 000× speedup for three small circuits with 5, 8, and 11 gates, respectively. The total run time of MC circuit simulation grows so rapidly with the number of gates that it is impractical to simulate a 4 × 4 multiplier. SERA, on the other hand, can analyze large circuits as is evident from Table I.

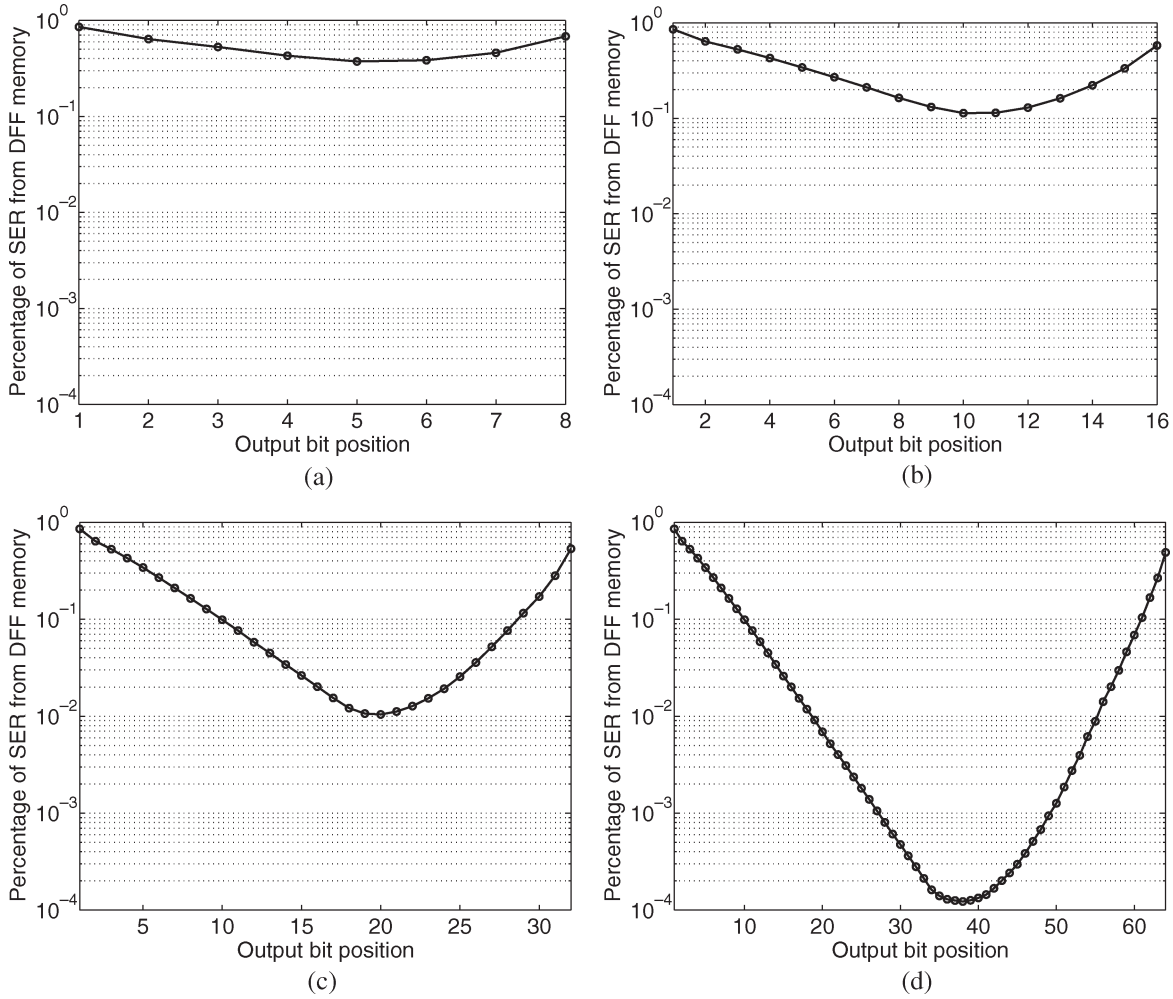

Fig. 11. Contribution of SER from DFF memory element at individual bit positions for multipliers of various sizes: (a) 4 × 4, (b) 8 × 8, (c) 16 × 16, and (d) 32 × 32.

B. Multiplier SER

We present the SER of multipliers as predicted by SERA. At sea level (New York City), the total neutron flux F is 56.5 $m^{-2}s^{-1}$ (see [21]). The sea level SER in units of failure in time is defined as the number of errors in 10^9 h. As stated earlier, the SER of combinational circuits is a function of the input-vector value, because the logical-masking mechanism changes with the input. Fig. 8 shows the importance of taking logical masking into account. Ignoring logical masking would have resulted in an unreasonable overestimation of the SER, especially for the MSBs. Fig. 9 shows the variation of SER with input-vector values. SER values for the center bits tend to spread more than the LSBs and the MSBs, because logical-masking mechanism varies more with input-vector values due to the large number of paths leading to those bits.

The SER averaged over 10 000 input-vector values are shown for individual bits of the parallel carry-save array multipliers of various sizes under nominal supply voltage and clock frequency in Fig. 10. Two factors influence the SER for an output bit: 1) the number of paths between the output bit and any internal circuit node and 2) logical masking. The former dominates for LSBs while the latter dominates for MSBs. This results in the peaking of individual bit SER at a bit position roughly two thirds of the full output precision away from the LSB. Fig. 11 shows the fraction of SER contributed by DFF memory element for multipliers of various sizes. As the size of the multiplier increases, less and less SER is contributed by the DFF memory element.

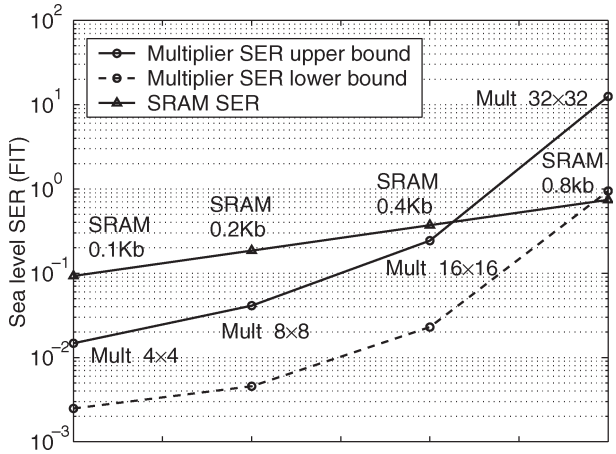

Fig. 12. Comparison between overall SERs of multipliers and SRAMs.

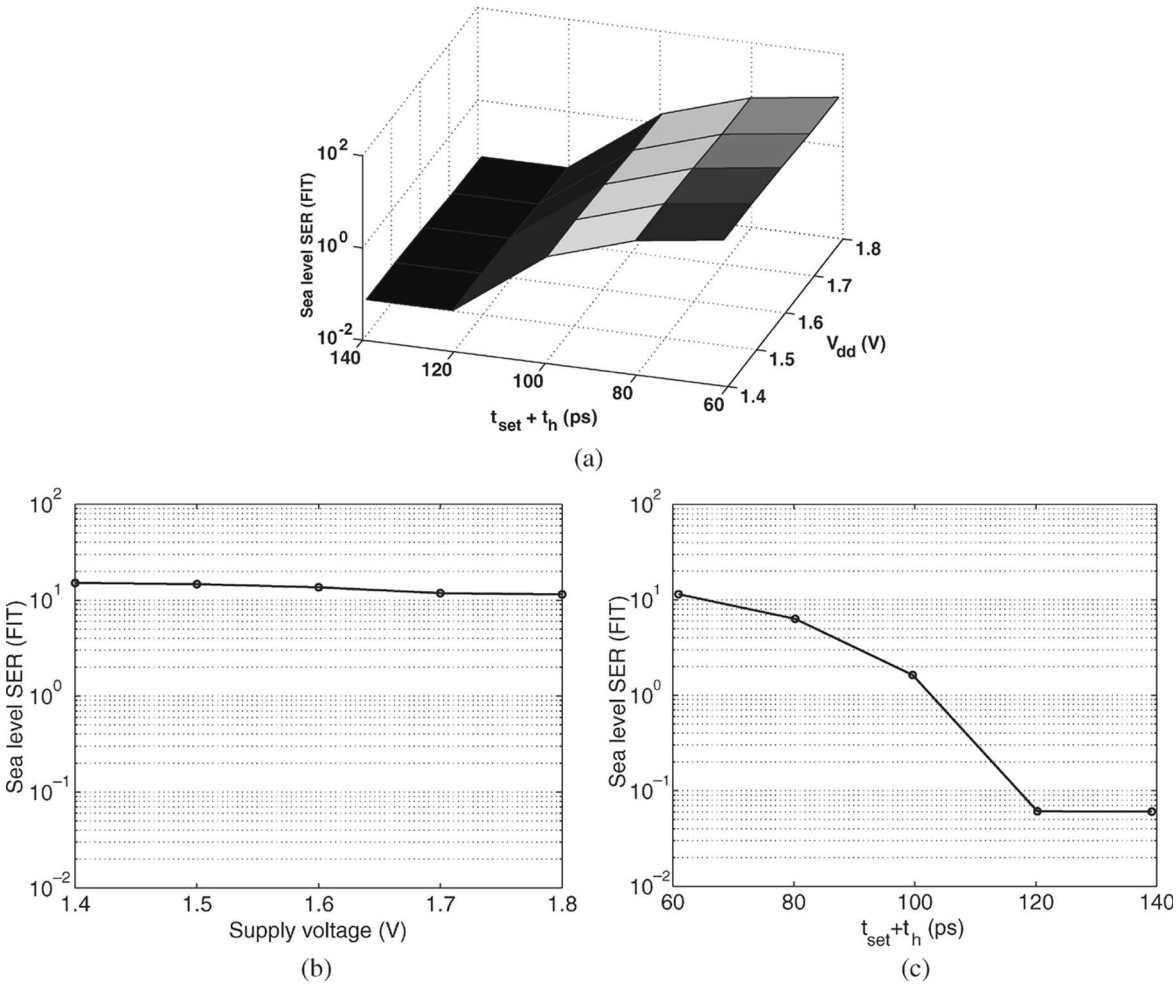

Fig. 13. SER upper bound of a 32 × 32 multiplier as function of $V_{\rm dd}$ and $t_{\rm set} + t_{\rm h}$. (a) Illustrative 3-D plot. (b) SER as function of $V_{\rm dd}$ when $t_{\rm set} + t_{\rm h} = 61$ ps. (c) SER as function of $t_{\rm set} + t_{\rm h}$ when $V_{\rm dd} = 1.8$ V.

Both upper and lower bounds on the overall SER are calculated from (2) and (6) as follows:

$$\max_i \text{SER}^{(i)} \leq \text{SER} \leq \sum_{i=1}^{B} \text{SER}^{(i)} \tag{26}$$

where B is the number of output bits. We use these bounds for plotting convenience. The results are compared with SRAMs of various sizes in Fig. 12. The SER lower bound of a 32 × 32 multiplier is close to the SER of a 1-kb SRAM in the same technology while its upper bound is close to SER of a 10-kb SRAM.

The SER of a 32 × 32 multiplier is further plotted as a function of supply voltage $V_{\rm dd}$ and DFF latching window $t_{\rm set} + t_{\rm h}$ in Fig. 13. For simplicity, only the SER upper bound is plotted. A wider latching window can very effectively decrease the error latching probability [see Fig. 4(b)] and hence the SER. The $P(\text{SE}|\text{HM})$ terms do not depend on latching window and start to dominate after $t_{\rm set} + t_{\rm h}$ is greater than roughly 120 ps so the reduction in SER thereafter becomes negligible. On the other hand, higher $V_{\rm dd}$ does result in a slight reduction of SER. This weak dependence of SER on $V_{\rm dd}$ is because the conditional probabilities are relatively weak functions of $V_{\rm dd}$ [see Fig. 4(c)]. In fact, the SER increases by more than 50× when $t_{\rm set} + t_{\rm h}$ is decreased by 20% from 120 ps, while it increases by only 28% when $V_{\rm dd}$ is decreased by 20% from 1.8 V.

C. Effect of Technology Scaling on SER

Impact of technology scaling on the SER of SRAM/latch circuits has been studied in existing literatures [3]. We attempt to reveal the correlation between technology scaling and the SER of combinational logic in this section. The SERs of multipliers of various sizes in an IBM 0.13-μm process technology were analyzed with an SERA. The results are shown in Fig. 14. The same SER peaking phenomenon can be observed for the multipliers as it is mainly determined by the logical-masking mechanism, which does not vary with the process technology. On the other hand, the electrical and latching window masking mechanisms do vary with the circuit parameters, which are closely related to process technology. This results in the change in the overall SER, as shown in Fig. 15. An increase of 0%–25% in SER for multiplier circuits of various sizes has been observed as technology scales from 0.18 to 0.13 μm. Please note that the SER of smaller circuits (such as a 4 × 4 multiplier) decreases slightly

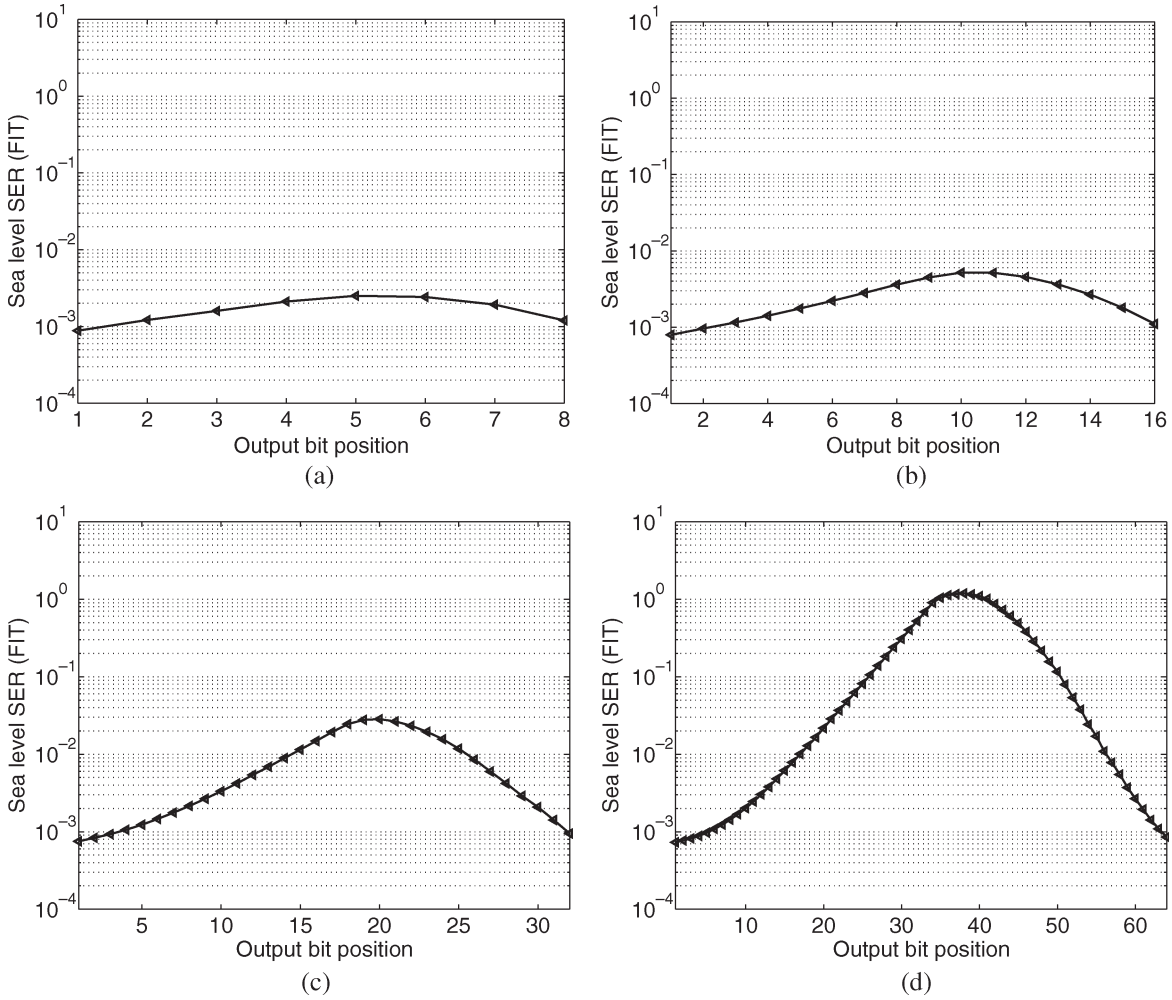

Fig. 14. SER at individual bits of multipliers of various sizes in 0.13-μm process technology: (a) 4 × 4, (b) 8 × 8, (c) 16 × 16, and (d) 32 × 32.

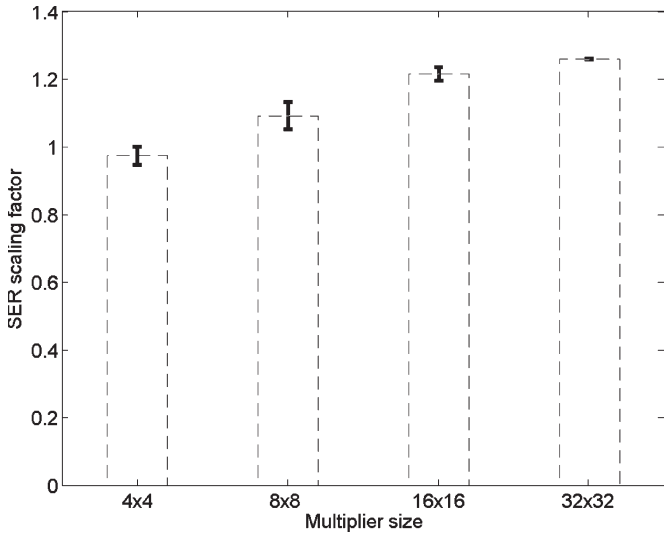

Fig. 15. SER scaling factor as process technology scales from 0.18 to 0.13 μm. (Upper edge of error bar corresponds to SER upper bound while lower edge corresponds to SER lower bound.)

for the newer technology because the reduction in the drain area overwhelms the increase in the conditional soft-error probabilities.

V. Conclusion

We present an SERA methodology for combinational and memory circuits. SERA is based on a modeling and analysis approach that employs a judicious mix of probability theory, circuit simulation, graph theory, and fault simulation. SERA achieves five orders of magnitude speedup over MC-based simulation approaches with less than 5% error. The proposed methodology reveals several interesting results such as: 1) the SER of combinational circuits is a much stronger function of the clock period and DFF latching window than supply voltage; 2) multipliers show an SER peaking phenomenon where the SERs of MSBs and LSBs are three orders of magnitude lower than those of the center bits; 3) SER of certain combinational circuits can be comparable to or exceed that of SRAMs with similar area; and 4) an increase of up to 25% in SER for multiplier circuits of various sizes has been observed as technology scales from 0.18 to 0.13 μm. SERA also points to several design guidelines for introducing a soft-error-tolerance in logic circuits, such as supply voltage tapering, increasing logic depth, and DFF setup time. Research in the area of a computer-aided design of soft-error tolerant circuits and systems is wide open. Our future work will focus on evaluating the impact of circuit styles on SER as well as characterization of SER of various

arithmetic units so that soft-error tolerant architectures and algorithms can be designed.

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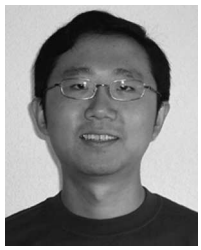

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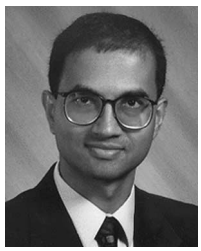

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