An Energy-efficient Circuit Technique for Single Event Transient Noise-Tolerance

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Abstract— **Presented is a circuit technique that mitigates the impact of single event transient (SET) noise in deep submicron (DSM) circuits with minimal speed, power and area penalty. The technique combines a novel dual-sampling flip-flop (DSFF) and a skewed CMOS (SCMOS) circuit style. The DSFF and SCMOS are designed to eliminate SETs with the polarity of 1-0-1 and 0-1-0, respectively. We present a case study of inverter chain circuits in a typical 0.18 μm process under the influence of radiation induced soft errors. We quantify the SET-tolerance of the proposed technique by simulating the circuits' soft error rate (SER) using a recently developed tool SERA (Soft Error Rate Analyzer). The results show that the DSFF latches the input without any speed penalty comparing to a conventional flip-flop, if no soft error has occurred. Otherwise, the DSFF alone eliminates the 1-0-1 SETs while incurring a worst-case speed and power penalty of 310 ps and 39 μW/GHz, respectively. The proposed technique can completely eliminate the impact of SETs with both polarities when tuned appropriately.**

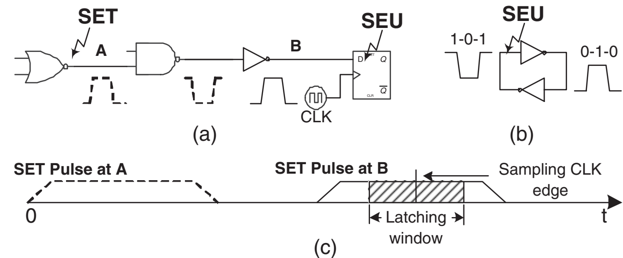

Fig. 1. Illustration of: (a) SET and SEU in a logic circuit, (b) SEU in the storage element of a flip-flop, and (c) timing diagram for propagation and capture of an SET.

I. Introduction

Noise has become a concern not only to analog and mixed signal designs, but also to modern microprocessors [1]. Technology scaling and aggressive design styles for achieving low power and high performance undermines the inherent noise immunity of digital circuits [2], [3]. Many noise sources present in microprocessors, such as soft errors caused by radiation events [4], are transient in nature. A radiation event such as a cosmic ray neutron hitting a semiconductor device, causes soft errors via two effects: single-event-upset (SEU) and single-event-transient (SET), as illustrated in Fig. 1. An SEU occurs in a memory cell or a flip-flop in its hold state when the contents of the storage element are flipped. An SET generates a transient noise pulse in a combinational circuit that may propagate to a flip-flop input and get latched. Functional failure may occur as a result of incorrect machine state stored. Prior work has shown that the soft errors, if uncorrected, result in a failure rate higher than all the other reliability mechanisms combined [4]. Another study shows that the soft error rate per chip of logic circuits will increase nine orders of magnitude from 1992 to 2011 [5]. It is important to develop design techniques for tolerating transient noise such as soft errors.

System level solutions have been used to provide soft error-tolerance, such as coding for error detection and correction (EDAC) in memory arrays [6] and triple modular redundancy (TMR) in logic [7]. However, these techniques tend to have a large performance and power penalty. Circuit level hardening techniques such as dual interlocked storage cell (DICE) [8], SER-tolerant latch [9], and switched-cap technique [10], are aimed at protecting the data from SEU. Recently, temporal sampling latch (TSL) [11] was proposed. It exploits the fact that a radiation induced SET has a pulse width typically less than a fixed value $\tau_{\max}$ (assumed to be 200 ps in [11]). It uses latch-level TMR and a four phase clock to eliminate both SEU and SET effects. The latch requires 107 transistors and a four phase clock generation circuitry, making multi-GHz designs complex and tricky. The presence of a three-input majority gate introduces additional delays to the data path, no matter whether there is a soft error event or not. For example, the latch latency penalty is at least 1 ns in 0.18 μm process technology, which is unacceptably high for multi-GHz designs. Furthermore, in the event of a soft error, there will be glitching (dynamic hazard) at the output of latch or flip-flop due to the voting mechanism, which in turn translates into more dynamic power consumption in both the latch or flip-flop itself and the down-steam logic circuits.

We present a simple and robust circuit design technique that mitigates the effect of SET with minimal speed, area and power penalty. The technique combines a novel dual-sampling flip-flop (DSFF) and skewed CMOS (SCMOS) combinational circuit to mitigate the impact of SETs with either polarity. The DSFF does not introduce any timing penalty when there are no soft errors; it will eliminate any 1-0-1 SETs while introducing a timing penalty that is slightly more than the maximum SET pulse width $\tau_{\max}$. The SCMOS can be tuned to eliminate 0-1-0 SETs. We show a case study of inverter chain circuits in a typical 0.18 μm process under the influence of radiation induced soft errors. We quantify the SET-tolerance of the proposed technique by simulating the circuits' soft error rate (SER) using a recently developed tool SERA (Soft Error Rate Analyzer) [12]. The results show that the DSFF latches the input without any speed penalty comparing to a conventional flip-flop, if no SET overlaps with the first transparency window of DSFF. Otherwise, the DSFF alone eliminates the 1-0-1 SETs while incurring a worst-case speed and power penalty of 310 ps and 39 μW/GHz, respectively. The proposed technique can completely eliminate the impact of SETs with both polarities when tuned appropriately.

This paper is organized as follows. In section II, we briefly review the flow of SERA and also describe the concept of error map. We then present the design details of DSFF and SCMOS, as well as simulation results, in section III. Finally, conclusions are made in Section IV.

II. SERA and Error Map

The previously developed soft error rate analyzer (SERA) is based on a modeling and analysis-based approach that employs a judicious mix of probability theory, circuit simulation, graph theory and fault simulation. SERA takes a circuit netlist and attaches time dependent pulse current source to possible particle strike nodes in a circuit at equally-spaced time instants. The overall SER is then computed based on a well-constructed probability space, after the circuit responses are simulated and combined with logic simulation results. Please refer to a recent publication [12] for more details on this topic.

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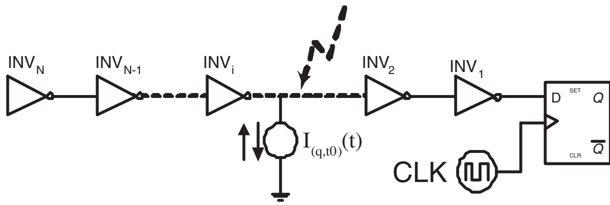

Fig. 2. Simulation set-up for studying the impact of SET on logic circuits.

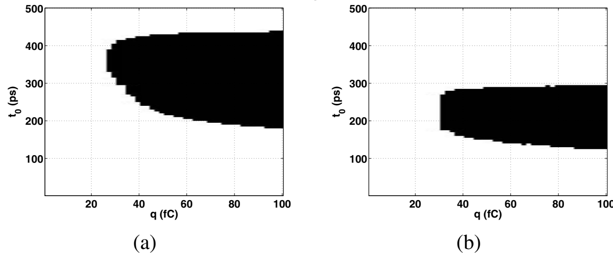

Fig. 3. Error maps for a neutron hit at the output of: (a) INV_1, and (b) INV_4.

To quantify the performance of proposed designs in this paper without significantly increasing the modeling complexity, we use SERA to analyze a flip-flop with its data input driven by an N-inverter chain circuit. SERA emulates a neutron hit by inserting the pulse current source with either polarity at one of the N possible locations, as shown in Fig. 2. The current source is assumed to take the following form [13]:

$$I_{(q,t_0)}(t) = \begin{cases} 0 & ,t < t_0 \\ \pm \frac{2q}{\tau\sqrt{\pi}}\sqrt{\frac{t-t_0}{\tau}}e^{-\frac{t-t_0}{\tau}} & ,t \geq t_0 \end{cases} \quad (1)$$

where q is the amount of collected charge, t_0 is the time instant at which a particle hits the node, and τ is a process technology-dependent time constant [14]. Note that the polarity of the current source is determined by whether the charge is collected by the drain of a PMOS or NMOS, as a drain node can collect only the minority carriers from the substrate or a well [15]. SERA then observes the value latched by the flip-flop with both parameters q and t_0 swept in the range $[0, Q_{\max}]$ and $[0, T_{\text{clk}}]$, respectively. The parameter $Q_{\max}$ is the maximum amount of collected charge and is assumed to be 100 fC in this work. The parameter T_{clk} is the clock period.

SERA reports an estimated SER for the circuit. For simplicity, we show only the probability of soft error given a particle hit on any of the inverter drain nodes, which is denoted $P(SE)$ in this work. Note that the $P(SE)$ term is proportional to SER [12]. We also use the aid of error maps to improve visibility into the designs. An error map, shown in Fig. 3 for a 4-inverter chain connected to a semidynamic flip-flop (SDFF) [17], is a two-dimensional plot showing error generating combinations of q and t_0. A black pixel in the error map corresponds to an error. The error maps in Fig. 3 indicate: a) errors occur if the collected charge at a specific node is large enough (e.g., $q > 30$ fC for INV_4) and the particle hit time t_0 lies between two specific values (e.g., 120 ps $\leq t_0 \leq$ 300 ps for INV_4) for a noise pulse to be captured by a latch, and b) neutron hits at drain nodes close to the flip-flop are more likely to cause errors.

III. SET-TOLERANCE TECHNIQUES

In this section, we propose and characterize circuit techniques for mitigating the impact of SETs. These techniques are based on a novel dual-sampling flip-flop and skewed CMOS circuit.

A. Dual-sampling Flip-flop

We propose a dual-sampling flip-flop (DSFF) as shown in Fig. 4. It is a pulsed flip-flop operating on the same principles as the hybrid

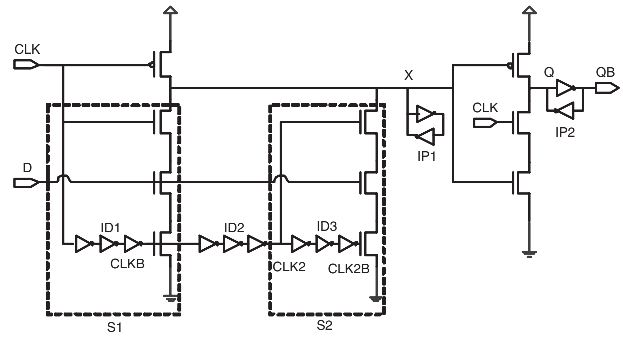

Fig. 4. Circuit schematic of the proposed DSFF.

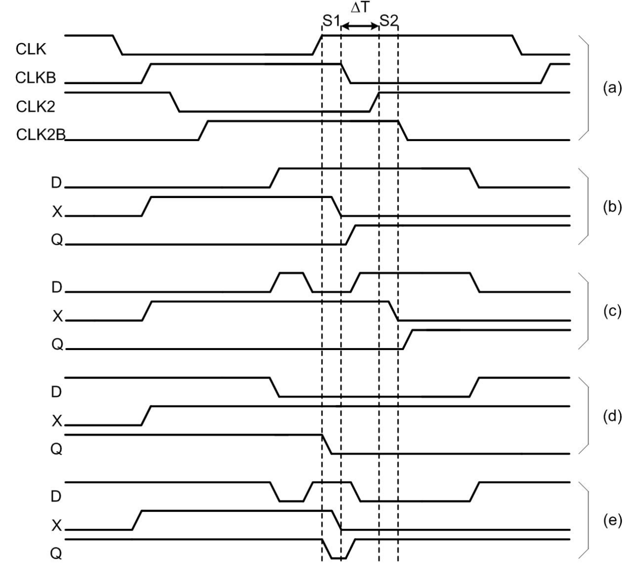

Fig. 5. DSFF timing diagram: (a) CLK signal and delayed CLK signals, (b) latching a one, (c) latching a one with a 1-0-1 SET, (d) latching a zero, (e) latching a zero with a 0-1-0 SET.

latch flip-flop (HLFF) [16] and the semidynamic flip-flop (SDFF) [17]. When *CLK* is low, node *X* is precharged high, as illustrated in Fig. 5. The flip-flop then utilizes a brief transparency period, determined by an integrated one-shot derived from the rising clock edge, to latch the data. This provides the flip-flop its edge-triggered nature as illustrated in Fig. 5(b) and (d).

The DSFF gets its SET-tolerance as a result of the dual sampling feature. As shown in Fig. 4, the transistors in box *S1* constitute the first sampler with a sampling window defined by signals *CLK* and *CLKB* (see Fig. 5(a)). The second sampler *S2* is identical to *S1* except that it is controlled by delayed versions of *CLK*. Note that each sampler has the same hold time t_{h}. The circuit configuration is such that the results of the two samplers are logically ORed. If the separation ΔT between the two sampling windows is made greater than $\tau_{\max}$ by sizing the inverter delay chain *ID2*, the DSFF will completely filter out SETs with 1-0-1 polarity at the input *D* of DSFF. This is because the signal at input *D* is high during at least one of the sampling windows and node *X* is always pulled low. Hence, correct latching of a one in the presence of a 1-0-1 SET is guaranteed.

However, the DSFF becomes more susceptible to a 0-1-0 SET than a SDFF. This is because the SET pulse overlapping with either of the two sampling windows would cause the voltage at node *X* to become low and stay there until the next precharge phase. This event can be seen in Fig. 5(e).

We compare DSFF, SDFF, and TSL in Table I. This comparison is justified because SDFF is a representative high-speed flip-flop, while

TABLE I
COMPARISONS OF FLIP-FLOPS.

	No. of Tr.	Worst-case latency (ps)	Power (μW/GHz)
DSFF	36	$t_{\rm h} + \tau_{\rm max} + t_{\rm CLK-Q} = 460$	265
SDFF	23	$t_{\rm CLK-Q} = 150$	226
TSL	107	$2{\cdot}t_{\rm h}{+}2\tau_{\rm max}{+}t_{\rm CLK-Q}{+}t_{\rm voter} = 1020$	955

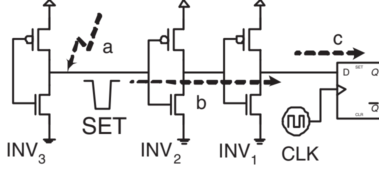

Fig. 6. The generation, propagation, and capture of an SET in a static balanced CMOS circuit with SDFF.

TSL is the state of the art in SET-tolerant flip-flop design. The worst-case delay for each flip-flop is written in terms of the hold time $t_{\rm h}$, maximum SET duration $\tau_{\rm max}$, and voter gate delay $t_{\rm voter}$. Note that we assume all the flip-flops are designed such that the setup time is zero. Compared to TSF, the speed penalty of the DSFF is smaller by 2.2X while consuming 3.6X less power. Specifically, the DSFF has the following advantages over TSL: a) compact structure and hence low power, b) simple clocking, c) a lower speed penalty, d) speed penalty exists only when a 1-0-1 SET reaches the DSFF's input and overlaps the first sampling window, and e) the voltage change at node *X* is unidirectional during evaluate phase and hence glitching is minimized. Compared to SDFF, DSFF has a 3X increase in worst-case latency and a 1.2X increase in power. Note that the speed penalty of DSFF is zero when no SET has occurred because only its first sampler is utilized to latch the input. We shall see later that the gain in SET-tolerance by using DSFF more than compensates for its speed and power penalty over SDFF.

B. Skewed CMOS

We propose to employ the skewed CMOS circuit technique [18] so that a 0-1-0 SET pulse is heavily attenuated before reaching the flip-flop inputs. Fig. 6 shows the three processes that jointly determine whether an SET pulse will be latched: (a) pulse generation, (b) pulse propagation and (c) pulse capture. Pulse generation and pulse propagation is determined by the transistor sizes. As the sizes increase, pulse generation is weakened but pulse propagation is strengthened. Pulse capture process depends on the propagated SET pulse magnitude, duration, and relative position with respect to the latching window.

Fig. 7 and Fig. 8 show the impact of scaling the transistor sizes in a conventional static CMOS circuit with balanced pull-up and pull-down paths (connected to an SDFF). Scaling up both NMOS and PMOS in all inverters by the same factor reduces the error probability by a factor of 10X when the transistor sizes are increased by a factor of 5X over a minimum sized balanced CMOS circuit. This is because increasing transistor sizes weakens the pulse generation process much more than it strengthens the pulse propagation process.

Figure 9 illustrates the skewed CMOS circuit style [18]. In skewed CMOS, either the NMOS or the PMOS transistors (indicated by an adjacent arrow in Fig. 9) are sized-up by a factor of k. Note that we do not precharge the intermediate nodes as in [18]. This type of skewed scaling results in 0-1-0 transients being significantly weakened at the flip-flop input. The 1-0-1 transients get slightly stronger because the propagation process is strengthened while the generation process is weakened. Fig. 10 shows the error maps for both 0-1-0 and 1-0-1 SETs before and after the skewed scaling. The impact of skewed scaling is also shown in Fig. 11. The $0 \rightarrow 1$ error probability

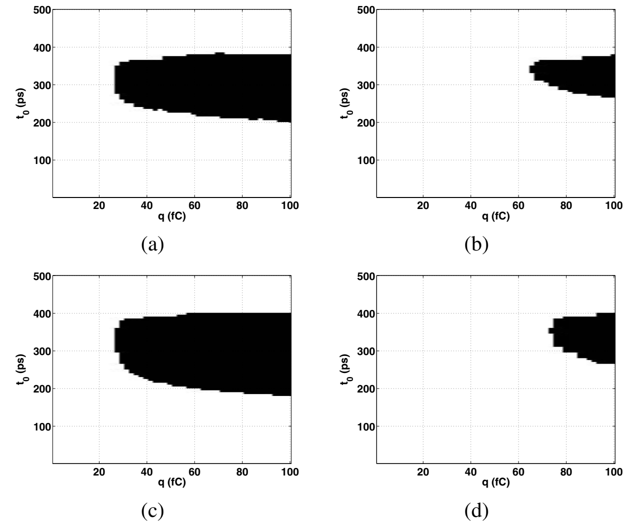

Fig. 7. Error maps for a neutron hit at the output of INV_2 in a static balanced CMOS circuit with SDFF for: 0-1-0 SET when scaling factor is (a) one and (b) three, and 1-0-1 SET when scaling factor is (c) one and (d) three.

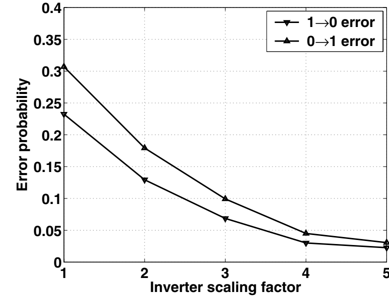

Fig. 8. Error probability as a function of inverter scaling factor in a 4-inverter balanced CMOS circuit with SDFF.

decreases by a factor of 10X when the skewing factor is greater than 3 and becomes zero when the skewing factor is 4. The $1 \rightarrow 0$ error probability increases by a factor of 1.8X at a skewing factor of 5. Simulations also show that only the last three stages of the inverter chain need to be skewed by the factor of 4 to eliminate $0 \rightarrow 1$ errors caused by SETs generated at the output of any inverter. This is because the weakening of pulse propagation process alone is sufficient to attenuate the SETs generated at an inverter far away from the flip-flop input.

C. Skewed CMOS with DSFF

As DSFF and skewed CMOS mitigate or eliminate 1-0-1 and 0-1-0 SETs, respectively, their combination could mitigate or eliminate SETs with both polarities. This fact is verified via simulation in Fig. 12, where a skewed 4-inverter circuit with a DSFF is employed. The 1-0-1 SETs are inherently tolerated by the DSFF. When the skewing factor reaches 4, all 0-1-0 SETs are eliminated. Driven by a 1 GHz clock, the DSFF alone causes 310 ps worst-case speed penalty

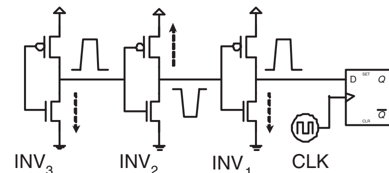

Fig. 9. Skewed CMOS circuit style that attenuates 0-1-0 SET pulses at the flip-flop input.

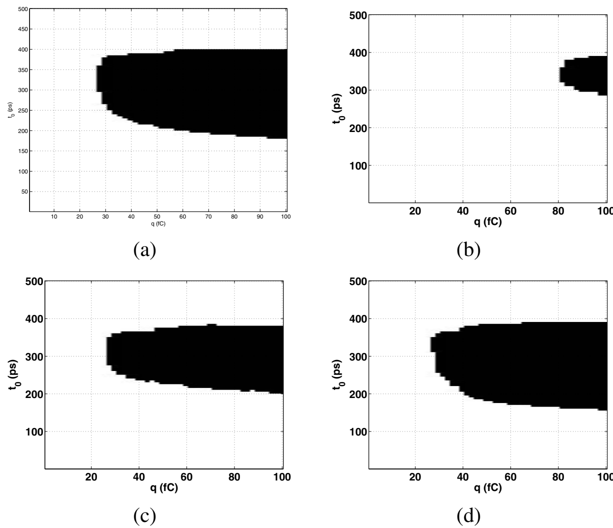

Fig. 10. Error maps for a neutron hit at the output of INV_2 in skewed CMOS circuit (with SDFF) for: 0-1-0 SET when the skewing factor is (a) one and (b) three, 1-0-1 SET when the skewing factor is (a) one and (b) three.

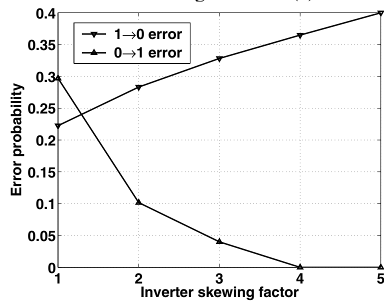

Fig. 11. Error probability as a function of skewing factor in a 4-inverter skewed CMOS circuit (with SDFF).

and 39 μW power penalty. The skewed CMOS circuit causes 110 ps speed penalty and 160 μW power penalty, comparing to a minimum-sized balanced 4-inverter chain circuit. On the other hand, scaling up both PMOS and NMOS transistors in the balanced inverter chain by a factor of 5 could reduce the error probability by a factor of 6 while inducing a large power penalty of 510 μW. The proposed technique is clearly an energy-efficient design for tolerating transient noise.

Simulation results in Fig. 13 further show that the proposed technique is very robust when the supply voltage is reduced. The error probability remains bounded below 0.05 even when the supply voltage is as low as 1.4 V. Note that this slight increase in error probability at low supply voltage can be eliminated by increasing the ΔT parameter of the DSFF and the skewing factor of the CMOS circuit.

IV. Conclusions

This paper describes a novel approach to eliminate radiation induced single-event-transient effect in logic circuit. We propose a dual-latching flip-flop and skewed CMOS combinational circuit style. In TSMC 0.18 μm process, the DSFF alone causes 310 ps worst-case speed penalty and 39 μW/GHz power penalty. The skewed CMOS circuit causes 110 ps speed penalty and 160 μW/GHz power penalty, for a 4-inverter chain circuit. Simulations show the proposed technique is much more energy efficient than using temporal sampling latch or scaling up balanced inverters.

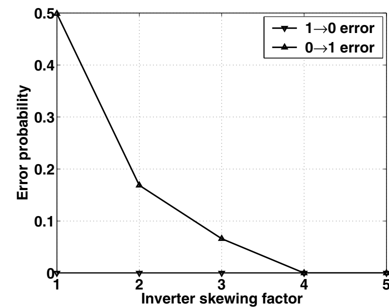

Fig. 12. Error probability vs. inverter skewing factor in a 4-inverter chain for the proposed circuit (DSFF with $t_{\mathrm{h}} = 110$ ps, $\Delta_T = 200$ ps).

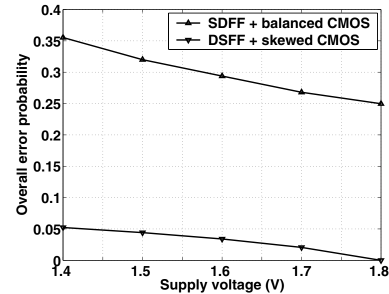

Fig. 13. Overall error probability (average of $0 \rightarrow 1$ and $1 \rightarrow 0$ error probabilities) as a function of the supply voltage in a 4-inverter CMOS circuit.

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