SIMPLIFIED CURRENT AND DELAY MODELS FOR DEEP SUBMICRON CMOS DIGITAL CIRCUITS

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ABSTRACT

This paper presents a model for estimating the drain current in deep submicron (DSM) CMOS devices based on Sakurai and Newton's [1] work, and hence is referred to as the modified SN-model. The proposed model preserves the simplicity of the SN-model while providing accurate drain current estimates for varying device widths. Manually computed current and delay values for inverter circuits via the proposed model match SPICE level 49 within 1.2% average (3% maximum) error in 0.25 μm and 0.18 μm CMOS processes over a wide range of transistor widths, fanouts, and input rise/fall times. A generalized delay model for circuits with interconnect is also proposed with accuracy within 3% error over a wide range of buffer sizes and interconnect lengths. The proposed model has been successfully incorporated into a senior level circuit design course at the University of Illinois at Urbana-Champaign.

1. INTRODUCTION

Accurate drain current and propagation delay modeling for DSM CMOS circuits is essential in the design and analysis of high-performance digital integrated circuits. Typically, circuit designers employ quick manual calculations in order to estimate the delay and power, which are then followed by more accurate but time consuming SPICE simulations. The Shichman and Hodges [2] classical quadratic current model for MOSFETs is widely used for manual calculations mainly due to its simplicity. However, in DSM process technologies, i.e., for 0.35 μm and below, this model gives errors in delay estimation that can be as high as 64%[1] when compared to SPICE latest models. The purpose of this paper is to propose a device model that is similar in complexity to the Shichman and Hodges [2] model but provides a high degree of accuracy when compared to SPICE level 49.

The Shichman and Hodges [2] is not accurate for short-channel transistors because it neglects carrier velocity saturation. Sakurai and Newton [3] proposed the α-power law model that takes into account short-channel behavior. However, the α-power law model was not sufficiently accurate, and an improved nth-power law model [1] (henceforth referred to as the *SN-model*) with additional parameters was proposed later. The SN-model provides sufficiently accurate estimates of the drain current when compared to SPICE level 3 [1], [4]. However, in the DSM regime, SPICE level 3 [4] models are no longer accurate. Furthermore, the SN-model is not accurate in describing the relationship between the current and the transistor width (as shown in Figure 3(a)). The *constant* transconductance parameter in this model leads to inaccurate drain calculations and, hence, delay calculations, when the transistor width is varied.

In [5] and [6], a simple closed-form formula for the propagation delay of a CMOS inverter circuit was derived. Several authors [6]-[8] have developed comprehensive delay models by introducing empirical parameters. These equations depend highly on physical parameters. Others have modeled the transistor netlist by using an RC equivalent [9] and derived an analytical expression for the output waveform. However, these models are highly empirical, more complex than the SN-model, and have been compared with SPICE level 3 [6]-[9]. Hence these models give inaccurate results when compared with SPICE level 49.

2. DRAIN CURRENT MODEL

We present below the drain current expressions for both the SN-model [1], [3] and the proposed modified SN-model:

SN-model

$$I_{DSAT} = \frac{W}{L_{eff}} B\,(V_{GS} - V_{TH})^{\alpha}\,(1 + \lambda V_{DS}), \tag{1}$$

$$I_{DLIN} = \frac{W}{L_{eff}} B\,(V_{GS} - V_{TH})^{\alpha} \left(2 - \frac{V_{DS}}{V_{DSAT}}\right) \frac{V_{DS}}{V_{DSAT}}, \tag{2}$$

Modified SN-model

$$I_{DSAT} = K\,(V_{GS} - V_{TH})^{\alpha}\,(1 + \lambda V_{DS}), \tag{3}$$

$$I_{DLIN} = K\,(V_{GS} - V_{TH})^{\alpha} \left(2 - \frac{V_{DS}}{V_{DSAT}}\right) \frac{V_{DS}}{V_{DSAT}}, \tag{4}$$

$$K = \beta_1 + \beta_2 W + \beta_3 W^2, \tag{5}$$

where in both models

$$V_{DSAT} = V_{DSAT_1} \left(\frac{V_{GS} - V_{TH}}{V_{DD} - V_{TH}}\right)^{0.5\alpha}, \tag{6}$$

$$V_{DSAT_1} = V_{DSAT}|_{V_{GS}=V_{DD}}, \tag{7}$$

and $1 \leq \alpha \leq 2$ is the velocity saturation index, B is the transconductance parameter, L_{eff} is the effective length, V_{TH} is the threshold voltage, V_{DD} is the supply voltage, λ is the channel length

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[1] For 0.25 μm process technology with $W = 0.36\,\mu$m, $L = 0.24\,\mu$m, and the remaining parameters are as described in Table 1.

modulation factor, V_{GS} and V_{DS} are the gate-source and drain-source voltages, respectively. The voltage V_{DSAT} determines the boundary between linear and saturation regions. The transconductance parameter in (5) (henceforth called the K parameter) is a width-dependent coefficient. It's values are derived from the slope of the curve in the $I_{eff}^{1/\alpha}$ *vs.* V_{GS} plots using (3), where $I_{eff} \triangleq I_D/(1 + \lambda V_{DS})$. The coefficients ($\beta_1$, β_2, and β_3) in (5) are then determined by fitting a quadratic to the K *vs.* W plot.

According to (1) and (2), the drain current is directly proportional to the transistor gate width (B is constant). Figure 1 shows that the SN-model is inaccurate when compared to the SPICE level 49 models especially as the transistor widths increase. The SN-model parameters were derived as described in [1] for transistor widths of 0.36 μm and 0.22 μm for the 0.25 μm and 0.18 μm process technologies, respectively. These parameters are then used to calculate the drain currents for larger widths. This inaccuracy is mainly due to the nonlinear effects of vertical and lateral high field mobility degradation and velocity saturation. Circuit designers typically need accurate current estimates for various widths. Thus, there is a need for a model that preserves the simplicity of the SN-model while improving its accuracy.

The proposed model parameters derived for the NMOS and PMOS devices are listed in Table 1. As shown in the plots in Figure 2 the proposed model matches SPICE level 49 simulations for different transistor widths and input voltages with a high degree of accuracy.

3. INVERTER DELAY ESTIMATION

We estimate the propagation delay (T_P) of a simple CMOS inverter which is driven by an input rise/fall time of T_{IN}. This delay model is given by [10]:

$$T_P = \left[\frac{v_{TH} + \alpha}{1 + \alpha} - \frac{1}{2}\right] T_{IN} + \frac{C_T V_{DD}}{2 I_D}, \tag{8}$$

where $v_{TH} = V_{TH}/V_{DD}$, C_T is the total capacitance discharged, T_{IN} is the input rise/fall time, and I_D is the drain saturation current with $V_{GS} = V_{DD}$.

We employed the modified SN-model as well as the SN-model to calculate the current I_D in (8) for inverters with varying device widths, input rise times, and load capacitances. We compare in Table 2, the simulated and calculated values of delay for the modified SN-model, and the SN-model [1], for 0.25 μm and 0.18 μm CMOS technologies. The SN-model parameters were derived for minimum-sized transistors in both technologies. As seen in Table 2, the modified SN-model has an average error of 1.16% with a maximum of 2.72% and a standard deviation of 0.83%. In contrast, the SN-model achieves an average error of 11.4% with a maximum of 23.5% and a standard deviation of 8.18%. Note that the SN-model gives accurate results only when the device widths are minimum sized.

4. CIRCUITS WITH INTERCONNECT

The parasitic resistance of a metal or polysilicon line can have a significant influence on the signal propagation delay over the line. First, the delay with zero line resistance (T_{P0}) is estimated using the delay expression in (8) and substituting for C_T the sum of the interconnect capacitance (C_{INT}), the device's parasitic capacitances (C_D), the effective gate capacitance (C_G), and the output load capacitance (C_L). If the interconnect resistance (R_{INT}) is not zero and if the metal or polysilicon line is used for local interconnect (i.e., the interconnect delay is not the dominating delay factor), a simple π model can be used [11]. This model places half the interconnect capacitance at the driver output and half at the load. These capacitances are separated by the interconnect resistance. Assuming a ramp input, the gate delay expressions with interconnect are as follows [12]:

$$T_P = T_{P0} + \frac{T_{INT1} T_{INT2}}{T_{INT1} + T_{INT2}} = T_{P0} + T_{LINT} \tag{9}$$

$$T_{INT1} = R_{INT}(C_D + C_{INT}/2), \tag{10}$$

$$T_{INT2} = R_{INT}(C_L + C_{INT}/2). \tag{11}$$

The added delay due to the line resistance, namely local interconnect delay (T_{LINT}), is therefore the final term in (9). The model in (9) is called the TLINT model.

For long interconnects, where the interconnection delay becomes a dominant delay factor, the added delay is approximately that of a step input driving a distributed RC wire. The delay analysis of such RC networks requires either SPICE simulations or other delay calculation methods such as the *Elmore delay formula* [11]. The gate delay with interconnect then becomes

$$T_P = T_{P0} + T_{GINT} \tag{12}$$

$$T_{GINT} = R_{INT}(0.38 C_{INT} + 0.69 C_L). \tag{13}$$

The model in (12) is called the TGINT model. The plots in Figure 3(a) compare the TLINT (9) and TGINT (12) delay models through a 10-μm polysilicon line to SPICE simulations for a wide range of driver sizes. As shown from the plots, the TLINT model fits SPICE simulation results for large buffer sizes while not performing well, as expected, for smaller buffer sizes, where the interconnect delay is comparable to the buffer delay. The opposite is true for the TGINT model. It can be inferred from the plots that a general model can be obtained by taking a weighted average between the local interconnect model (TLINT) and the global interconnect model (TGINT). Hence, we propose the general interconnect model called the TINT model as follows:

$$\begin{aligned} T_P &= T_{P0} + \frac{T_{P0}}{T_{P0} + T_{LINT}} T_{LINT} + \frac{T_{LINT}}{T_{P0} + T_{LINT}} T_{GINT} \\ &= T_{P0} + \frac{T_{P0} + T_{GINT}}{1 + T_{P0}/T_{LINT}}. \end{aligned} \tag{14}$$

Shown in the plots in Figure 3(a) are the delay calculation results using (14) with the SN-model (1)-(7) and the modified SN-model (3)-(5) employed to calculate T_{P0}. For small buffer sizes, the SN-model results were 14% smaller than those obtained by SPICE. This error decreases as the interconnect delay dominates over that of the device. On the other hand, the TINT model using the modified SN-model to calculate T_{P0} gives a maximum error of 2.6%. Figure 3(b) compares the equivalent input slew rate (T_{IN2}) found using SPICE to the results of (14) using the modified SN-model for a size 1 inverter driving a size 4 inverter through various wire lengths. As shown from the plots, the general interconnect model was able to predict the SPICE simulation results over the range of interconnect lengths.

5. CONCLUSION

This paper provides a current model that accurately expresses the DSM CMOS $I - V$ characteristics. The delay predicted by the

Table 1: Modified SN-model parameter values.

	0.25 μm CMOS Process		0.18 μm CMOS Process	
Parameters	NMOS	PMOS	NMOS	PMOS
V_{TH0} (V)	0.560	-0.51	0.555	-0.450
λ (V^{-1})	0.049	0.150	0.069	0.139
γ $(V^{1/2})$	0.440	0.490	0.460	0.606
$2\phi_f$ (V)	0.860	0.880	0.886	0.880
β_1	31.23×10^{-6}	6.885×10^{-6}	2.088×10^{-5}	-4.72×10^{-8}
β_2	209.8	66.06	422.5	118.0
β_3	1.951×10^{6}	523.2×10^{3}	2.170×10^{6}	3.266×10^{6}
α	1.224	1.380	0.930	1.475
V_{DSAT_1} (V)	1.200	-1.286	1.000	-1.120
V_{DSAT} (V)	$0.8(V_{GS}-V_{TH})^{0.5\alpha}$	$0.8(V_{GS}-V_{TH})^{0.5\alpha}$	$0.9(V_{GS}-V_{TH})^{0.5\alpha}$	$0.9(V_{GS}-V_{TH})^{0.5\alpha}$

model is very close to that produced by SPICE level 49 simulations. The model is supported through comparison between calculated and simulated values of the current drawn and propagation delays of different CMOS circuits over a large range of gate widths, loads with and without interconnect, and input ramp durations. By using SPICE level 49 electrical simulations for 0.25 μm and 0.18 μm processes as reference, we have shown that the models can be scaled across technology. The proposed models base their validity on a set of process parameters that can be extracted directly from the SPICE models and experimental measurements.

Table 2: T_{PHL} results for different inverter circuit configurations.

W_n [μm]	T_{IN} [ps]	C_L [fF]	SPICE [ps]	MSN* [ps]	SN** [ps]	Error1 [%]	Error2 [%]
0.25 μm technology†							
0.36	50	50	289.8	287.5	286.2	0.81	1.23
		100	520.4	519.0	516.7	0.28	0.71
	100	50	297.7	295.0	293.8	0.90	1.31
		100	528.5	526.5	524.3	0.37	0.79
1.44	50	50	104.1	103.4	82.75	0.71	20.5
		100	179.8	176.8	140.4	1.67	21.9
	100	50	111.4	110.9	90.32	0.41	18.9
		100	187.1	184.4	147.9	1.46	20.9
2.88	50	50	60.37	62.01	48.83	2.72	19.1
		100	99.61	100.0	77.64	0.42	22.1
	100	50	67.63	69.59	56.40	2.89	16.6
		100	106.8	107.6	85.21	0.75	20.2
4.32	50	50	45.06	46.24	36.53	2.61	18.9
		100	71.52	72.67	56.73	1.61	20.7
	100	50	52.31	52.80	40.98	0.94	21.7
		100	78.69	80.64	60.23	2.48	23.5
0.18 μm technology‡							
0.22	45	45	313.3	313.4	317.0	0.03	1.18
		75	498.4	492.7	498.4	1.15	0.00
	75	45	317.7	317.6	321.3	0.02	1.12
		75	502.9	496.9	502.6	1.19	0.05
0.88	45	45	92.34	94.47	87.39	2.30	5.36
		75	142.9	143.8	132.7	0.62	7.12
	75	45	97.33	98.72	91.64	1.43	5.85
		75	147.9	148.0	137.0	0.09	7.38
1.76	45	45	53.14	54.55	49.12	2.65	7.57
		75	79.66	80.11	71.79	0.56	9.88
	75	45	58.34	58.80	53.37	0.79	8.52
		75	88.50	87.45	76.04	1.19	14.1
2.64	45	45	37.79	38.11	34.36	0.85	9.07
		75	55.22	55.61	48.48	0.71	12.2
	75	45	42.78	43.35	38.06	1.34	11.0
		75	60.18	60.86	50.73	1.13	15.7
					Average Error	1.16	11.4
					Standard Deviation	0.83	8.18

* MSN=Modified SN-Model

** SN=SN-Model

† $W_p = 1.44\ \mu$m and $B = 7.165 \times 10^{-5}$ for SN-model.

‡ $W_p = 0.88\ \mu$m and $B = 8.830 \times 10^{-5}$ for SN-model.

6. REFERENCES

[1] T. Sakurai and A. R. Newton, "A simple MOSFET model for circuit analysis," *IEEE Transactions on Electron Devices*, vol. 38, no. 4, pp. 887-894, April 1991.

[2] H. Shichman and D. A. Hodges, "Modeling and simulation of insulated-gate field-effect transistor switching circuits," *IEEE Journal of Solid-State Circuits*, vol. 3, no. 2, pp. 584-594, April 1990.

[3] T. Sakurai and A. R. Newton, "Alpha-power law MOSFET model and its applications to CMOS inverter delay and other formulas," *IEEE Journal of Solid-State Circuits*, vol. 25, no. 2, pp. 584-594, April 1990.

[4] T. Quarles, A. R. Newton, D. O. Pederson, and A. Sangiovanni-Vincentelli, *SPICE 3B1 User's Guide*, EECS, University of California at Berkeley, 1998.

[5] A. Chatzigeorgiou and S. Nikolaidis, "A modeling technique for CMOS gates," *IEEE Transactions on Computer-Aided Design of Integrated Circuits and Systems*, vol. 18, no. 5, pp. 557-575, May 1999.

[6] K. A. Bowman, B. Austin, J. Eble, X. Tang, and J. Meindl, "A physical α-power law MOSFET model," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 10, pp. 1410-1414, October 1990.

[7] J. Daga and D. Auvergne, "A comprehensive delay macro modeling for submicrometer CMOS logics," *IEEE Journal of Solid-State Circuits*, vol. 34, no. 1, pp. 42-55, January 1999.

[8] H. Chow and W. Feng, "An analytical CMOS inverter delay model including channel-length modulations," *IEEE Journal of Solid-State Circuits*, vol. 27, no. 9, pp. 1303-1306, September 1992.

[9] H. Park and M. Soma, "Analytical model for switching transitions of submicron CMOS logics," *IEEE Journal of Solid-State Circuits*, vol. 32, no. 6, pp. 880-889, June 1997.

[10] T. Sakurai, "CMOS inverter delay and other formulas using alpha-power law MOS model," in *IEEE International Conference on Computer-Aided Design*, November 1988, pp. 74-74.

[11] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective*. Upper Saddle River, NJ: Prentice-Hall, 1996.

[12] T. Sakurai, "Closed-form expressions for interconnection delay, coupling, and crosstalk in VLSI's," *IEEE Transaction on Electronic Devices*, vol. 40, no. 1, pp. 118-124, January 1993.

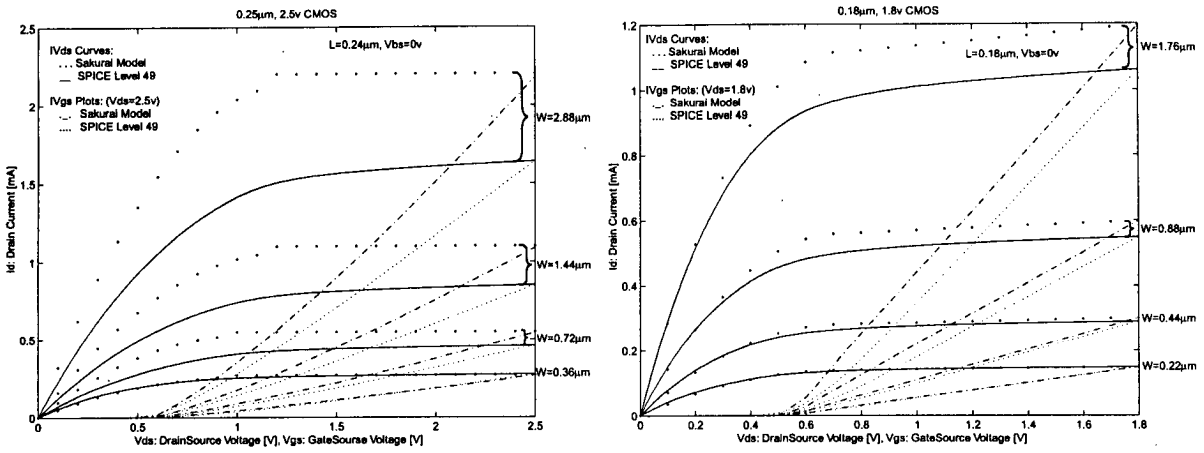


Figure 1: SN-model $I - V$ plots.

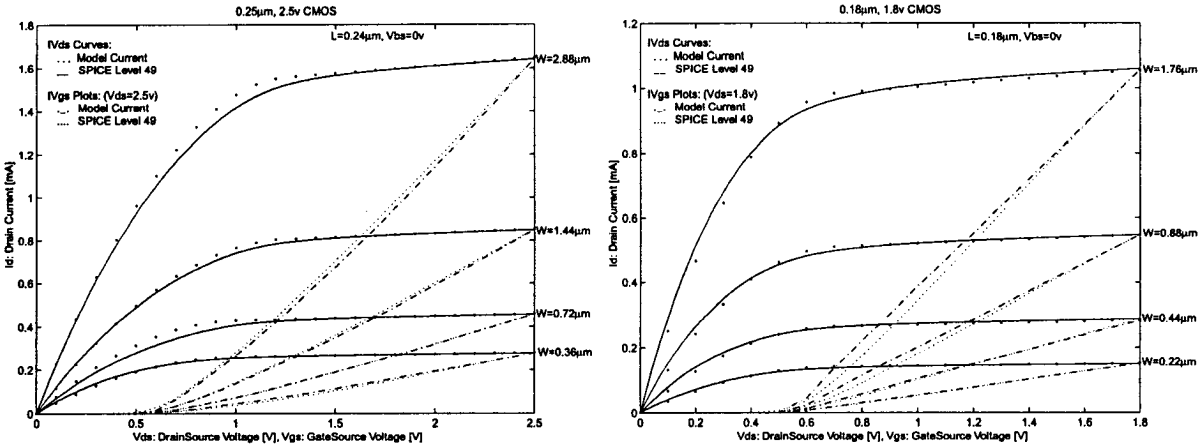
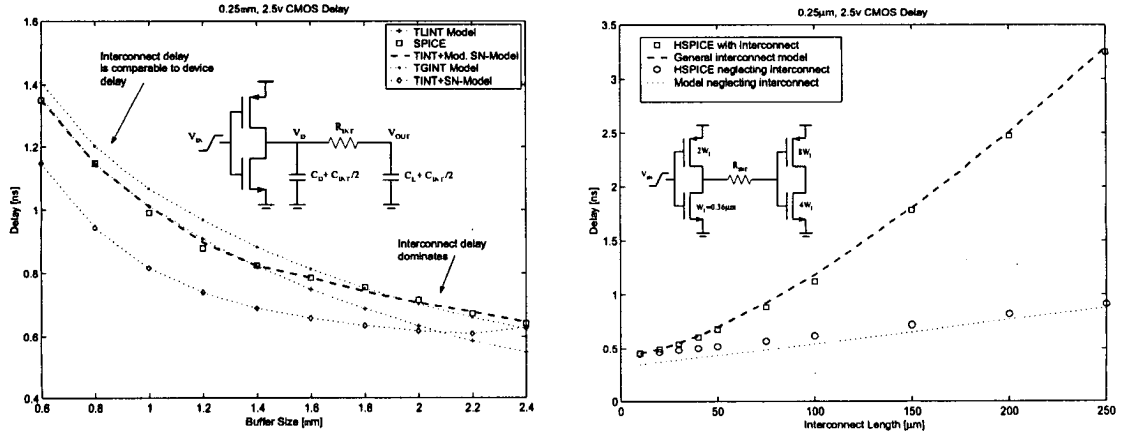


Figure 2: Modified SN-model $I - V$ plots.



(a) (b)

Figure 3: Inverter delay with wire resistance for (a) different buffer sizes and (b) wire lengths.