High Bandwidth Transimpedance Amplifier Design Using Active Transmission Lines

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***Abstract*— A transimpedance amplifier (TIA) is designed based on the first order wave equation. The feedback resistance is set as the objective function for transimpedance. The main feedback amplifier provides transimpedance and a wide band compensation amplifier determines the characteristics of overall TIA. The stability of the TIA is not affected due to the open loop nature of compensation. Simulation results show that the TIA achieves a 58 dB gain and 1.32 GHz bandwidth in a 0.25 μm standard CMOS process.**

***Index Terms*— TIA, wave equation, active transmission lines**

I. Introduction

A lossless transmission line can be described as

$$\frac{\partial^2 u(x,t)}{\partial t^2} = c^2 \frac{\partial^2 u(x,t)}{\partial x^2}, \tag{1}$$

which is called a wave equation where t and x represents the time and space axis, respectively. The equation consists of two terms, one of which is propagating to the right (positive x) and the other to the left. The first order wave equation that propagates to the right is given by

$$\frac{\partial u(x,t)}{\partial t} = -c \frac{\partial u(x,t)}{\partial x}. \tag{2}$$

The general solution of above equation is $f(x+ct)$, implying that a wave is propagating at a speed c. In reality, an ideal integrator required to implement (2) is not feasible. However, the above equation can be written in an implementable form as follows

$$u(x,t) + \frac{1}{p}\frac{\partial u(x,t)}{\partial t} = -A \frac{\partial u(x,t)}{\partial x}, \tag{3}$$

where A is the gain of the amplifier and p is the 3-db pole location. With an initial condition of $u(0,t) = asin(wt)$, $u(0,0) = 0$ and $u'(0,0) = 0$, we solve (3) to get

$$u(x,t) = ae^{-pt} sin(t - \frac{x}{w_{unity}}), \tag{4}$$

where w_{unity} is the unity gain frequency of the amplifier. From (4), it is clear that a non-ideal integrator attenuates the input signal and the degree of attenuation is determined by the 3-db pole location p. Also from (4), the propagation speed of the wave is determined by the unity gain frequency w_{unity}. Equations (3),(4) describe an *active transmission line*.

However, in order to implement (3), we discretize the derivative. Considering stability, we set $\frac{\partial u}{\partial x} = \frac{u_n - u_{n-1}}{h}$ where $u_n = V_o$(the output node) and $u_{n-1} = V_{in}$(the input node). Then (3) becomes

$$u_n + \frac{1}{p}\frac{\partial u_n}{\partial t} = -A'(u_n - u_{n-1}), \tag{5}$$

where $A' = \frac{A}{h}$. Equation (5) is the description of a unity-gain feedback amplifier. The dispersion relation can be found by substituting

$$u_n = ae^{j(kn+wt)} \tag{6}$$

in (5) to obtain

$$w = \frac{A'p}{j}(e^{-jk} - 1 - \frac{1}{A'}). \tag{7}$$

By substituting (7) into (6), we get gain factor G given by,

$$G = \frac{A'p}{p(A'+1) + jw}. \tag{8}$$

The truncation error T of (5) is found by using Taylor expansion at u_n which is given by

$$T = a(\frac{1}{2}hu_{xx} - \frac{1}{3!}(h)^2 u_{xxx} \cdots), \tag{9}$$

where u_{xx} and u_{xxx} are the second and third order spatial derivatives of $u(x,t)$, respectively. It is clear that a unity gain feedback amplifier is highly dispersive because all the high order terms appear.

II. High Bandwidth TIA Design

In this section, a transimpedance amplifier (TIA) will be configured using an active transmission line and a design procedure will be presented. A TIA is used to convert the current into voltage. The TIA requirements are high bandwidth (0.7 times the data rate), high gain, low noise ($<$ 1 mA). A simple resistor is a transimpedance device but it is not effective in terms of gain-bandwidth product. The capacitance of the photo detector (PD) and that of the bonding pad make the input node a dominant pole location.

A single-stage TIA has sufficient phase margin and robustness to substrate coupling noise [1] but the bandwidth is usually smaller than a two stage design. However, a two-stage design has several drawbacks. Addition of the second stage adds an additional pole and reduces the phase margin. Also it is hard to increase the open-loop gain because of the limited voltage headroom. Capacitor peaking [2] can increase the bandwidth but stability becomes a problem.

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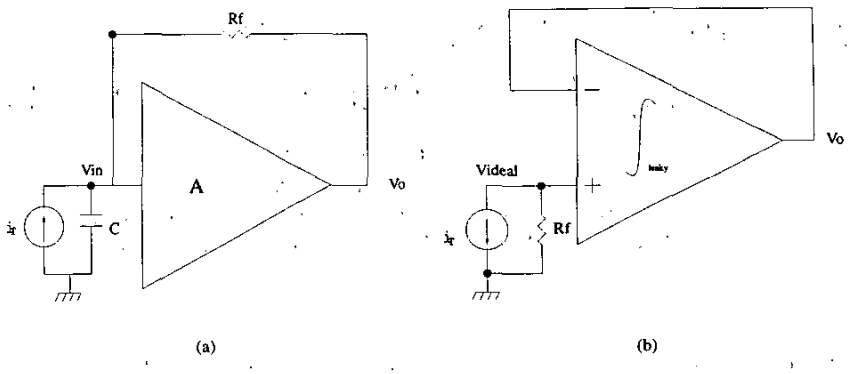

Fig. 1. A transimpedance amplifier:(a) a conventional TIA design, and (b) an equivalent representation.

In a conventional TIA in Fig. 1(a), the dominant pole is located at the input node. Assuming that the gain of the amplifier is finite and the bandwidth is infinite, the equivalent amplifier including the input node capacitance is a single pole amplifier. As a single pole amplifier can be regarded as a leaky integrator, the overall system satisfies

$$\frac{V_{in} - V_o}{R_f} = i_T, \tag{10}$$

$$-\int_{leaky} V_{in} dt = V_o. \tag{11}$$

By substituting V_{ideal}=$-i_T R_f$ and from (10) and (11), we have

$$V_o = \int_{leaky} (V_{ideal} - V_o) dt, \tag{12}$$

where V_{ideal} is the objective function that the output voltage V_o should follow. The system corresponding to (12) is shown in Fig. 1(b). As shown in introduction, we can regard V_{in} and V_o as two nodes in discrete space. Thus, we can rewrite (12) as following, assuming the leaky integrator has a gain A and a 3-dB pole p.

$$\lim_{\Delta t \to 0} \frac{\Delta_t V(x + \Delta x, t)}{\Delta t} + pV(x + \Delta x, t) + a\frac{\Delta_x V(x,t)}{\Delta x} = 0, \tag{13}$$

where $V(x,t) = V_{ideal}(t)$, $V(x + \Delta x, t) = V_o(t)$, $\frac{a}{\Delta x}$ is a unity gain bandwidth Ap, and $\Delta_x V(x,t)$ and $\Delta_t V(x,t)$ are forward differences shown below:

$$\Delta_x V(x,t) = V(x + \Delta x, t) - V(x,t), \tag{14}$$

$$\Delta_t V(x,t) = V(x, t + \Delta t) - V(x,t). \tag{15}$$

Equation (13) is an *active transmission line* equation with a zero order dispersion term when $\Delta x \to 0$ (shown in (3)) and it represents a conventional TIA.

We propose a new TIA circuit called a box TIA, which is described as following

$$\lim_{\Delta t \to 0} \Big(\frac{\delta_t (V(x, t + \frac{\Delta t}{2}) + V(x + \Delta x, t + \frac{\Delta t}{2}))}{2\Delta t} + p\frac{V(x,t) + V(x + \Delta x, t)}{2} + a\frac{\delta_x (V(x + \frac{\Delta x}{2}, t) + V(x + \frac{\Delta x}{2}, t + \Delta t))}{2\Delta x} \Big) = 0, \tag{16}$$

where $\delta_t V(x,t)$ and $\delta_x V(x,t)$ are central differences defined as:

$$\delta_x V(x,t) = V(x + \frac{1}{2}\Delta x, t) - V(x - \frac{1}{2}\Delta x, t), \tag{17}$$

$$\delta_t V(x,t) = V(x, t + \frac{1}{2}\Delta t) - V(x; t - \frac{1}{2}\Delta t). \tag{18}$$

Equation (16) can be simplified by noting $V(x,t) = V_{ideal}$, and $V(x + \Delta x, t) = V_o(t)$

$$\frac{d(V_o + V_{ideal})}{2dt} + p\frac{V_o + V_{ideal}}{2} + a\frac{(V_o - V_{ideal})}{\Delta x} = 0. \tag{19}$$

The box TIA maintains symmetry of averaged differences. The truncation error T_{box} due to the discretized spatial domain can be found by using Taylor expansion at $V(x + \frac{\Delta x}{2}, t)$ and which is

$$T_{box} = a\Big(\frac{(\Delta x)^2}{24} V_{xxx} + \frac{(\Delta x)^4}{1920} V_{xxxxx} \cdots\Big), \tag{20}$$

where V_{xxx} and V_{xxxxx} are the third and fifth order spatial derivatives of V, respectively. The box TIA has a third order accuracy regarding spatial discretization, whereas a conventional single stage TIA has a second order accuracy.

Similarly, the gain factor G_{box} for the box TIA is

$$G_{box} = \frac{(A-1)p - jw}{(A+1)p + jw}. \tag{21}$$

Substituting (10) in (19) and we get

$$\begin{aligned} V_o &= -2\int_{leaky} (V_o + i_T R_f) dt + i_T R_f \\ &= -\int_{leaky} (V_o + i_T R_f) dt + \tfrac{V_{in}}{2}, \end{aligned} \tag{22}$$

where the integrator is a single-pole amplifier. Figure 2(a) shows the block diagram of the box TIA.

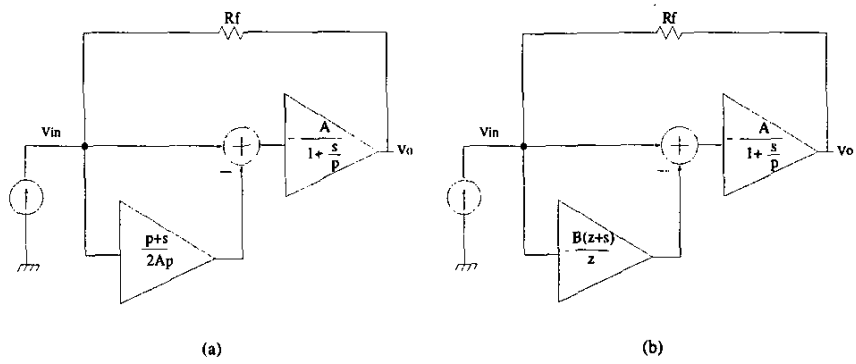

Fig. 2. The proposed box TIA: (a) direct implementation, and (b) a modified structure with left half plane zero.

However, this scheme generates a closed loop right half plane zero and thus the system has nonminimum phase. The location of open loop zero and the gain of compensation amplifier is adjusted to create a closed loop left half plane zero and to compensate for the dominant pole. In this design, the dominant pole is compensated by using multiple signal path instead of using cascaded stages [1]. Therefore, the compensation amplifier can be included in the closed loop resulting in improved linearity.

Figure 2(b) shows the modified block diagram of the box TIA with a left half plane zero z_{lp}. The transfer function of modified box TIA is

$$-(1+\frac{B(z_{lp}+s)}{z_{lp}})\frac{A}{1+\frac{s}{p}}V_{in}=V_o.$$
$$\frac{V_{in}-V_o}{R_f}=i_T. \tag{23}$$

The gain of compensation amplifier and the location of open loop zero should satisfy

$$\frac{z_{lp}(B+1)}{B}=p. \tag{24}$$

III. Circuit Implementation

Figure 3 shows the actual TIA design using a CMOS process. A wide bandwidth left half plane zero is implemented using a simple common source amplifier with an active inductor [3]. The location of the zero z_{lp} is

$$z_{lp}=C_{gs,1}R \tag{25}$$

and that of the dominant pole p_{real} is

$$p_{real}=\frac{AB+A+1}{R_f(C+C_{Ma}+C_{Mb})}, \tag{26}$$

where A is the gain of the main amplifier and B is the gain of compensation amplifier, $C_{gs,1}$ is the gate-source capacitance of M_1, and C_{M_a} and C_{M_b} are the total input capacitance of M_a and M_b, respectively. In reality, the main feedback loop creates two real poles and the compensation amplifier generates one real left half plane zero and two high frequency left half plane complex poles. The zero introduced by the compensation amplifier cancels the dominant pole created by the main amplifier. Figure 4 demonstrates pole, zero locations of the compensated TIA.

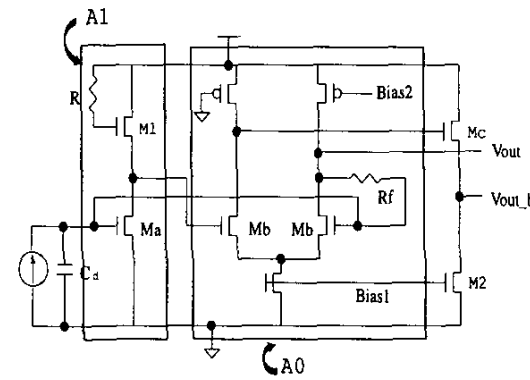

Fig. 3. TIA implementation using CMOS process.

As the compensation is made using multiple signal path, the stability of the overall TIA is determined by the main feedback amplifier, which is stable due to single stage design, and the frequency response is determined by the poles induced by the wide band compensation amplifier. Compared to two stage designs [2], the proposed scheme has relaxed stability issues and can operate with a lower supply voltage. Also, by achieving a large transconductance in M_a and M_b, the substrate coupling noise can be reduced [1]. By using this compensation scheme, the product of transimpedance and bandwidth of TIA is increased by more than 50 % compared to that of a single stage TIA.

A. Noise Analysis

The equivalent input noise current of the proposed TIA in Fig. 3 is:

$$i_{eq}^2 \approx i_f^2+\omega^2(C_{gs,Ma}+C_{gs,Mb}+C_d)^2 \times \frac{(i_{d,Ma}^2+i_{d,M1}^2)\frac{g_{m,Mb}^2}{g_{m,M1}^2}+2i_{d,Mb}^2}{(1-B)^2 g_{m,Mb}^2}, \tag{27}$$

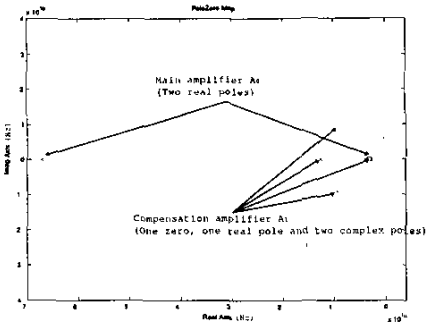

Fig. 4. Pole, zero location of TIA.

where C_d is the capacitance of the photo-detector, $-B$ is the DC gain of compensation amplifier, i_f is the feedback resistor noise current, $i_{d,Mb}$, $i_{d,Ma}$ and $i_{d,M1}$ are the noise currents of transistors Mb, Ma and $M1$, respectively, $C_{gs,Ma}$ and $C_{gs,Mb}$ are the gate-source capacitances of transistors Ma and Mb, respectively, and $g_{m,Ma}$ and $g_{m,Mb}$ are the transconductances of transistors Ma and Mb, respectively. By noting that $B \approx -\frac{g_{m,Ma}}{g_{m,M1}}$, the equivalent noise conductance is

$$\frac{S(i_{eq})}{4kT} \approx G_f + \frac{2}{3}w^2(C_d + C_{gs,Ma} + C_{gs,Mb})^2 \times [\frac{-B}{(1-B)g_{m,Ma}} + \frac{2}{(1-B)^2 g_{m,Mb}}], \tag{28}$$

where $S(i_{eq}) = \frac{i_{eq}^2}{\Delta f}$ and $G_f = \frac{i_f^2}{4kT\Delta f}$. Using the fact that

$$g_m = \mu_n C_{ox}\frac{W}{L}\Delta \tag{29}$$

$$C_{gs} = \frac{2}{3}C_{ox}WL, \tag{30}$$

where $\Delta = V_{gs} - V_t$ and substituting $C_{gs,Mab} = \alpha C_{gs,Ma}$, (28) becomes

$$\frac{S(i_{eq})}{4kT} \approx G_f + \frac{4L^2\omega^2}{9(1-B)\mu_n\Delta}(\frac{-B}{C_{gs,Ma}} + \frac{2}{\alpha(1-B)C_{gs,Ma}}) \times [(\alpha+1)C_{gs,Ma} + C_d]^2. \tag{31}$$

By taking the partial derivative of (31) with respect to $C_{gs,Ma}$, we can show that the noise conductance is minimum when

$$C_{gs,Ma} = \frac{C_d}{\alpha+1} \tag{32}$$

$$C_{gs,Mb} = \alpha\frac{C_d}{\alpha+1}. \tag{33}$$

The minimum equivalent noise conductance is therefore given by

$$\min(\frac{S(i_{eq})}{4kT}) = G_f + \frac{16C_dL^2\omega^2(\alpha+1)}{9(1-B)\mu_n\Delta}[-B + \frac{2}{\alpha(1-B)}] \tag{34}$$

and the noise is minimum with $\alpha = \sqrt{\frac{2}{-B(1-B)}}$. As $B \approx -1$, we set α to be close to unity in our design. The simulated input referred noise current for the proposed TIA is approximately $0.7\,\mu A_{rms}$, which is well within the specifications.

IV. Simulation Result

Figure 5 shows that the TIA bandwidth with a $1pF$ input capacitor is $1.32GHz$ with the transimpedance gain of $58dB$ at room temperature. The transimpedance bandwidth product is increased more than 67.5 % compared to a single stage TIA.

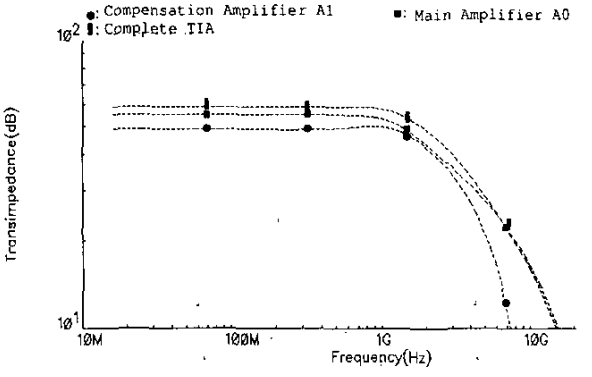

Fig. 5. Simulated transimpedance of the complete front-end with $1pF$ input capacitor.

The simulated performance of the proposed TIA is summarized in Table I.

TABLE I
Simulation Summary

Process	0.25 μm, 1 poly 5 metal CMOS
Transimpedance gain	58 dB
Bandwidth	1.32 GHz(1 pF input capacitance)
Power dissipation	50 mW
Power supply	2.5 V
Input noise current	0.7 μA
maximum input current	0.58 mA
Full scale output	0.5 V peak-to-peak

V. Conclusion

We analyzed the TIA as an *active transmission line*. The reduction of truncation error caused by the discretization of the spatial domain was design goal. As a result, TIA with multiple signal path has been created. The right half plane zero generated as a result was converted to left half plane zero to prevent having a nonminimum phase. Accordingly, the compensated TIA achieves 58 dB gain and 1.32 GHz bandwidth with 1 pF input node capacitance using 0.25 μm standard CMOS process.

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