An MLSE Receiver for Electronic Dispersion Compensation of OC-192 Fiber Links

Hyeon-Min Bae, Jonathan B. Ashbrook, Jinki Park, Naresh R. Shanbhag, *Fellow, IEEE*, Andrew C. Singer, *Senior Member, IEEE*, and Sanjiv Chopra

***Abstract*—A maximum-likelihood sequence estimation (MLSE) receiver is fabricated to combat dispersion/intersymbol interference (chromatic and polarization mode), noise (optical and electrical), and nonlinearities (e.g., fiber, receiver photodiode, or laser) in OC-192 metro and long-haul links. The MLSE receiver includes a variable gain amplifier with 40-dB gain range and 7.5-GHz 3-dB bandwidth, a 12.5-Gb/s 4-bit analog-to-digital converter, a dispersion-tolerant phase-locked loop, a 1:8 demultiplexer, and a digital equalizer implementing the MLSE algorithm. The MLSE receiver achieves more than 50% reach extension at signal-to-noise levels of interest as compared to conventional clock data recovery systems.**

***Index Terms*—A/D converter (ADC), clock data recovery (CDR), demultiplexer (DEMUX), electronic dispersion compensation (EDC), electronic post-detection equalization (EDE), G.709 optical transport network (OTN), high-speed ASIC, maximum-likelihood sequence estimation (MLSE), OC-192, phase-locked loop (PLL), variable gain amplifier (VGA).**

I. Introduction

ELECTRONIC dispersion compensation (EDC) receivers have increasingly been investigated as a cost-effective way to (partly) mitigate the OC-192/STM-64 link transmission impairments arising from group-velocity dispersion [also referred to as chromatic dispersion (CD)], polarization-mode dispersion (PMD), and other pattern-dependent impairments in a wide range of optical links [1]. Maximum-likelihood sequence estimating (MLSE) receivers are known to provide optimum performance under dispersion [2], [3] and have recently promised to allow optimal EDC reach extension in wavelength-division multiplexing (WDM), low-optical-signal-to-noise-ratio (OSNR) applications with either Mach–Zehnder intensity modulator (MZM) nonreturn-to-zero (NRZ) or optical duo binary (ODB) modulation [4].

An MLSE receiver that operates in the digital domain provides robust performance under severe channel impairments (e.g., nonlinearities or noise) unlike analog EDC solutions such as feed-forward equalizers (FFEs) and decision feedback equalizers (DFEs) [5]. Consequently, an MLSE receiver blends well with more demanding enhanced forward error correction (EFEC) as well as with externally modulated laser (EML) transmitters; the latter is enabling the increasingly important pluggable WDM optical interfaces. Such performance robustness becomes the most valuable attribute of next generation WDM systems that enable new multiservice metropolitan architectures.

MLSE-based solutions can also offer additional features such as link diagnosis and failure identification and detection that are not available in analog-based EDC implementations. Alarms, thresholds for dispersion and nonlinearity, real-time link monitoring, and tamper control can also be obtained. Additional value of such an MLSE implementation can also be garnered by enabling the use of soft-input forward error correction (FEC) decoding algorithms.

This paper presents an MLSE receiver for OC-192/STM-64 long-haul (LH), ultralong-haul (ULH), and metro fiber networks. The MLSE receiver comprises an analog front-end (AFE) IC implemented in a 0.18-μm, 3.3-V, 75-GHz, SiGe BiCMOS process and a digital equalizer (DE) IC fabricated in a 0.13-μm, 1.2-V CMOS process. The AFE and DE are packaged in a 23 mm $\times$ 17 mm, 261-pin multichip module (MCM). The MLSE receiver is compatible with the multisource agreement (MSA) for 300-pin 10-Gb/s transponders [6].

II. MLSE Receiver Architecture

The architecture of the MLSE receiver is shown in Fig. 1. It features a variable gain amplifier (VGA), a 4-bit flash analog-to-digital converter (ADC), a dispersion-tolerant clock recovery unit (CRU), and a 1:8 demux (DEMUX). The ac-coupled line rate input (9.953–12.5 Gb/s) can be single-ended or differential. The input signal is amplified by the VGA then sampled by the ADC. The CRU recovers a line rate clock for the ADC and the DEMUX. The 4-bit line rate ADC samples are demuxed 1:8 to generate a 32-bit LVDS interface to the digital equalizer IC (see Fig. 1). The digital equalizer IC implements the four-state MLSE algorithm which assumes a channel memory of three symbols. The digital equalizer includes a blind, adaptive channel estimator and a data decoding unit on-chip that require no training. The integrated channel estimator and data decoding block help to eliminate potential bit error rate (BER) floors or error propagation that could develop from poor front-end or channel estimation/tracking performance.

III. VGA

A VGA for EDC-based optical front-ends should satisfy linearity as well as sensitivity specifications because it can be incorporated either in OSNR limited or receive power-limited applications. Amplified links which usually operate with a limited OSNR, require only linearity of the VGA; however, unamplified point-to-point metro links require both linearity and high sensitivity because high dispersion is accompanied by severe attenuation. Conventional limiting amplifiers are not suitable for

Manuscript received February 25, 2006; revised May 3, 2006.

H.-M. Bae, J. B. Ashbrook, J. Park, and S. Chopra are with Intersymbol Communication Inc., Champaign, IL, 61820 USA (e-mail: bae1@intersymbol.com).

N. R. Shanbhag and A. C. Singer are with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Champaign, IL 61820 USA.

Digital Object Identifier 10.1109/JSSC.2006.883317

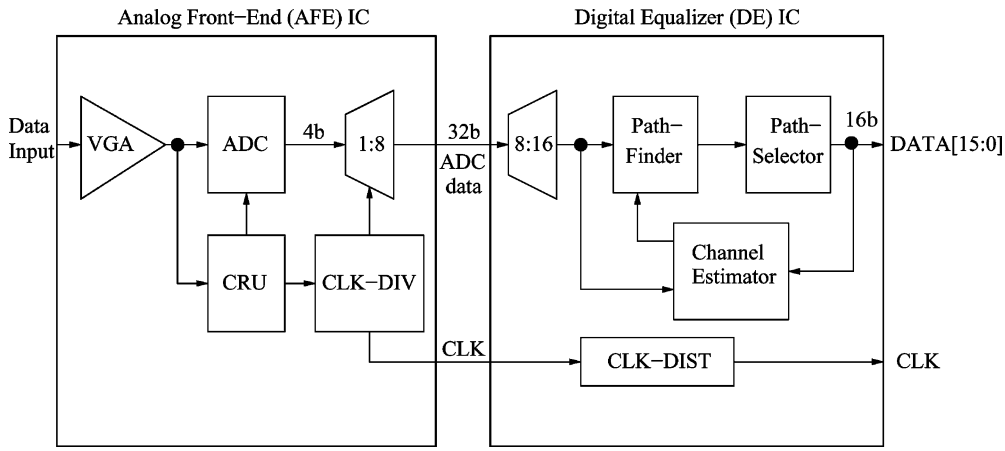


Fig. 1. Block diagram of MLSE-based receiver.

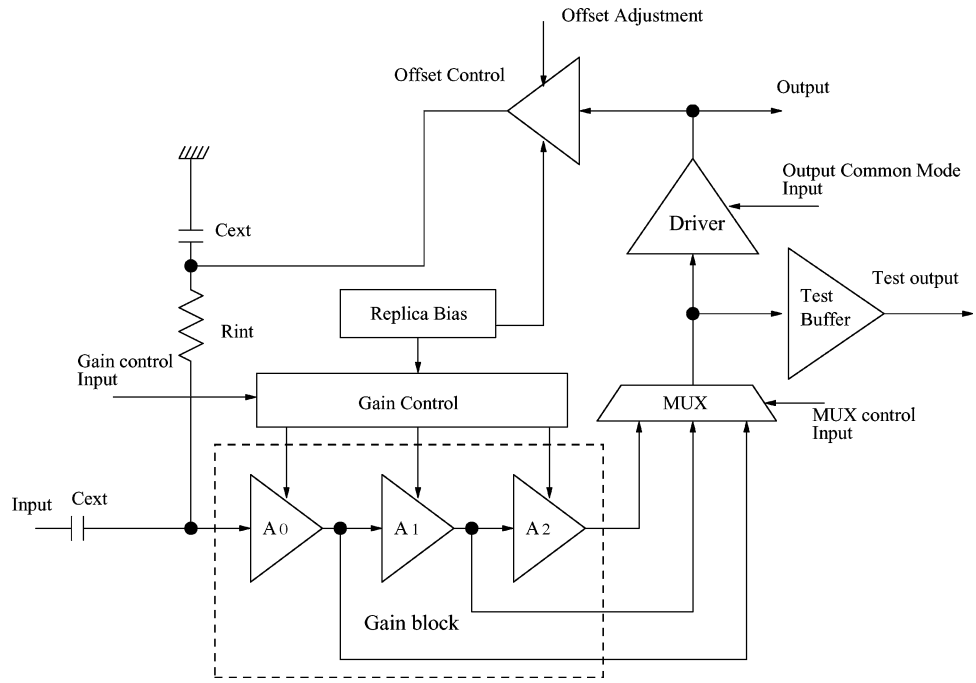


Fig. 2. Block diagram of the proposed SiGe VGA.

such applications due to nonlinearities [7]. The output offset of the VGA should be insensitive to overall gain within the VGA to minimize the BER impact with respect to input power transients.

In order to cover previously mentioned applications, a variable gain range of >40 dB, a spurious free dynamic range (SFDR) of >18 dB, an input sensitivity of <10 mV, and a 3-dB bandwidth of >6 GHz are required.

A. VGA Architecture

The proposed VGA (see Fig. 2) consists of a gain block, an analog multiplexer (MUX), a gain control block, an offset control block, a replica bias generator, and output drivers.

The gain block consists of three identical cascaded differential amplifier stages. Each stage provides a gain range of -1–11 dB. The output of each stage is connected to an analog MUX. The gain of the VGA is controlled by a current injected into the gain control block and the analog MUX control input. The replica bias generator generates a replica of the dc bias points of the gain block and provides them to the gain control block and offset control block in order to achieve process insensitivity. The analog MUX feeds into an output driver that includes a common-mode feedback (CMFB) loop to track the common-mode voltage information provided by the ADC. The outputs of the driver provide offset information to the offset control block which then adjusts the output dc offset voltage by using a low frequency feedback loop. This scheme enables gain-insensitive output offset control without impacting front-end bandwidth or power consumption. Another important functionality of the offset control block is to provide proper input bias voltage to the first gain stage such that the gain of the overall VGA is insensitive to process variations.

B. Gain Block and Process-Insensitive Gain Control

The gain block consists of three identical differential amplifiers each having tunable emitter degeneration. The emitter degeneration resistor is made tunable by employing an nMOS

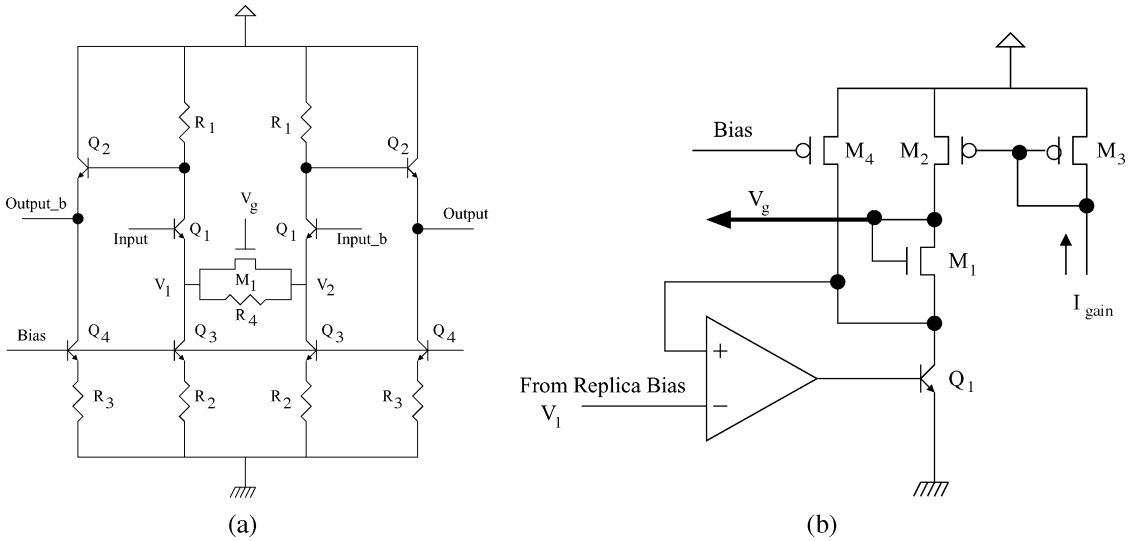


Fig. 3. Circuit diagram of (a) gain stage and (b) process-insensitive gain control.

transistor in parallel with a fixed resistor as shown in Fig. 3(a). The gain is controlled by tuning the gate voltage of the nMOS transistor M_1 biased in the linear region. The fixed resistor R_4 sets the minimum gain.

One benefit of the proposed architecture is that sufficient linearity is achieved without impacting receiver sensitivity. The VGA achieves high sensitivity for small input signals via small degeneration resistance. The linearity of the gain stage is consistent with the input amplitude. When the input signal is large, the VGA gain is reduced and linearity is increased by increasing the degeneration resistance. Another advantage of the proposed gain stage design over conventional VGA designs [8] is low supply voltage operation due to a smaller transistor stack. This lower supply results in lower power consumption.

The performance of the gain block is highly dependent on the MOS process variables such as the threshold voltage $V_{\rm th}$ and the device transconductance K of M_1 [see Fig. 3(a)]. By noting that the gain of each gain stage A_v is given by

$$A_v \approx (1 + KR_4(V_{\rm gs} - V_{\rm th}))\,\frac{2R_1}{R_4} \tag{1}$$

where $V_{\rm gs}$ is the gate-to-source voltage of M_1, it is necessary to control the gate-to-source voltage $V_{\rm gs}$ carefully in order to achieve process independence. The process-insensitive gain controller schematic is shown in Fig. 3(b). The replica bias cell (not shown here) generates the dc bias point V_1 [see Fig. 3(a)] for the gain control block. By incorporating a diode-connected nMOS M_1 which is identical to the nMOS M_1 used in the gain stages [see Fig. 3(a)], the gain control voltage V_g is given by

$$V_g = V_1 + V_{\rm th} + \sqrt{\frac{2I_{\rm gain}}{K}} \tag{2}$$

where $I_{\rm gain}$ is the external current input which controls the gain. Substituting (2) into (1), we obtain

$$A_v \approx (1 + R_4\sqrt{2KI_{\rm gain}})\,\frac{2R_1}{R_4}. \tag{3}$$

From (3), it is clear that the gain is independent of the threshold voltage and that sensitivity to device transconductance K is also decreased.

The total simulated gain variations are 1.3 and 2.5 dB at low and high gain modes, respectively, with the minimum-size nMOS transistor in M_1.

Transistor M_4 injects idling current into Q_1 to maintain phase margin in the low-gain case by keeping the pole at the collector of Q_1 at a sufficiently high frequency.

C. Analog Multiplexer

The analog MUX is incorporated to satisfy both the linearity and sensitivity requirements. The analog MUX consists of cascaded parallel amplifiers whose final outputs are summed using an open collector scheme. The first and second stages of the MUX are intended for amplified fiber links, where the received power is high due to erbium-doped fiber amplifiers (EDFAs) and the third stage of the MUX is intended for unamplified metro links where the receiver sensitivity dominates the performance. Given that the linearity of the analog MUX is better than that of the gain stages because the former employs larger passive fixed-degeneration resistors for unity gain, the overall VGA linearity is improved over a static three-cascaded-stage architecture. Simulation results reveal that the proposed analog MUX design improves the VGA linearity by 10 dB compared with the conventional cascaded structure.

One drawback of the analog MUX could be its bandwidth limitation. However, this limitation is not found to be significant when proper layout guidelines and emitter peaking are employed.

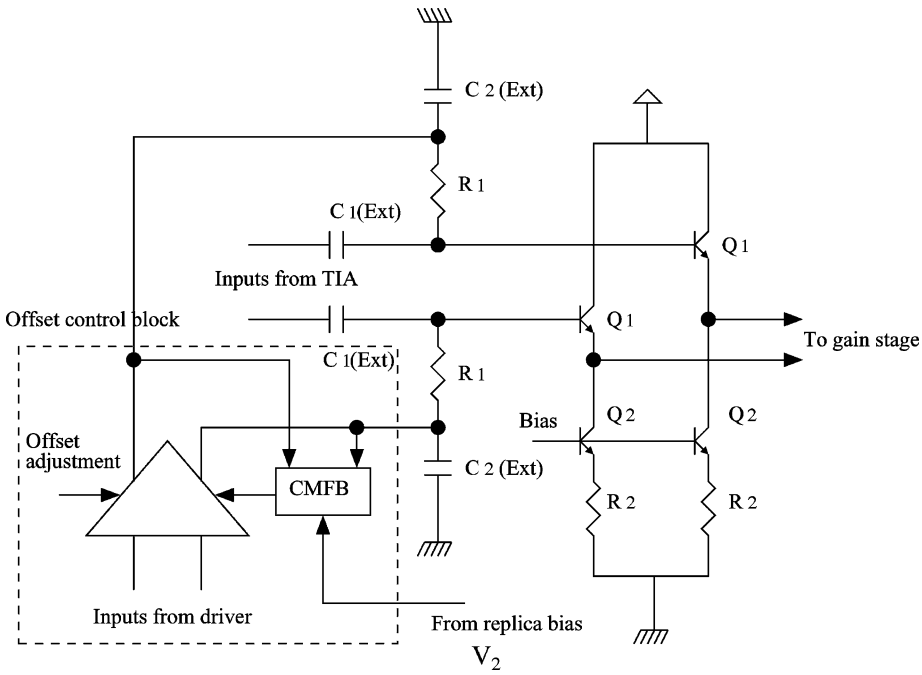


Fig. 4. Simplified circuit schematic including offset cancellation scheme and input termination.

D. Input Termination and Offset Control

The main focus of input termination and offset control design is to enable single supply and single-ended operation while maintaining process-insensitive VGA gain.

The emitter follower stage shown in Fig. 4 isolates the input termination from the gain stage, thereby providing a constant input impedance over the entire gain range. The correct input common mode voltage [$V_{\rm in} = V_{\rm cc} - I_{\rm bias}R_1 - V_{{\rm be},Q_2}$ in Fig. 3(a)] is generated by the replica bias and used as a common-mode voltage reference. As a result, the first stage also benefits from the process-insensitive gain control scheme described earlier.

The offset control circuitry suppresses unwanted VGA output offsets caused by various imbalances and allows for injection of a controlled offset, improving performance in amplified optical fiber links where the noise is not uniformly distributed. Offset control circuitry must have a wide linear input voltage range for proper operation. The output offset of the VGA is insensitive to the gain of the VGA, enabling error-free operation in the presence of input power transients without manually adjusting the output offset. The 3-dB cutoff bandwidth is chosen carefully such that the offset control tracks input power transients. The offset control circuitry is carefully simulated with the package model in order to ensure the stability of the entire VGA.

IV. ADC

The ADC architecture shown in Fig. 5 has a stage of preamplifiers followed by two stages of metastability flip-flops (ADC FFs) and a Gray encoder. The ADC architecture [9] is chosen considering the bandwidth requirement and voltage headroom. One soft-decision ADC FF (low effective gain and bandwidth) is followed by a hard-decision ADC FF (high effective gain and bandwidth), lowering the metastability-related BER floor while minimizing data feedback to the sensitive reference ladder [10]. The Gray encoder limits coding errors to one least significant bit (LSB), minimizing their impact on the BER. The PLL clock is distributed using microstrip transmission lines with far-end termination and buffered locally to reduce aperture uncertainty at the ADC FFs. The input swing is digitally controlled to achieve optimum balance between thermal noise and voltage dependent group delay variations across the preamplifiers. The center of the dummy ladder (not shown), which is a replica of the reference ladder, provides the correct ADC input common-mode voltage to the VGA. The ADC can be configured between a 4-bit mode and a power-saving 3-bit mode by disabling alternating preamplifiers and ADC FFs.

The cascode preamplifier (see Fig. 6) reduces summing node resistance and VGA output loading. The estimated input offset is 2.86 mV at room temperature, assuming 6% transistor mismatch (process data when they are 15 μm apart) and 5% resistance mismatch due to layout variability. Considering one LSB size, the estimated offset voltage is sufficiently low so that additional offset averaging circuitry [11] is not required. The current biasing circuitry for the preamplifiers and reference ladder are carefully designed and protected by guard rings to minimize substrate mixing.

The ADC FFs incorporate CML-based latches for high-speed operation [9]. Bandgap-voltage-referenced current biasing guarantees a constant logic swing level regardless of temperature and supply voltage variations.

The ADC clock and data paths are matched to provide consistent sampling points across all 16 comparators. Clocks for the Gray encoder are carefully delayed and distributed to compensate for the logic gate delays.

Isolation between the preamplifiers, the ADC back-end (ADC FFs and the encoder), and the DEMUX is critical. Guard rings are placed between the preamplifiers and the ADC back-end,

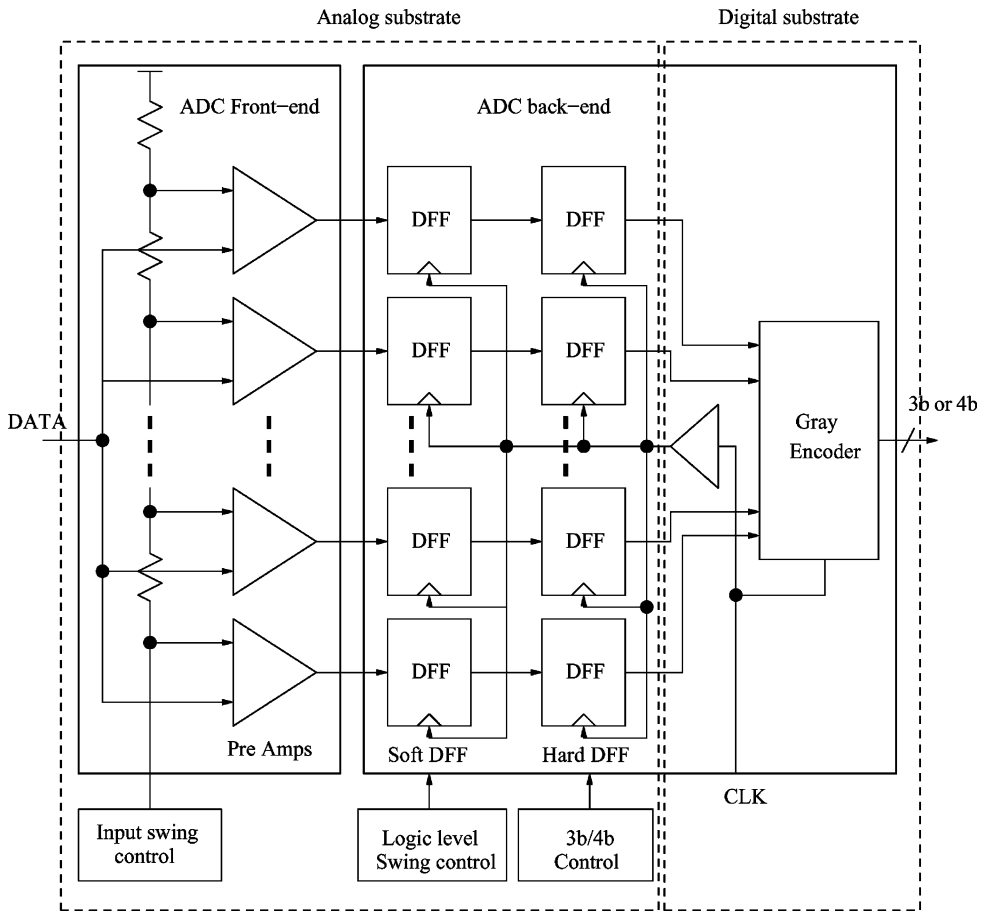


Fig. 5. Block diagram of 3-bit/4-bit configurable ADC.

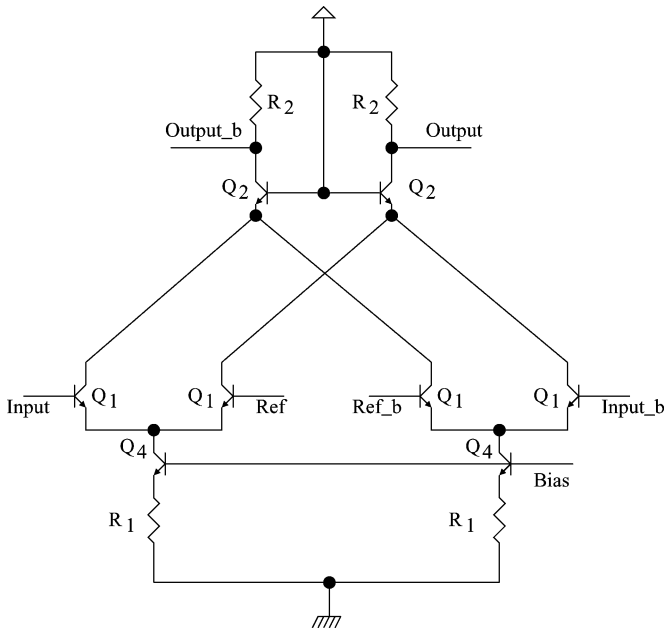


Fig. 6. Schematic of the ADC preamplifier.

and between the ADC back-end and the DEMUX. The ground and substrate connections of the preamplifiers and the ADC FFs are shared to minimize ground bounce. The swing in the digital blocks (i.e., ADC back-end and DEMUX) is made programmable to strike a balance between substrate injection and noise immunity. The optimum swing level of digital blocks is determined based on overall BER performance of the entire system.

V. Clock Recovery Unit

The CRU shown in Fig. 7 is a bang–bang PLL [12] with a phase frequency detector (PFD), a fast differentially tuned voltage-controlled oscillator (VCO), a phase interpolator for sampling time adjustment, and phase filtering which enables clock extraction in the presence of a closed eye. The frequency detector carries the VCO frequency up to the narrow locking range of the phase detector. A multiplexer with smooth transition is incorporated to switch between frequency acquisition mode and phase acquisition mode. The selection is made based on the outputs of the loss of lock detector (LOL) and the loss of signal (LOS) detector. LOL declares a loss of lock if the frequency difference between the external reference clock and the VCO output clock is more than 200 ppm.

The phase interpolator adjusts the sampling time by ± 10 ps to compensate for unwanted phase offsets generated by either input signal distortion or process variations. The phase interpolator adjusts delay by utilizing a weighted average between the direct and delayed signals.

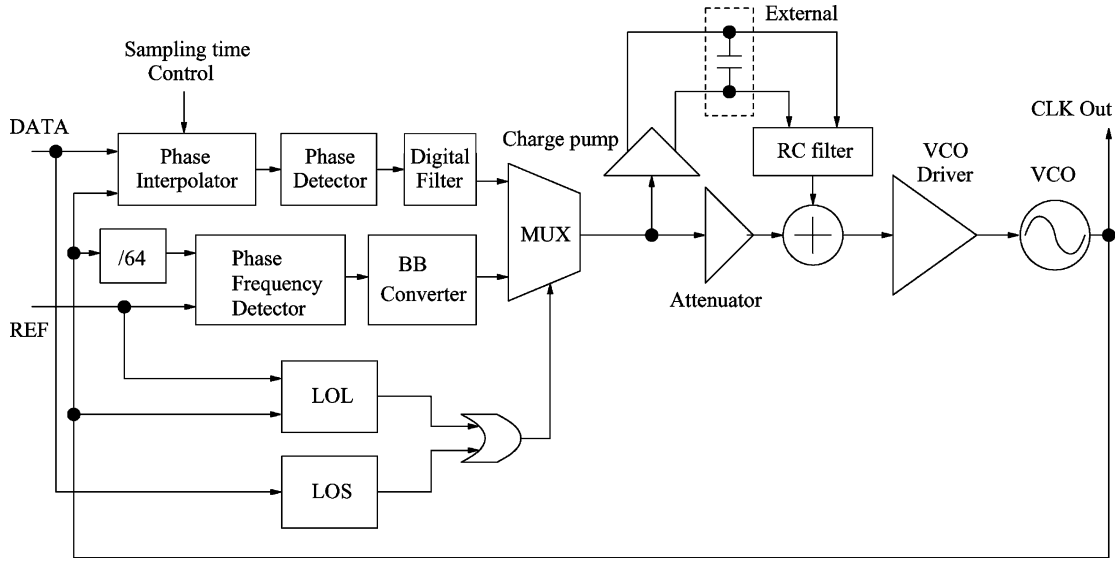


Fig. 7. Block diagram of jitter-tolerant PLL.

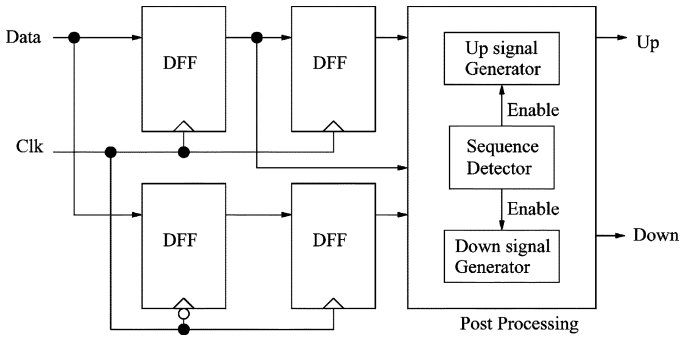


Fig. 8. Alexander phase detector with postprocessing.

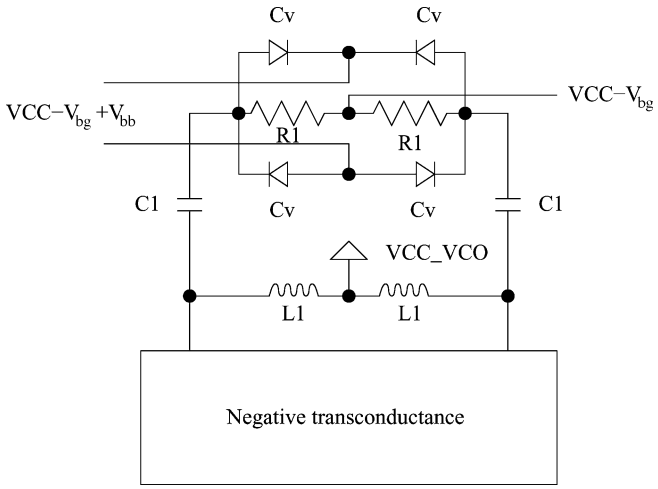


Fig. 9. Four-point bridge varactor design with process/supply voltage-independent frequency control.

The phase updates have low- and high-frequency components where the latter tracks instantaneous phase changes and only the former is sent off-chip to a loop capacitor using a four-point tuning-sensing bridge connection. The bridge connection removes inductive peaking caused by the bond wires. The sensing input has a third-order *RC* filter to reduce off-chip noise.

Blocks in the data and clock paths of the CRU, VGA, and ADC are matched to provide automatic center-of-eye sampling.

A. Phase Detector

Fiber nonlinearities, dispersion, and noise (amplified spontaneous emission (ASE) in amplified links and electrical noise in unamplified links) in LH/metro fiber links spread the zero crossings and severely distort the duty cycle of the transmitted signal. The PLL design incorporates advanced strategies to overcome these obstacles in the presence of high dispersion. Conventional PLLs generate significant jitter and cycle slips after 70–80 km of fiber at an OSNR < 12 dB.

An Alexander, or bang-bang, phase detector [13] is chosen over a Hogge phase detector [14] because the output frequency of the Alexander phase detector is half that of the Hogge phase detector. This makes the Alexander phase detector less sensitive to narrow pulses caused by dispersion and nonlinearities. Also, a bang-bang PLL generates less output jitter under low-input SNR conditions than a linear PLL [12]. A single-edge-sensitive phase detector using a divider at the input of the data path [15] is an effective scheme for dealing with duty cycle distortions. However, an isolated 10-Gb/s pattern with severe dispersion and nonlinearities causes false phase update signals with this scheme. Also, phase offset arising from Clock-to-Q delay is hard to match across process and temperature variations using linear circuit blocks. Therefore, a standard Alexander phase detector is chosen as a basic phase-detector architecture and modified to enhance the dispersion tolerance.

Fig. 8 shows the Alexander phase detector with postprocessing. The UP and DOWN signals generated by latched data are enabled by the sequence detector. Postprocessing achieves two main goals. First, it enables phase updates with only one type of data edge, overcoming duty cycle distortion. Second, it disables the phase updates when the pattern-dependent jitter caused by an isolated 10-Gb/s pattern is more than 0.25 UI

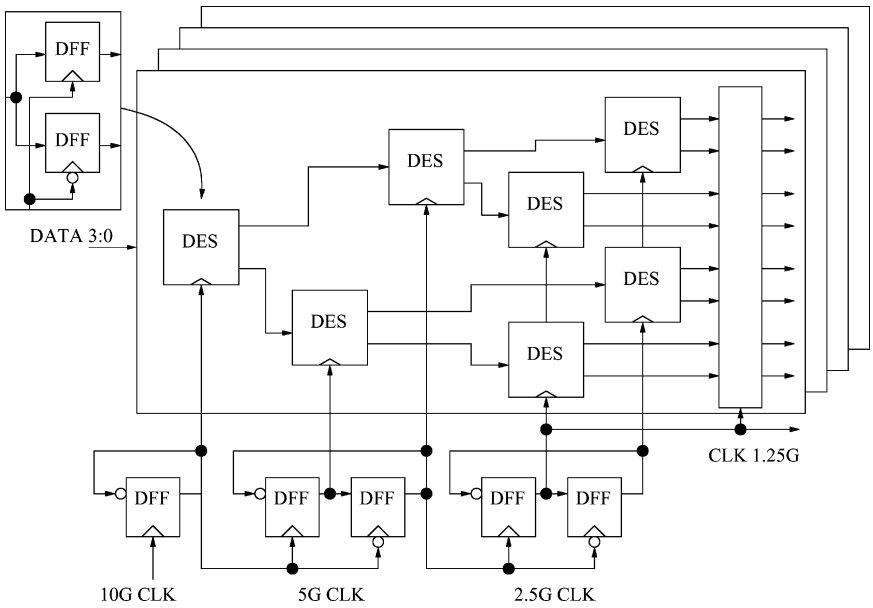


Fig. 10. Block diagram of 1:8 DEMUX.

under severe dispersion. This scheme does not cause any phase offset because the update decision is made after sampling.

B. VCO Design

An *LC* VCO is chosen over a ring-type VCO to suppress jitter generation. Metal–insulator–metal (MIM) capacitor C_1 in Fig. 9 is inserted to achieve insensitivity to supply voltage variations. Three VCOs, each with a 1-GHz tuning range, cover a 9.9–12.5-GHz frequency range with sufficient frequency overlap. The VCO in Fig. 9 employs a bridge varactor driven by an emitter follower to provide instantaneous frequency updates while increasing common-mode noise immunity. The VCO has a fully differential tuning input with more than a 2-GHz bandwidth to guarantee instantaneous frequency shifts in the VCO.

The VCO has a dedicated power supply and ground. The common-mode voltages of the differential tuning input and bias inputs are identical and set at the supply-referenced bandgap voltage $V_{\rm CC} - V_{\rm bg}$. The four-point bridge connection is more immune to PLL supply-induced jitter and injection locking than a fully differential two-point connection [16] due to the nonlinear varactor tuning characteristics. Consequently, all first-order charge injection mechanisms are eliminated in this design.

The varactors in the bridge are sized to minimize the net transient current flowing into C_1 in the locked condition for jitter reduction. The VCO is isolated from hard-switching blocks, such as the clock dividers in the PLL, the ADC FFs, and the DEMUX, to reduce noise coupling and avoid injection locking through the substrate.

VI. 1:8 DEMUX

The 4-bit ADC output is deserialized by a factor of eight using four parallel conventional tree-structured DEMUXs. The DEMUX is comprised of a clock divider block, along with four data trees (shown in Fig. 10). The clock divider accepts the 10-GHz recovered clock and creates 5-, 2.5-, and 1.25-GHz clocks that are used by the data trees. Additionally, copies of the 5- and 2.5-GHz clocks are created with a 90° phase shift. Each data tree takes one data bit at 10 Gb/s as input and provides eight data bits at 1.25 Gb/s at the output. The data tree has a latency of nine clock cycles.

The 10-GHz clock divider is a master–slave FF with the data input tied to the inverted output. The 5- and 2.5-GHz dividers are each comprised of a primary positive-edge-triggered master–slave FF followed by a secondary negative-edge-triggered master–slave FF. The output from the secondary FF is inverted and fed back to the data input of the primary. The secondary FF creates the phase-shifted copy of the primary divided clock. The clock outputs are carefully buffered so that, for each frequency, each buffer drives the same size load. The layout for the clock tree is also carefully balanced to provide the smallest possible clock skew. The buffer and layout balancing provide process-insensitive clock distribution.

Each data tree is built from concatenated dual-edge samplers. Each of these samplers contains two master–slave FFs, one positive-edge-triggered and the other negative-edge-triggered. Thus, each sampler demuxes the data by a factor of two. Each DEMUX stage uses either the primary or phase-shifted secondary clock, depending on the edge that launched the previous data. The positive-edge launched data are always sampled by the phase-shifted clock, and the negative-edge launched data are always sampled by the primary clock. This prevents interaction between clock and data that were launched from the same clock edge. This technique makes the DEMUX logically correct without using process-sensitive delay lines. The final stage of the data tree is clocked by a common clock to align all eight data bits to the same clock phase.

The CML-based flip-flops used in the DEMUX resemble those in the ADC backend and share the same bias scheme. Lower frequency stages are designed to use less bias current while maintaining the same swing. The primary design consideration for the FFs is ensuring that they have reasonably

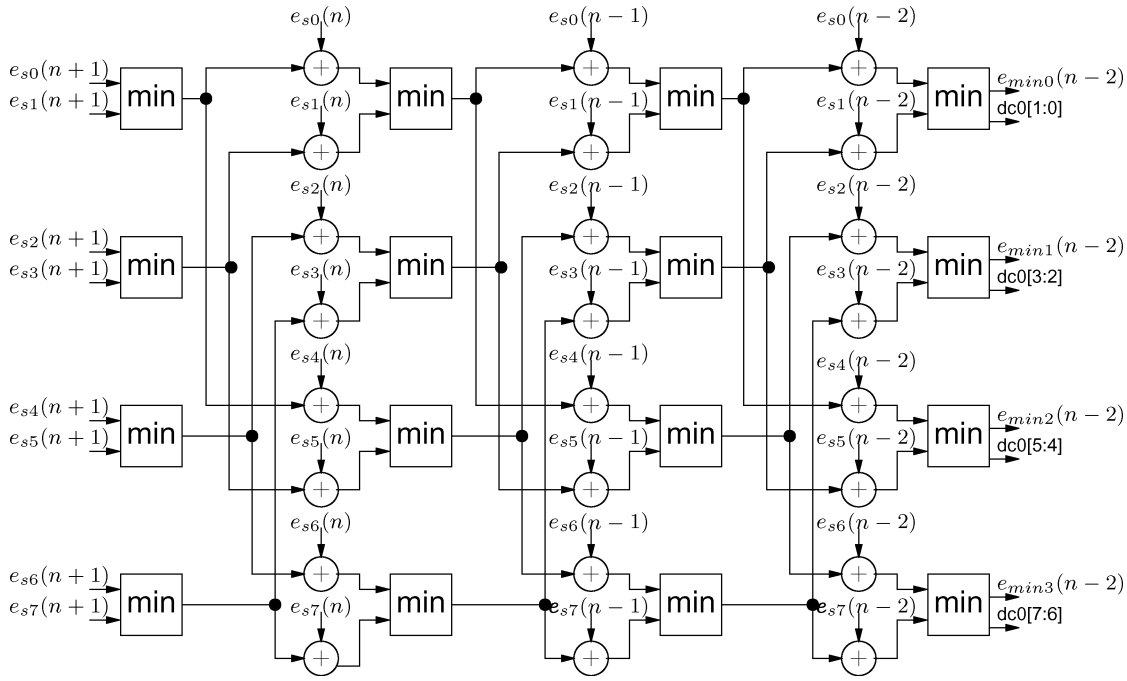


Fig. 11. CAS block.

smallsetup and hold times. The fastest path in the design is the feedback in the 10-GHz clock divider. At 12.5 GHz, this path has positive slack of 30 ps, leaving a comfortable 30% margin.

VII. MLSE Implementation

The digital IC accepts a line-rate/8, 32-bit LVDS input stream, along with a line-rate/16 clock from the AFE IC, as shown in Fig. 1. The received clock is used to dual-edge sample the data and create 4-bit, 16-parallel data which are fed into the MLSE engine. The MLSE engine is a novel parallel, time-reversed, sliding-window Viterbi decoder [17]. The decoder utilizes backward recursion to reduce the critical path to a cascade of eight multiplexers. The MLSE engine is supplied with channel estimates from a low-frequency adaptive channel estimator, which models the nonlinear channel impulse response over three bit periods. The digital IC provides a 16-bit line-rate/16 LVDS output stream compliant with the OFI-SFI4-01.0 [18] implementation agreement.

As mentioned above, the MLSE engine models the channel impulse response over three bit periods. Thus, the current received sample $r(n)$ is a function of the transmitted symbol $d(n)$, as well as the previous two transmitted symbols $d(n-1)$ and $d(n-2)$, hence the engine is a four -state Viterbi equalizer. The channel estimator provides channel estimates $\hat{r}_{000}(n)-\hat{r}_{111}(n)$ corresponding to all eight possible combinations of the current and previous two transmitted symbols.

In each symbol/bit period, a conventional Viterbi decoder employs the current received sample $r(n)$ to compute branch metrics and employs it to update the four path metrics that corresponds to the likelihood of the best path ending at each of the four states. This update is done using the add-compare-select (ACS) operation which is recursive and therefore hard to implement at a line rate of 12.5 Gb/s. High-speed Viterbi architectures employ parallel processing or higher radix processing [19]. In parallel processing, the input sequence is divided into subblocks and more than one subblock is processed at a time. However, disjoint processing of blocks leads to undesirable edge-effects where the symbols at block edges tend to have a higher BER. In higher radix architectures, more than one trellis section is processed in each clock cycle. It has been noted that speed-ups with higher radix processing lie between 1 and 2 and thus are not sufficient for this application [19].

The proposed MLSE algorithm employs parallelization by a factor of eight to achieve high throughput, a sliding window to minimize edge effects, and backward/time-reversed processing of the trellis combined with a fixed-delay look-back of 6 bit in order to eliminate the ACS recursion. The only recursion in the MLSE engine is a loop with two multiplexers.

For each received sample, the engine starts with all possible *final* states and their branch error metrics. The engine then begins with the most recent channel observations and works backwards through the trellis to determine the most likely path through the trellis for all 16 received samples.

The MLSE engine begins by computing the branch metrics $e_{sk}(n)$ by comparing each received sample against the eight possible channel estimates: $e_{sk}(n) = (r(n) - \hat{r}_{k\%8}(n))^2$. This results in 128 sample errors $e_{s0}(n) \ldots e_{s127}(n)$. These sample errors are then fed into the **path-finder** block. The **path-finder** operates on eight sets (being eight-parallel) of two received samples and their corresponding branch metrics. Path metrics are then computed by successive compare-add-select (CAS) operations, as shown in Fig. 11 for one bit pair. Note that this is the reverse of the ACS operations of a conventional Viterbi decoder and is nonrecursive. The **path-finder** outputs eight sets of four bit-pairs dc0[7:0]. . .dc7[7:0]. Each of the four bit-pairs in a set is a decision candidate corresponding to the value of the

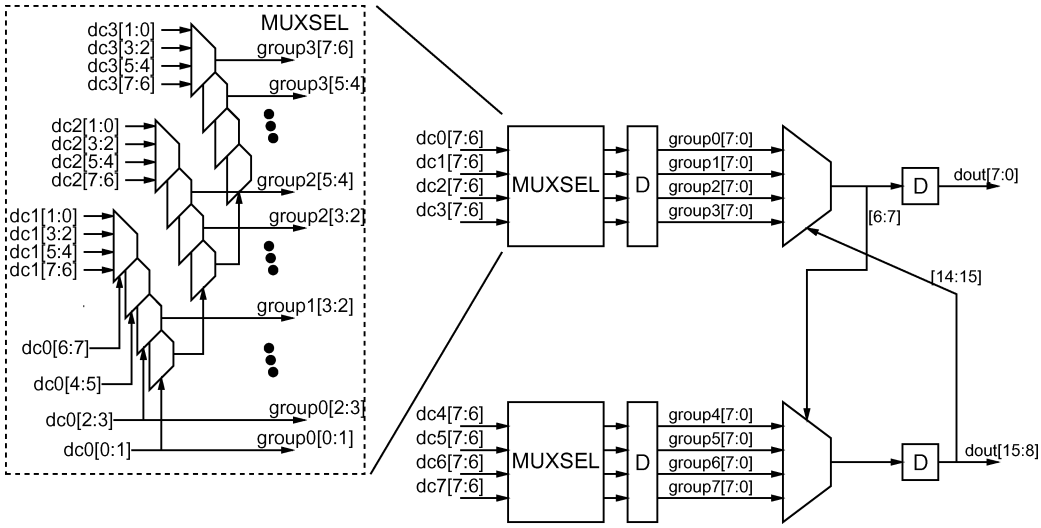
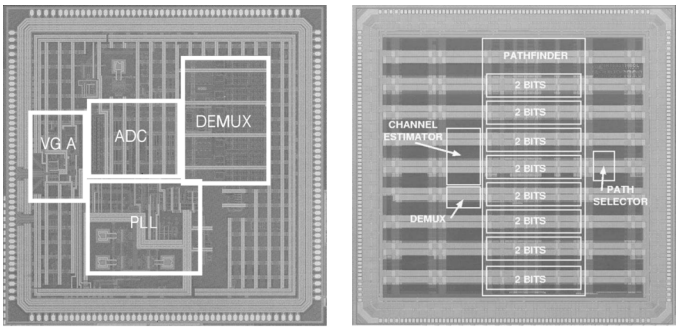


Fig. 12. Path selector block.



(a) (b)

Fig. 13. Microphotograph of (a) analog front-end and (b) digital equalizer.

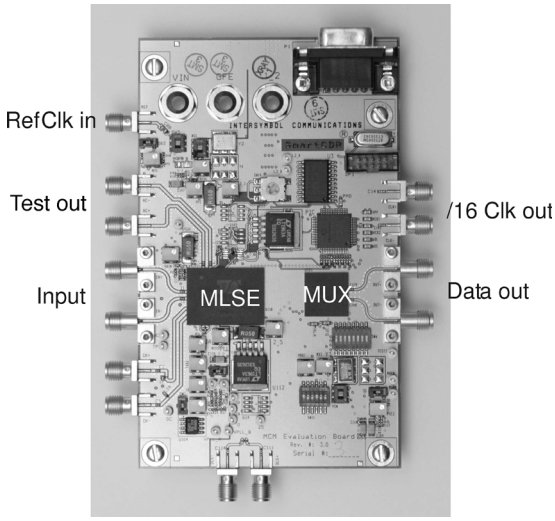


Fig. 14. Test board.

previous two decoded bits. The **path-selector** selects the correct bit-pair based on the value of the previous two bits. The **path-selector** therefore stores two past decisions and employs these in selecting the next 16 bit by progressively traversing eight multiplexers.

The time-reversed structure of the architecture results in an entirely feedforward **path-finder** architecture and a short critical path in the **path-selector**. This architecture can thus be arbitrarily pipelined and is highly regular consisting of only comparators, adders, and multiplexers. This implementation uses a 3-bit carry-select adder as the basic computational kernel for the comparators and adders. The uniform pipeline can perform an 8-bit addition and some miscellaneous logic in one clock cycle. This high utilization results in the IC having an overall latency of only 21 clock cycles.

As mentioned above, the critical path in the **path-selector** is the traversal of eight multiplexers. This path can be pipelined to reduce the critical path as shown in Fig. 12. This pipelining is accomplished by using a selection look-ahead structure. The `muxsel` structures create eight groups, `group0...group7`, of 8 bit each. `group0...group3` each contain a set of the eight least significant output bits corresponding to the previous two decoded bits. Likewise, `group4...group7` each contain a set of the eight most significant output bits corresponding to the last two bits selected from `group0...group3`. Thus, the critical path consists of making a selection from `group0...group3` and then a selection from `group4...group7`. Because of loading, the `muxsel` multiplexer chain is faster than the final two-multiplexer chain. This pipelining technique could be extended one more time such that the critical path was only one multiplexer by precomputing four full 16-bit sets of results.

VIII. Measured Results

The AFE IC is implemented in a 0.18-μm 3.3-V 75-GHz SiGe BiCMOS process. The digital equalizer IC is fabricated in a 0.13-μm, 1.2-V CMOS process. The AFE and DE are packaged in a 23 mm $\times$ 17 mm 261-pin MCM. The chip microphotographs are shown in Fig. 13(a) and (b).

The two chips were tested independently first and then together in various fiber plants with various transmitters. The ten-layer evaluation board (shown in Fig. 14) is fabricated to characterize the MLSE MCM. The evaluation board includes

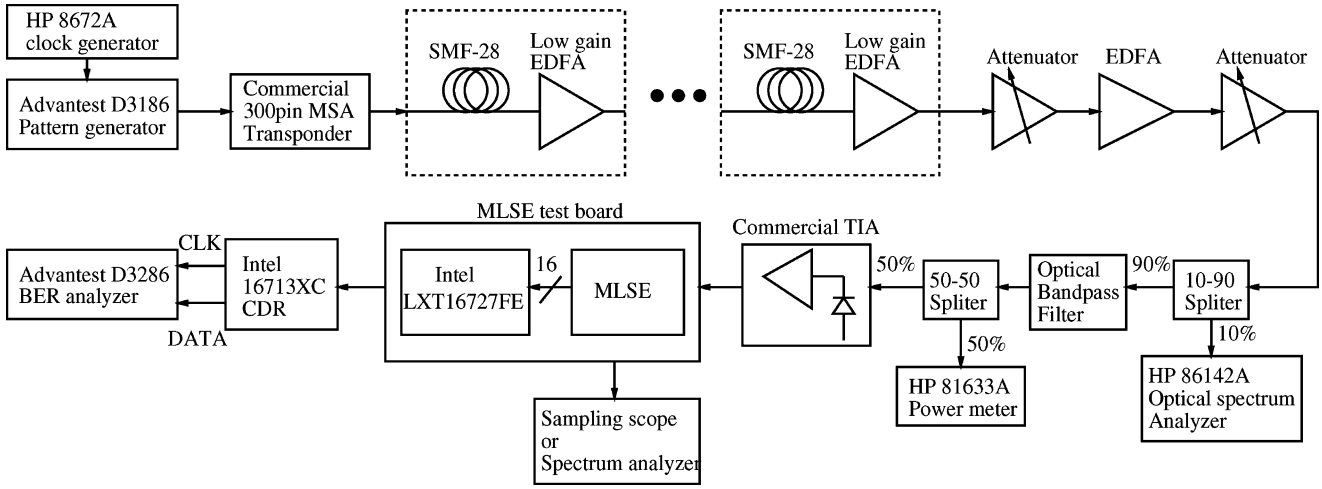


Fig. 15. Nominal measurement setup for MLSE receiver.

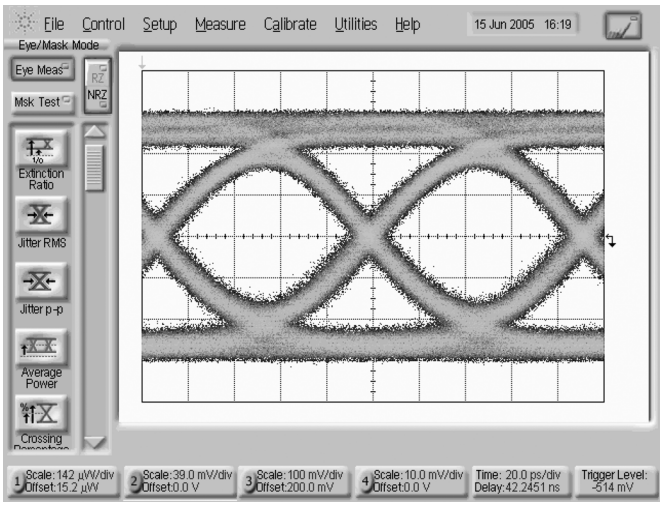


Fig. 16. Captured eye diagram of VGA at test buffer output.

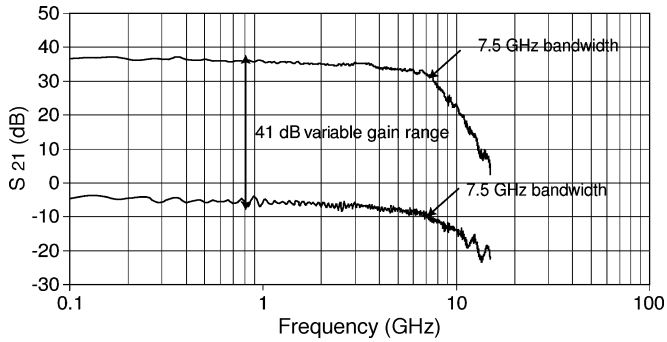


Fig. 17. Measured S_{21} of VGA at minimum and maximum gain.

an Intel LXT16727FE MUX to serialize the 16 demuxed MLSE outputs. An Intel 16713XC CDR following the MUX extracts the clock from the serialized data output for BER testing. A test buffer on the MLSE chip provides for monitoring the VGA output or the 64-divided VCO clock output. The test buffer has -8-dB gain, >30-dB SFDR, and >8-GHz 3-dB bandwidth.

The measurement setup for the MLSE receiver is shown in Fig. 15. The HP8672A feeds a 9.953–12.5-GHz clock to the Advantest D3186 pattern generator. A commercial 300-pin MZM NRZ transponder is used as a transmitter. Low gain EDFAs are inserted to control OSNR and nonlinearities. The final EDFA is used as an ASE noise source for OSNR control. A commercial PIN-TIA with a 3-dB bandwidth of 8 GHz and input sensitivity of 20 dB at BER of 1×10^{-12} is used for all measurements.

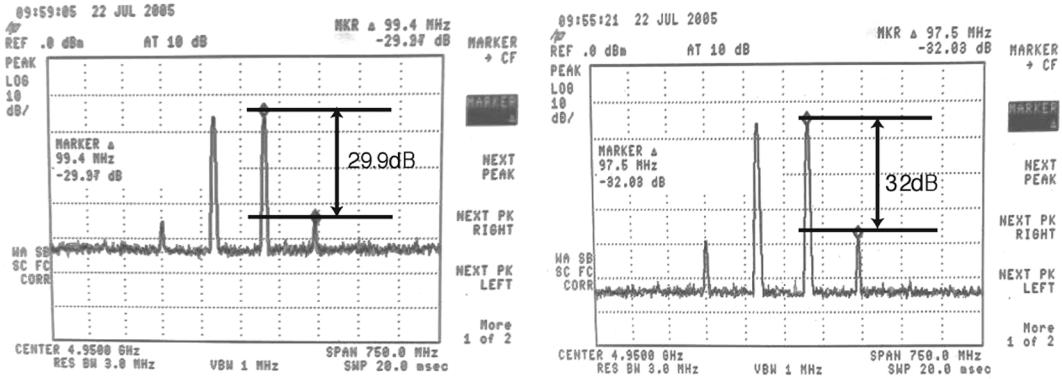
Fig. 16 shows the captured eye diagram at the output of the VGA with a $2^{31} - 1$ pseudorandom binary sequence (PRBS) and high (>25 dB) received OSNR.

Fig. 17 shows the measured S_{21} of the VGA test buffer. For a given gain setting, the input power is adjusted such that the single-ended power at the test buffer output is -10 dBm. This is done because the gain of the test buffer is -8 dB and the nominal VGA output swing is set to 1-V peak-to-peak differential. The maximum measured gain of the VGA is 37 dB and the minimum gain is -4 dB. The measured 3-dB cutoff frequency is approximately 7.5 GHz.

The linearity of 5-GHz patterns dominates EDC performance in most of the LH, ULH, and metro fiber links because they are most susceptible to dispersion. Fig. 18(a) and (b), respectively, shows the linearity of the entire VGA in the maximum and minimum gain mode around the 5-GHz frequency range. The single-ended output signal powers are set at -16 dBm with both 4.9- and 5-GHz sinusoidal input signals in both cases. The measured third-order intermodulation distortion (IM_3) is 32 dB in minimum gain mode and 29 dB in maximum gain mode. The SFDR is lower for maximum gain because all three gain blocks are cascaded.

Fig. 19 shows the measured single-ended reflection coefficient of the VGA. The termination scheme of the VGA maintains < -15 dB of S_{11} up to 5 GHz and < -10 dB up to 20 GHz. At increased transmission distances, self-phase modulation (SPM) in the optical link causes spectral broadening. Thus, maintaining low S_{11} up to a sufficiently high frequency is essential to suppress SPM-induced pattern dependencies in the BER.

Fig. 20 shows the effective number of bits (ENOB) of the ADC for various data frequencies at a sampling frequency of



(a) (b)

Fig. 18. Frequency spectrum of VGA at (a) the maximum gain and (b) the minimum gain with 4.9- and 5-GHz tone.

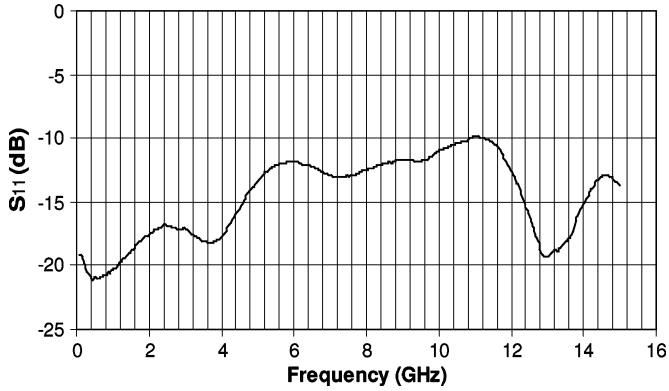


Fig. 19. Measured single-ended reflection coefficient S_{11} of the VGA.

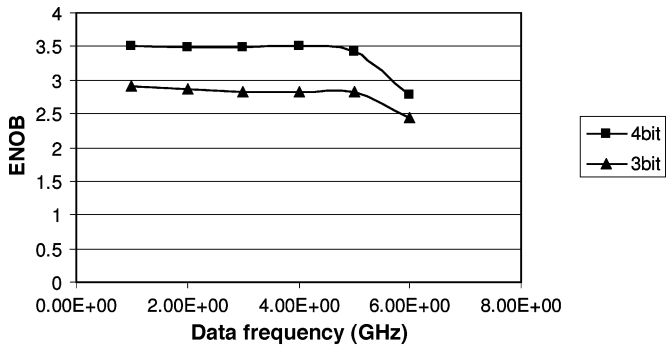


Fig. 20. 3-bit and 4-bit mode ENOB at 12.5-Gb/s sampling frequency.

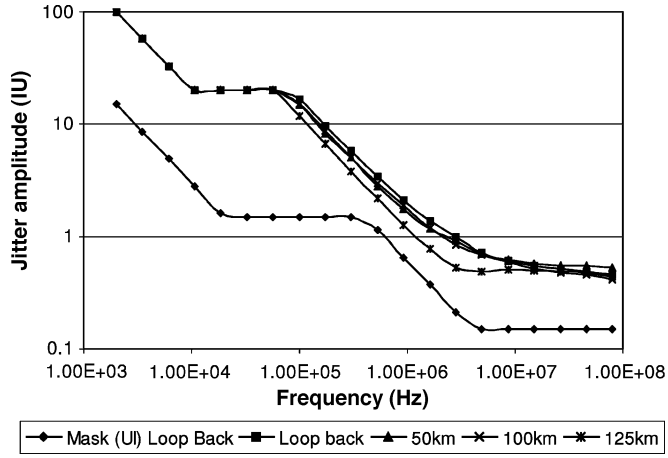


Fig. 21. Jitter tolerance of the MLSE receiver.

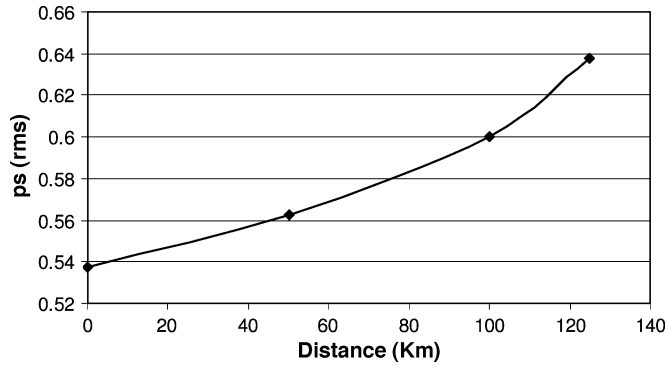


Fig. 22. Output jitter of the MLSE receiver at a BER of 10^{-3}.

12.5 GS/s. The measured ENOB at a data frequency of 5 GHz is >3.4 bit in 4-bit mode and >2.8 bit in 3-bit mode. An internally generated frequency-locked clock is used for sampling in this measurement. ENOB is calculated by comparing an ideally sampled sinusoid and captured ADC output in MATLAB. The ENOB at the Nyquist frequency with a sampling frequency of 10.71 GHz (G.709 OTN) is >3.6 b.

Fig. 21 shows the jitter tolerance performance of the MLSE receiver. A sufficient jitter tolerance margin is required in loopback to meet the SONET jitter tolerance mask [20] at longer fiber distances. The MLSE receiver satisfies the SONET jitter tolerance specifications with 2200 ps/nm of dispersion. An HP OMNIBER OTN is used for this measurement. The measured output clock jitter is $< 0.5\ \mathrm{ps_{rms}}$. Fig. 22 shows the PLL output clock jitter under practical circumstances where the MLSE receiver operates (BER $\approx 10^{-3}$). The output BER is kept at 10^{-3} and the CD is varied up to 2200 ps with a $2^{31}-1$ PRBS. The fixed BER is achieved by adjusting the OSNR while maintaining the received optical power at -14 dBm. The PLL output clock jitter is less than 0.64 $\mathrm{ps_{rms}}$ across test conditions. The PLL maintains lock without cycle slips with up to 1300 consecutive identical digits (CIDs) at a BER of 10^{-2}, with a 125-km SMF-28 optical fiber link.

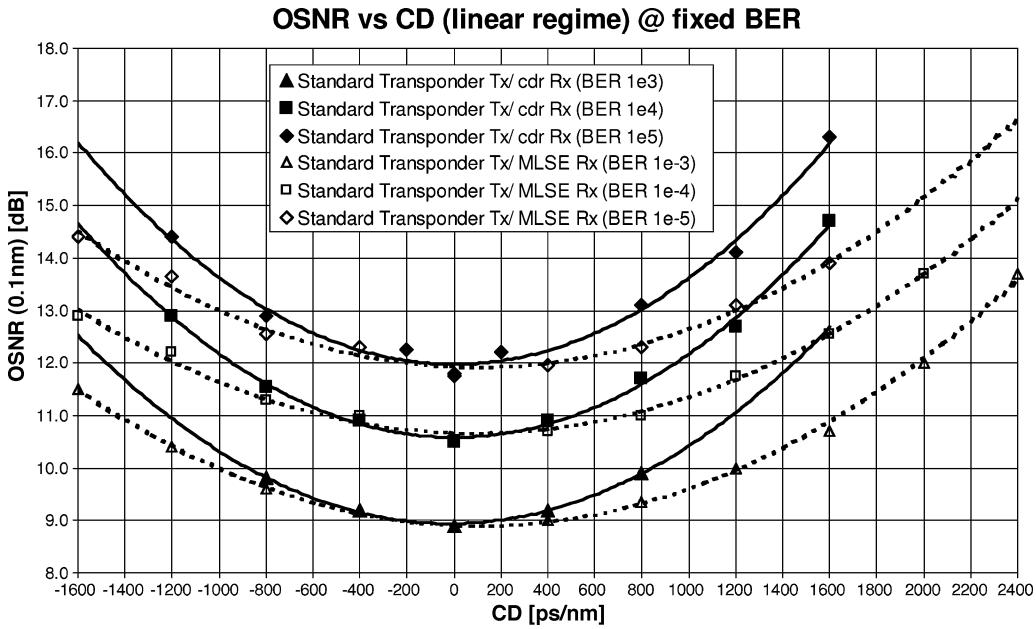


Fig. 23. OSNR penalty of standard CDR and MLSE receiver with standard 300-pin MSA transponder with $2^{31} - 1$ PRBS.

TABLE I
SUMMARY OF MLSE RECEIVER

Technology	AFE: $0.18\,\mu$m, SiGe BiCMOS (f_T=75 GHz), DE: $0.13\,\mu$m CMOS
Supply voltage	AFE: 3.3 V±0.3 V, DE: 1.2 V/2.5 V(I/O)
Data rate	9.953 GHz to 12.5 GHz
Power	ADC: 1 W, VGA: 0.3 W, PLL: 0.5 W DEMUX (4 times more complexity than conventional DEMUX): 1 W LDVS between AFE and DE: 0.7 W DE : 1 W Total : 4.5 W
Chip area	AFE: $25\,\mathrm{mm}^2$, DE: $25\,\mathrm{mm}^2$
Number of transistors	AFE: 34,100 = 24,900(FET) + 9200 (BJT), DE: 937,000 (FET)
ADC ENOB (@ 12.5 GS/s)	>3.4 (4-bit mode) with 5 GHz data >2.8 (3-bit mode) with 5 GHz data
Output	620 to 781 Mb/s LVDS
Jitter tolerance	Meets SONET spec in presence of dispersion
Jitter generation	$< 0.5\,\mathrm{ps}_{\mathrm{rms}}$
RX sensitivity	$< 5\,\mathrm{mV}_{\mathrm{pp}}$ differential
CID tolerance	1300 @ 1E-2 BER, 125 km SMF-28
Packaging	23 mm × 17 mm, 261ball FBGA (MCM)

The MLSE receiver achieves a BER of 10^{-4} at an OSNR of 14.2 dB with 2200 ps/nm of dispersion, as shown in Fig. 23. A received power of -14 dBm is used throughout the testing. The MLSE receiver reduces the OSNR penalty of a standard CDR by more than 2 dB at CD of 1600 ps/nm and a BER of 10^{-4}. The penalty for a standard CDR increases rapidly beyond 1600 ps/nm of CD. Fig. 23 also shows that the MLSE receiver does not have a penalty in the back-to-back configuration.

The receiver has been shown to provide an error free (BER $< 10^{-15}$) post-FEC output, with a pre-FEC BER of 10^{-3} at 10.71 Gb/s with 2000 ps/nm of dispersion. It can compensate for 60 ps of instantaneous differential group delay (DGD) with a 2-dB OSNR penalty (BER $= 10^{-6}$). The channel estimator in the MLSE engine adapts at a rate of 30 MHz and thus is able to track DGD variations of up to that rate.

Table I summarizes the features of the two-die solution.

IX. CONCLUSION

This paper has described the design of an MLSE-based receiver for EDC in optical links. The design of an MLSE-based receiver for optical data rates is made challenging because of the high data rates (>10 Gb/s), the linearity requirements on the front-end electronics (SFDR $>$ 18 dB), the need to recover a low-jitter clock in presence of severe dispersion (closed eye), the need for an ADC that samples at baud-rate, and the need for a high-data-rate Viterbi decoder. Furthermore, such a complex receiver needs to demonstrate a very low noise floor in order to meet the input sensitivity specifications. The design presented in this paper has met these stringent and complex specifications through a variety of innovations at the algorithmic, architectural, and circuit levels.

The use of complex DSP and linear mixed-signal circuits in optical communications is a relatively new phenomenon. The

latter leverages the cost-effectiveness of electronic solutions to optical impairments. As such numerous challenges and opportunities exist in this area. The key among these are issues related to power and performance, especially if MLSE-like techniques are to migrate into enterprise networks, which are power- and cost-sensitive applications. Key problems include robust clock recovery in presence of dispersion, low-power low-precision (6 bit or less) high-sampling rate (10 GS/s or more) ADCs, integration of complex high-frequency digital and analog blocks on the same substrate, not to mention the numerous system design issues that arise from the inherent nonlinearity of the optical channel. It is clear that innovative solutions can only be obtained by jointly addressing algorithmic, architectural, and circuit issues.

ACKNOWLEDGMENT

The authors would like to acknowledge the contributions of R. Hegde, J. Janovetz, M. Rowlands, P. Setty, P. Suppiah, and R. Walker.

REFERENCES

[1] T. Nielsen and S. Chandrasekhar, "OFC 2004 Workshop on optical and electronic mitigation of impairments," *J. Lightw. Technol.*, vol. 23, no. 1, pp. 131–142, Jan. 2005.

[2] H. F. Hauntein, K. Sticht, A. Dittrich, W. Sauer-Greff, and R. Urbansky, "Design of near optimum electrical equalizers for optical transmission in the presence of PMD," in *Proc. OFC*, 2001, pp. WAA4–1–WAA4–3.

[3] H. Bülow and G. Thielecke, "Electronic PMD mitigation—from linear equalization to maximum-likelihood detection," in *Proc. OFC*, 2001, pp. WAA3–1–WAA3–3.

[4] J. P. Elbers, H. Wernz, H. Griesser, C. Glingener, A. Faerbert, S. Langenbach, N. Stojanovic, C. Dorschky, T. Kupfer, and C. Schulien, "Measurement of the dispersion tolerance of optical duobinary with an MLSE-receiver at 10.7 Gb/s," in *Proc. OFC*, 2005, OthJ4.

[5] E. A. Lee and D. G. Messerschmitt, *Digital Communications*, 2nd ed. Norwell, MA: Kluwer, 1994.

[6] "300 pin multi source agreement for 10 gigabit transponders (SerDes transceivers)," 10 giga MSA Consortium, Apr. 2001.

[7] Y. M. Greshishchev and P. Schvan, "A 60 dB gain, 55 dB dynamic range, 10 Gb/s broadband SiGe HBT limiting amplifier," *IEEE J. Solid-State Circuits*, vol. 34, no. 12, pp. 1914–1920, Dec. 1999.

[8] M. Moller, H. M. Rein, and H. Wernz, "13 Gb/s Si-bipolar AGC amplifier IC with high gain and wide dynamic range for optical-fiber receivers," *IEEE J. Solid-State Circuits*, vol. 29, no. 7, pp. 815–822, Jul. 1994.

[9] B. Peetz, B. D. Hamilton, and J. Kang, "An 8-bit 250 megasample per second analog-to-digital converter: operation without a sample and hold," *IEEE J. Solid-State Circuits*, vol. SC-21, no. 6, pp. 997–1002, Dec. 1986.

[10] C. W. Mangelsdorf, "A 400 MHz input flash converter with error correction," *IEEE J. Solid-State Circuits*, vol. 25, no. 2, pp. 184–191, Feb. 1990.

[11] M. Choi and A. A. Abidi, "A 6-b 1.3-Gsample/s A/D converter in 0.35-μm CMOS," *IEEE J. Solid-State Circuits*, vol. 36, no. 12, pp. 1847–1858, Dec. 2001.

[12] R. Walker, *Phase-Locking in High Performance Systems*. Piscataway, NJ: IEEE Press, 2003.

[13] J. D. H. Alexander, "Clock recovery from random binary signals," *Electron. Lett.*, vol. 11, pp. 541–542, Oct. 1975.

[14] C. R. Hogge, "A self-correcting clock recovery circuits," *J. Lightw. Technol.*, vol. LT-3, no. 12, pp. 1312–1314, Dec. 1985.

[15] Y. M. Greshishchev and P. Schvan, "SiGe clock and data recovery IC with linear-type PLL for 10-Gb/s SONET application," *IEEE J. Solid-State Circuits*, vol. 35, no. 9, pp. 1353–1359, Sep. 2000.

[16] H. Werker, S. Mechnig, C. Holuigue, C. Ebner, G. Mitteregger, E. Romani, F. Roger, T. Blon, M. Moyal, M. Vena, A. Melodia, J. Fisher, G. L. G. de Mercey, and H. Geib, "A 10-GB/s SONET-compliant CMOS transceiver with low crosstalk and intrinsic jitter," *IEEE J. Solid-State Circuits*, vol. 39, no. 2, pp. 2349–2358, Dec. 2004.

[17] R. Hegde, A. Singer, and J. Janovetz, "Method and apparatus for delayed recursion decoder," U.S. Patent 2004/0264555 A1, Jun. 24, 2003.

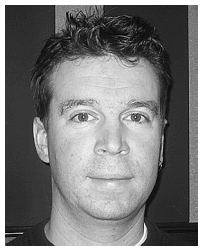
[18] "SFI-4-proposal for a common electrical interface between SONET framers and serializer/deserializer parts for OC-192 interfaces," Optical Internetworking Forum Physical and Link Layer Working Group, OIF-SFI4-01.0, Sep. 2000.

[19] P. J. Black and T. H. Meng, "A 140-Mb/s, 32-state, radix-4 Viterbi decoder," *IEEE J. Solid-State Circuits*, vol. 27, no. 12, pp. 1877–1885, Dec. 1992.

[20] "Synchronous Optical Network (SONET) Transport Systems: Common generic criteria," Telcordia Technologies, GR-253-CORE, issue 3, Sep. 2000.

Hyeon-Min Bae received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 1998 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 2001 and 2004, respectively.

From 2001 to 2006, he was the founding engineer of Intersymbol Communications Inc., Champaign, IL, which was later acquired by Kodeos Communications, South Plainfield, NJ, where he was the Lead Chip Architect and designed high-performance analog blocks including VGA, PLL, and ADC for MLSE-based receivers for 10-Gb/s fiber-optic communications.

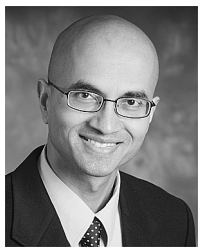


Jonathan B. Ashbrook received the B.S. and M.S. degrees in electrical engineering from the University of Illinois at Urbana-Champaign in 1998 and 2000, respectively.

From 2000 to 2002, he was with IBM, Essex Junction, VT, designing high-performance semi-custom ASICs. In 2002, he joined Intersymbol Communications Inc., Champaign, IL, where he is the Lead Digital Architect responsible for digital and mixed-signal optical receiver chips. He holds two patents in the area of high-performance memory design.

Jinki Park received the B.S. degree from Seoul National University, Seoul, Korea, in 1999, and the M.S. degree from Texas A&M University, College Station, in 2002, both in electrical engineering.

In 2003, he joined Intersymbol Communication Inc., Champaign, IL, where he was involved in designing ADC and CDR for MLSE-based electronic dispersion compensation receivers for SONET applications. Currently, he is with Texas Instruments, Dallas, TX, developing mixed-signal power management ICs.



Naresh R. Shanbhag (F'06) received the Ph.D. degree in electrical engineering from the University of Minnesota, Minneapolis, in 1993.

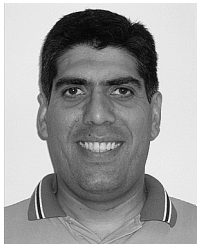
From 1993 to 1995, he was with AT&T Bell Laboratories, Murray Hill, NJ, where he was the Lead Chip Architect for AT&T's 51.84-Mb/s transceiver chips over twisted-pair wiring for asynchronous transfer mode (ATM)-LAN and very high-speed digital subscriber line (VDSL) chip-sets. Since August 1995, he has been with the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, where he is presently a Professor. His research interests are in the design of integrated circuits and systems for broadband communications including low-power/high-performance VLSI architectures for error-control coding, equalization, as well as digital integrated circuit design. He has authored or coauthored numerous publications in this area and holds three U.S. patents. He is also a coauthor of the research monograph *Pipelined Adaptive Digital Filters* (Kluwer, 1994).

Dr. Shanbhag was the recipient of the 2001 IEEE TRANSACTIONS ON VERY LARGE SCALE INTEGRATED (VLSI) SYSTEMS Best Paper Award, the 1999 IEEE Leon K. Kirchmayer Best Paper Award, the 1999 Xerox Faculty Award, the Distinguished Lecturership from the IEEE Circuits and Systems Society in 1997, the National Science Foundation CAREER Award in 1996, and the 1994 Darlington Best Paper Award from the IEEE Circuits and Systems Society. From 1997 to 1999 and from 1999 to 2002, he served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS II: ANALOG AND DIGITAL SIGNAL PROCESSING and the IEEE TRANSACTIONS ON VLSI, respectively. He has served on the technical program committees of various conferences.

Andrew C. Singer (M'95–SM'05) received the S.B., S.M., and Ph.D. degrees, all in electrical engineering and computer science, from the Massachusetts Institute of Technology (MIT), Cambridge, in 1990, 1992, and 1996, respectively.

Since 1998, he has been on the faculty of the Department of Electrical and Computer Engineering (ECE), University of Illinois at Urbana-Champaign, where he is currently an Associate Professor with the ECE Department, a Research Associate Professor with the Coordinated Science Laboratory, and a Willett Faculty Scholar. During the academic year 1996, he was a Postdoctoral Research Affiliate with the Research Laboratory of Electronics at MIT. From 1996 to 1998, he was a Research Scientist with Sanders, A Lockheed Martin Company, Manchester, NH, where he designed algorithms, architectures, and systems for a variety of DOD applications. His research spans statistical signal processing and communication systems and machine learning. In 2005, he was appointed as the Director of the Technology Entrepreneur Center (TEC) in the College of Engineering and has started several successful initiatives in the Center. He also cofounded Intersymbol Communications Inc., Champaign, IL, a venture-funded fabless semiconductor IC company. Intersymbol develops signal processing enhanced chips for ultrahigh-speed optical communications systems.

Prof. Singer is a member of of Eta Kappa Nu and Tau Beta Pi. He was a Hughes Aircraft Masters Fellow and was the recipient of the Harold L. Hazen Memorial Award for excellence in teaching in 1991. He received the National Science Foundation CAREER Award in 2000, the Xerox Faculty Research Award in 2001, and was named a Willett Faculty Scholar in 2002. He serves as an Associate Editor for the IEEE TRANSACTIONS ON SIGNAL PROCESSING and is a member of the MIT Educational Council.



Sanjiv Chopra received the B.S. degree in electrical engineering from the Birla Institute of Technology, India, the M.S. degree in electrical engineering from Iowa State University, Ames, and the M.B.A. degree from Northwestern University, Evanston, IL.

He has worked in the technology industry in various engineering and management roles for over 13 years. He has cofounded two technology startups and has served as a consultant to various others. Since 2001, he has been a Chief Operating Officer with Intersymbol Communications Inc., Champaign, IL. Intersymbol is a venture-backed technology company developing disruptive, mixed-signal integrated circuits for optical communications industry. Prior to joining Intersymbol, he was the cofounder and Executive Vice President of CapacityWeb Inc., a venture-backed supply chain technology company. From 1991 to 1997 he was with Integrated Device Technology, Silicon Valley, CA, where he developed semiconductor integrated circuit products for the personal computer and communications industry. He has also been a management consultant with Booz, Allen and Hamilton in Chicago, IL. As a Visiting Lecturer with the College of Engineering, University of Illinois, he teaches a popular graduate level course titled "Technology Innovation and Strategy."