Variation-Tolerant, Low-power PN-Code Acquisition using Stochastic Sensor NOC

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***Abstract*— Presented in this paper is an energy-efficient and variation-tolerant PN-code acquisition architecture for the wireless CDMA2000 standard. The architectures is based on the recently proposed stochastic sensor network-on-chip (SSNOC) computational paradigm [5]. The latter employs the principles of *statistically similar decomposition* and *robust estimation theory* to compensate for timing errors due to process variations. Performance of the SSNOC-based PN-code acquisition architecture at the slow process corner indicates that the average probability of detection P_{Det} improves by up to 3 orders-of-magnitude over that of the conventional architecture, while the variation in P_{Det} (σ/μ) is reduced by up to 2 orders-of-magnitude over that of the conventional architecture while simultaneously achieving a power reduction of 39%.**

I. Introduction

Nanometer CMOS process technologies in the sub-45 nm regime exhibit increased process variations. Device parameter variations result in gate delay and leakage current variations. Delay variations result in uncertainty in the data arrival time at the registers or memory elements resulting in logic errors. Process variations cause 30% variability in operating frequency in current process technology and this variability is expected to increase to 60% within the next 10 years [1]. In the presence of such increased variations, a worst-case design which avoids errors has high power consumption while the nominal design, even though it is energy-efficient, will exhibit intermittent errors. Previous schemes to *avoid* timing errors have relied on adaptive body biasing (ABB) and adaptive supply voltage (ASV) [2]. However, the effectiveness of ABB is known to decrease with reduction in channel length while ASV requires an accurate and power-hungry circuitry.

Design techniques that tolerate variations and noise are needed. Communications-inspired techniques such as *algorithmic noise-tolerance (ANT)* [3]-[4] are known to be effective at solving this problem at the architectural level. Recently, we have proposed [5] the notion of employing sensor networks-inspired techniques to jointly optimize energy-efficiency and robustness of nanometer systems-on-a-chip (SOCs). Referred to as *stochastic sensor network-on-a-chip (SSNOC)*, our approach takes the view that computational nodes can make errors and that robust low-power computation can be achieved by employing robust estimation techniques to combat errors at the architectural level.

The authors acknowledge the support of the Gigascale System Research Center (GSRC), one of five research centers funded under the Focus Center Research Program (FCRP), a Semiconductor Research Corporation program, and Texas Instruments, Inc..

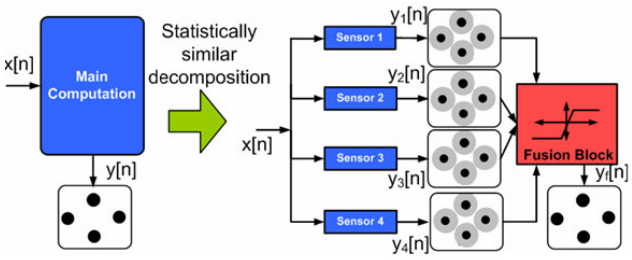

Fig. 1. The stochastic sensor network-on-a-chip (SSNOC) paradigm.

A. Contribution

In this paper, we study the performance of the SSNOC-based PN-code acquisition architecture in the presence of errors due to process variations and voltage overscaling (VOS). Under VOS, in order to push the limits of energy-efficiency, the supply voltage is reduced into the regime where timing violations occur [3]. Preliminary results showing the benefits of the proposed architecture in correcting VOS induced timing errors were presented in [5]. In this paper, we study the performance and energy-efficiency of the SSNOC in presence of both process and voltage (VOS-type) variations.

II. The SSNOC Paradigm

Figure 1 illustrates the concept of a SSNOC. Traditionally, the main computation block generates the desired output $y[n]$. The centralized nature of this computation makes it vulnerable to localized sources of non-idealities such as particle hits, hot-spots, and across die process variations and hence result in hardware errors. The SSNOC computational paradigm is based on two key principles: 1) it employs the concept of *statistically similar decomposition* to decompose a centralized computation into a network of sensors, and 2) it employs *robust estimation theory* to construct/fuse the final output from the outputs of the sensor units.

A. Statistically Similar Decomposition

In SSNOC, the main/original computation is decomposed into M ($M = 4$ in Fig. 1) lower-complexity sensors with a complexity ratio R, where R is the ratio of the complexity

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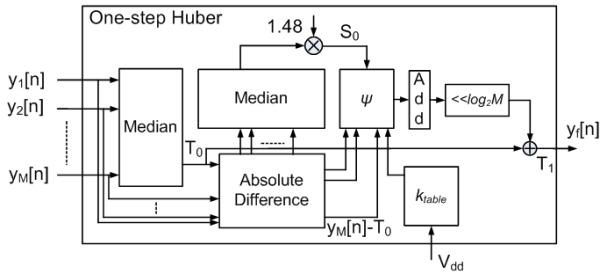


Fig. 2. One-step Huber fusion block architecture.

of one sensor to that of the main computation. The sensor output $y_i[n]$ $(i = 1, \ldots, M)$ are *statistically similar*, i.e., for $1 \leq i \leq M$

$$y_i[n] = y[n] + \eta_i[n] \tag{1}$$

$$E[y_i[n]] = y[n] \tag{2}$$

$$E[\eta_i[n]] = 0 \tag{3}$$

Note: statistical similarity implies that the mean of $y_i[n]$ is a constant across the sensors (equal to $y[n]$), the correct output at time index n. The gray regions in Fig. 1 refer to the fact that instantaneous values of the sensor outputs $y_i[n]$ may not equal the correct output. Thus, an SSNOC is characterized by two key parameters, the complexity ratio R and the decomposition factor M (or the number of sensors).

Note that in the SSNOC, $\eta_i[n]$, the errors in the sensor outputs arise from two sources: 1) $\eta_{e,i}[n]$, estimation error due to the use of low-complexity sensors, and 2) $\eta_{h,i}[n]$, hardware error due to the non-idealities in process, voltage or temperature. Irrespective of the error source, a fusion block combines the sensor outputs to produce an output $y_f[n]$, which is statistically close to the correct output $y[n]$. The algorithm resident in the fusion block is described next.

B. Robust Estimation

Sensor output errors can be modeled as random variables drawn from a distribution that is Gaussian (estimation error) with probability $(1 - \epsilon)$ and some unknown distribution with probability ϵ (due to process/voltage non-idealities) for some $0 < \epsilon < 1$, i.e., an ϵ-contaminated distribution. In the following, for the sake of simplicity, we drop the time index n. Thus,

$$y_i = \theta + \eta_i \qquad \text{for } 1 \leq i \leq M. \tag{4}$$

where M is the decomposition factor/number of sensors, y_i is the i^{th} sensor output, θ is the desired output and η_i is the additive noise.

Huber [6] shows that the following class of estimators, known as *M-Estimators*, are optimal in a certain robust sense:

$$\sum_{k=1}^{M} \psi[y_k - \theta] = 0 \tag{5}$$

where ψ is a general odd-symmetric function known as the influence function, and for ϵ-contaminated $\mathcal{N}(0, 1)$ distributions,

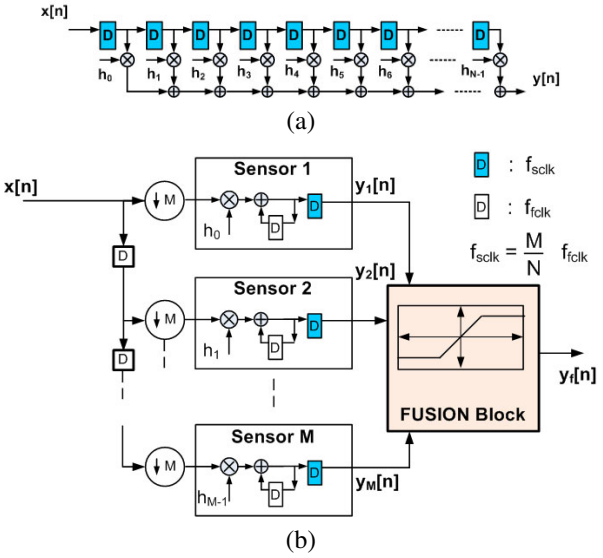


Fig. 3. Matched filter for PN-acquisition: (a) traditional, and (b) an SSNOC-based matched filter.

ψ is given by

$$\psi(y, k) = \begin{cases} y, & \text{if } |y| \leq k \\ k \text{ sgn}(y), & \text{else.} \end{cases} \tag{6}$$

where k is a constant that depends only on ϵ and the nominal distribution, $\mathcal{N}(0, 1)$ [6]. The *One-step Huber* algorithm [6] can be employed to compute the parameters of the estimator, as shown below:

1) Compute scale estimate (Median Absolute Deviation):

$$\begin{aligned} T_0 &= \text{median}\{y_i\} \\ S_0 &= 1.4826 * \text{median}\{|y_i - T_0|\} \end{aligned}$$

2) Compute location estimate:

$$T_1 = T_0 + \frac{\frac{1}{M}\sum_i \psi(y_i - T_0, S_0 \cdot k_{table})}{0.5}$$

where 0.5 is used to approximate $\frac{1}{M}\sum_i \psi'(\frac{y_i - T_0}{S_0})$ [6].

The One-step Huber architecture is shown in Fig. 2. The median filter for the robust fusion algorithm is implemented using the architecture described in [11]. The value of k_{table} is pre-characterized and stored in a ROM. It needs to be read only once by the ψ block depending upon ϵ, the probability of hardware error due to non-idealities of process/voltage.

III. SSNOC-based PN-Code Acquisition System

The system level throughput requirements for the PN-code acquisition system was fixed at 12.5 Mchips/s. We chose a PN-code of length $N = 256$ from a subset of the length 2^{15} PN sequence specified in the CDMA2000 standard. The received signal was assumed to be an 8-bit length-1000 subsequence of the same PN sequence corrupted by AWGN channel noise to yield an $SNR = -12$dB.

A. Conventional Architecture

Figure 3(a) shows the traditional centralized direct form implementation of the matched filter. Multiply-accumulate (MAC) units are commonly employed to compute the correlation of the received signal with the PN-code [8]. The tap weights of the MAC are the PN-code bits. The peaks in the output of the MAC are used for detection. In the conventional architecture, the MACs are designed and operated at a critical supply voltage $V_{dd-crit}$, such that the worst-case critical path (with respect to process/voltage/temperature corner and input combination) is less than the clock period.

B. SSNOC-based Architecture

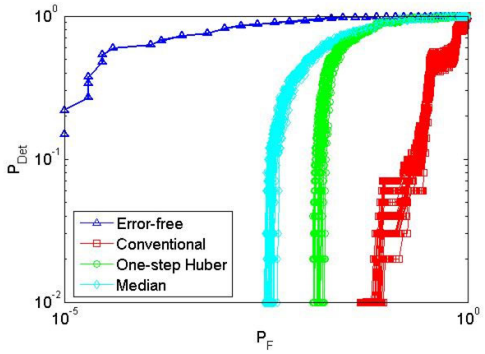
In the SSNOC-based design, statistically similar decomposition is achieved via poly-phase decomposition as shown in Fig. 3(b). The M sensor outputs exhibit an estimation error $\eta_{e,i}[n] = y[n] - My_i[n]$ due to input subsampling even under error-free hardware operation. Additionally, the sensors will generate timing errors due to delay variations induced by process, temperature and voltage variations. The fusion block is implemented using T_1 in One-step Huber, and the median T_0 in the Huber algorithm. For a fair comparison, the conventional matched filter in Fig. 3(a) is also polyphase decomposed [9] as in Fig. 3(b) but with an M-operand adder in place of the fusion block.

IV. Simulation Setup and Results

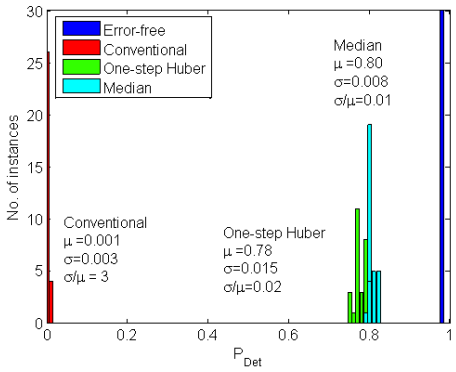
Process variations are classified as die-to-die (D2D) and within-die (WID) variations. The standard deviation of the gate delay due to D2D process variations is denoted as σ_g.

A. Simulation Setup

We first characterized the delay distribution of basic gates such as an inverter, xor, and a full adder due to WID variations at various values of the supply and body bias voltage combinations (V_{dd},V_b) for an IBM 130nm CMOS process. Next, we sample the distributions in order to obtain the gate delays of a gate level implementation of the sensor MACs at: 1) the $3\sigma_g$ slow process corner operating at critical supply voltage $V_{dd-crit} = 1.2V$ corresponding to nominal process corner, 2) the $3\sigma_g$ slow process corner operating at sub-critical supply voltage, 3) the $3\sigma_g$ slow process corner operating under adaptive supply voltage (ASV) and adaptive body bias voltage (ABB). This process is repeated 30 times in order to obtain 30 instances of the conventional and SSNOC architectures. We simulate the conventional and the SSNOC architectures using the HDL simulator which operates at the gate-level to determine the MAC outputs. Each of the 30 instances of either the conventional or SSNOC architecture results in a different performance. This is because the path delay distribution and hence the timing violations will be different for each instance. Each instance output is post-processed 1000 times using Matlab to compute the receiver operating characteristic (ROC), the probability of detection (P_{Det}) versus probability of false-alarm (P_F). A threshold detector is used to evaluate ROC by sweeping the threshold. Detection event is defined as correct detection of a PN-code in the input stream by the threshold detector. We assumed $P_F = 5\%$ in order to compare P_{Det} vs. power trade-off [13].



(a)



(b)

Fig. 4. (a) ROCs and (b) pdfs of P_{Det} (at a $P_F = 5\%$) of the conventional and the SSNOC architectures due to WID variations at $3\sigma_g$ slow process corner.

B. Simulation Results

The ROCs and the P_{Det} distributions due to WID variations at $3\sigma_g$ slow process corner are shown in Fig. 4. Similar plots were obtained for the other two cases enumerated above corresponding to VOS and ABB/ASV respectively. The means μ_i and the standard deviations σ_i of the P_{Det} corresponding to these cases are tabulated in Table I. We note from Fig. 4 and Table I that the mean P_{Det} drops by close to 3 orders-of-magnitude for the conventional architecture at the $3\sigma_g$ slow process corner operating at supply voltage $V_{dd-crit} = 1.2$. The SSNOC architecture improves P_{Det} by close to 3 orders-of-magnitude over the conventional architecture under identical process and voltage conditions. In addition, the SSNOC improves the variation in P_{Det} (σ/μ) by 2 orders-of-magnitude. Table I indicates that the SSNOC architecture with One-step Huber and the median block provides an improvement of more than 1 order-of-magnitude and 2 orders-of-magnitude, respectively, in the presence of VOS and a $3\sigma_g$ slow process corner. Finally, we note that the conventional architecture with ABB/ASV recovers its loss in detection performance to

TABLE I

CHARACTERISTICS OF P_{Det} DISTRIBUTIONS (AT A $P_F = 5\%$) OF THE THREE ARCHITECTURES ON A $3\sigma_g$ SLOW DIE DUE TO WID VARIATIONS.

M		Process			Process and VOS			Process and ASV/ABB		
		Conventional	SSNOC (median)	SSNOC (Huber)	Conventional	SSNOC (median)	SSNOC (Huber)	Conventional	SSNOC (median)	SSNOC (Huber)
8	μ_i	0.001	0.80	0.78	0.0009	0.4773	0.016	0.83	0.969	0.977
	σ_i	0.003	0.008	0.015	0.01	0.0571	0.0089	0.24	0.003	0.0047
	σ_i/μ_i	3	0.02	0.01	10	0.12	0.5	0.29	0.003	0.0048
32	μ_i	0.128	0.89	0.94	0.026	0.61	0.63	0.57	0.92	0.97
	σ_i	0.034	0.015	0.015	0.0156	0.038	0.044	0.01	0.0019	0.046
	σ_i/μ_i	0.27	0.016	0.016	0.59	0.063	0.07	0.08	0.002	0.01

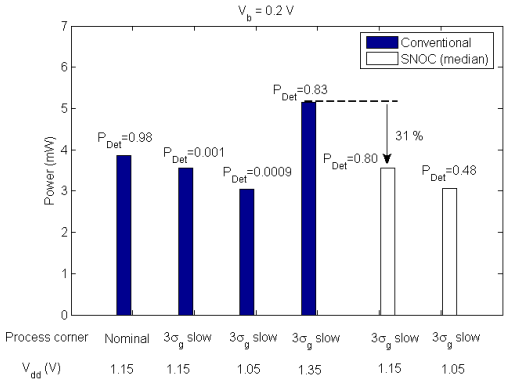


Fig. 5. Power vs. P_{Det} trade-off (at a $P_F = 5\%$).

achieve a $P_{Det} \approx 0.83$, which is comparable to that achieved by the SSNOC architecture. However, the SSNOC has a 2 orders-of-magnitude better (smaller) P_{Det} variation (σ/μ), and a smaller power as shown later. Table I further indicates that the performance degradation due to process variations is reduced with an increase in the number of sensors from $M = 8$ to $M = 32$ for all architectures. Since the performance of the median is comparable to that of the One-step Huber, we choose the SSNOC with median fusion block in the following discussion of power-performance trade-off.

C. Power vs. Performance Trade-offs

We compare power consumption of the SSNOC architecture with that of the conventional architecture. We simulate the transistor level netlists of sensors (MACs) in the conventional and the SSNOC architecture using HSPICE with a few random input vectors to obtain the power consumption of the sensors at different supply and body-bias voltages. The power consumption of the fusion blocks (M-operand adder and median) are obtained using *Synopsys Design Analyzer*.

In Fig. 5, the first bar shows the power consumed by the conventional architecture operating under error-free conditions on a nominal process die. The supply voltage and MOS body bias voltage, i.e., (V_{dd}, V_b), are adjusted in order to minimize power. We note that the error-free P_{Det} is 0.98 with a power consumption of $3.85mW$ at $(1.15V, 0.2V)$ and the nominal process corner. As seen before, at the $3\sigma_g$ slow process corner, with or without VOS, the mean P_{Det} of the conventional architecture drops by up to 3 orders-of-magnitude while the power consumption drops slightly to $3.55mW$ (slow process) and $3.054mW$ (slow process and VOS ($V_{dd} = 1.05V$)). Under identical conditions, the SSNOC architecture consumes $3.551mW$ (slow process) and $3.055mW$ (slow process and VOS($V_{dd} = 1.05V$)), which is not too different from the conventional architecture but provides up to 3 orders-of-magnitude improvement in P_{Det} and up to 2 orders-of-magnitude improvement in P_{Det} variation. The application of ABB and ASV to reduce the gate delays and correct the timing errors increases the power consumption of the conventional architecture to $5.152mW$ at $(1.35V, 0.2V)$ while achieving a mean $P_{Det} = 0.83$. The SSNOC architecture achieves a comparable $P_{Det} = 0.80$ but consumes $3.551mW$ of power, which is 31% lower power than the conventional architecture. It can also be shown that with nearly equal mean P_{Det}s, the SSNOC results in 39% power savings with $M = 32$. Thus, SSNOC is able to trade-off power and performance very effectively and its probability of detection P_{Det} is robust to process variations.

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