MODELING AND MITIGATION OF JITTER IN HIGH-SPEED SOURCE-SYNCHRONOUS INTER-CHIP COMMUNICATION SYSTEMS

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ABSTRACT

Jitter significantly limits the maximum achievable data rates (MADR) over high-speed source-synchronous I/O links. In this paper, we present a simple model that comprehends transmitter and receiver jitter in a source-synchronous I/O link. We show that the channel can have a significant impact on transmit jitter at high data rates, resulting in 1.1X-3.8X jitter amplification for typical cases. We quantify the performance degradation of transmit/receive equalization and multi-level modulation schemes, due to jitter in high-speed I/O links. We present two design techniques to mitigate the effect of jitter on performance - transmission of a slower source-synchronous clock, and jitter equalization. Both techniques can improve MADR by 13% when signaling over a 20" FR4 channel.

1. INTRODUCTION

The relentless progress of integrated circuit technology has pushed on-chip processing capability into the multi-GHz regime. The translation of this increased computation capability into an improvement in overall system performance requires reliable, high-speed inter-chip communication networks. The analysis and design of high-speed I/O circuits is thus an important part of designing a multi-GHz digital system. Data rates in recently published I/O links are approaching 10 Gbps [1, 2], a regime where channel and signaling non-idealities have a significant impact on link performance. Intersymbol interference (ISI) is the dominant channel impairment, while jitter is the principal noise introduced by the signaling circuits. The frequency response of a typical I/O channel (20" FR4 with two connectors), shown in Fig. 1, clearly illustrates the significance of ISI at data rates beyond 5 Gbps. While signaling over ISI channels is well understood [3], the impact of jitter on the performance of high-speed I/O links has not been adequately modeled or analyzed. In this paper, we propose models and analysis methods to comprehend jitter in an important class of I/O systems that use source-synchronous signaling.

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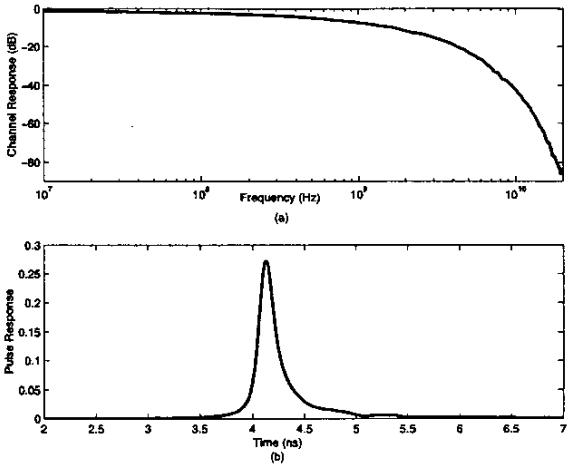

Fig. 1. (a) Frequency response of a typical high-speed I/O channel. The channel consists of a 20" FR4 trace, two connectors, and a 1 pF capacitance at its two ends. (b) Response of the channel to a 100 ps input pulse.

Source-synchronous signaling is a widely accepted technique for high-speed parallel bus interfaces in digital systems [1, 4] (see Fig. 2). The distinctive feature of this signaling scheme is the presence of a clock channel to transmit the clock used to generate the parallel data stream. The receive path is simplified to a DLL (for clock deskew [1]) instead of an expensive clock-data recovery (CDR) unit. Another motivation for the explicit transmission of the clock is to enable better tracking of jitter between clock and data. The effect of the channel on jitter tracking performance has however not been studied. In this paper, we will quantify the impact of the channel on jitter and show that it significantly limits the maximum achievable data rate (MADR).

Jitter can be broadly defined as random variations in the phase of a nominally periodic signal. More specifically, we define jitter to be a random sequence whose elements represent the deviation of the actual zero-crossings (the instant when the clock signal crosses a certain threshold) from the zero-crossings of an ideal reference clock. The main source of jitter in the I/O link shown in Fig. 2 is the transmitter

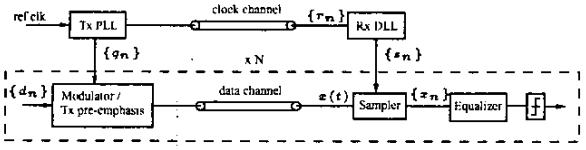

Fig. 2. Schematic view of a source-synchronous I/O system. A separate channel is dedicated to transmit the clock, which is then deskewed at the receiver by a delay locked loop (DLL) to sample at the middle of the data eye. The cost of the additional clock channel is amortized by sharing it among several parallel data channels.

PLL/clock distribution network, whose noise is highly colored [5]. In this paper, we will show that the frequency distribution of jitter can have a significant effect on achievable data rates.

In the next section, we develop a first-order model that comprehends both transmit and receive jitter on the received data samples. This is followed by an analysis of the effect of the channel on the transmit clock jitter and the derivation of an equivalent jitter transfer function from the channel response. We then investigate the effect of jitter on the performance of commonly used equalization and modulation schemes. Finally, we discuss design techniques to mitigate the effect of jitter.

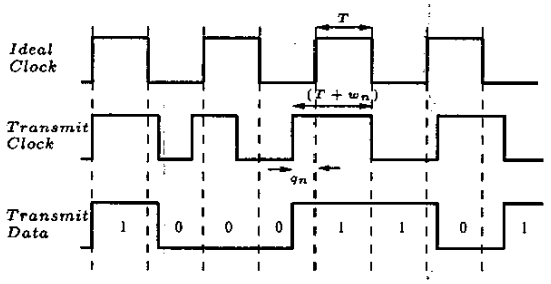

Fig. 3. Figure showing the interpretation of accumulated jitter q_n and period jitter w_n in the transmit clock.

2. SOURCE-SYNCHRONOUS I/O JITTER MODEL

In this section, we derive a model to analyze the effect of jitter in the source-synchronous link shown in Fig. 2.

2.1. First Order Model for Transmit and Receive Jitter

In Fig. 2, the transmit symbols $\{d_n\}$ are modulated by the transmit clock whose accumulated jitter is described by the random sequence $\{q_n\}$ (see Fig. 3). We want to relate the received samples $\{x_n\}$ to $\{q_n\}$, and the sampling jitter $\{s_n\}$. The modulated waveform $d_T(t)$ that is transmitted over the channel is given by,

$$d_T(t) = \sum_k d_k r(t - kT - q_k, w_k) \quad (1)$$

where $r(t, w)$ is the modulation pulse (typically a rectangular pulse) of width $(T+w)$, T is the nominal symbol period, and the sequence $\{w_n\}$ is represents the period jitter (cycle-to-cycle variations in the symbol period - Fig. 3) which is related to $\{q_n\}$ by,

$$w_n = q_{n+1} - q_n \quad (2)$$

The received waveform $x(t)$ (without additive noise) is

$$x(t) = d_T(t) * f(t) = \sum_k d_k h(t - kT - q_k, w_k) \quad (3)$$

where $f(t)$ is the channel impulse response, and $h(t, w) = f(t) \star r(t, w)$ is the response of the channel to the modulation pulse $r(t, w)$. If $\{s_n\}$ is the sampling jitter sequence, the received sample sequence $\{x_n\}$ is given by,

$$\begin{aligned} x_n &= x(t_0 + nT + s_n) \\ &= \sum_k d_k h(t_0 + (n-k)T + s_n - q_k, w_k) \end{aligned} \quad (4)$$

where t_0 is the sampling offset. Using Taylor's series expansion, maintaining only first-order terms, and assuming a rectangular modulation pulse $r(t)$, we get the following expression for the received sample sequence $\{x_n\}$:

$$\begin{aligned} x_n \quad = \quad & \sum_k d_k h_{n-k} - \sum_k v_k q_k f_{0,n-k} \\ & + s_n \sum_k v_k f_{0,n-k} \end{aligned} \quad (5)$$

where $v_k = (d_k - d_{k-1})$, and $\{f_{0,n}\} = \{f(t_0 + nT)\}$, is the sampled channel impulse response. The first term models ISI, while the second and third terms convert jitter at the transmitter and receiver into equivalent voltage noise. The model above shows that the effect of jitter depends on the data transition density (non-zero v_k) and the channel response. It also shows that small-amplitude jitter is a proportional noise source, whose energy scales with transmit signal energy.

2.2. Effect of the channel on transmit jitter

The principal reason for explicit transmission of the clock in a source-synchronous system is to maximize the correlation between jitter in data and clock across a wide band of jitter frequencies. Below, we show that the channel can have a significant impact on the level of 'jitter tracking', especially at high data rates. We present two derivations that lead to equivalent results, one in the time domain and another in the frequency domain.

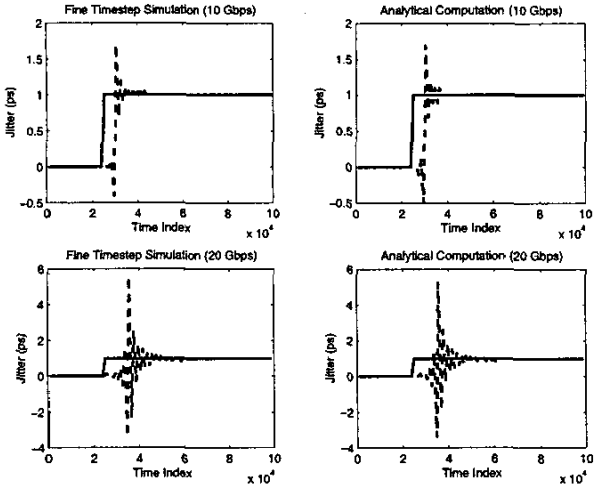

Fig. 4. Effect of a 20" FR4 channel on a 1 ps transmit jitter step at two data rates - 10 Gbps (top), 20 Gbps (bottom). Results obtained from a fine timestep simulation (left) are compared with those obtained analytically from equation (8) (right). The fine timestep simulation used a time resolution of 100fs at 10 Gbps, and 50fs at 20 Gbps. The solid line in the figure shows transmit jitter, while the dotted line shows the receive jitter.

2.2.1. Time Domain Analysis

In source-synchronous links, alternating binary data is usually transmitted on the clock channel and both the rising and falling edges of the clock are used to sample the receive waveform. The transmit clock waveform with jitter is filtered by the channel and is received as,

$$c(t) = \sum_k (-1)^k h(t - kT - q_k, w_k) \tag{6}$$

If the ideal zero-crossings occur at (t_c+nT), and the receive jitter sequence is $\{r_n\}$, then

$$c(t_c + nT + r_n) = \sum_k (-1)^k h(t_c + (n-k)T + r_n - q_k, w_k) \tag{7}$$

should equal zero. An approximate solution for the receive jitter can be derived using a first-order Taylor's series expansion (followed by simplifications similar to the previous section) :

$$r_n = \frac{\sum_k (-1)^k f_{c,k} q_{n-k}}{\sum_k (-1)^k f_{c,k}} \tag{8}$$

where $\{f_{c,n}\} = \{f(t_c + nT)\}$, with $f(t)$ being the impulse response of the channel. Thus, the effect of the channel on transmit jitter can be modeled by a filter $\{g_n\}$ given by,

$$g_n = \frac{(-1)^n f_{c,n}}{\sum_k (-1)^k f_{c,k}} \tag{9}$$

The discrete-time fourier transform (DTFT) of the above equation gives the jitter transfer function (JTF) :

$$G(e^{j\omega}) = \frac{F_c(e^{j(\omega+\pi)})}{F_c(e^{j\pi})} \tag{10}$$

$F_c(e^{j\omega})$ is an aliased version of the channel response and generally has a low pass characteristic (see Fig. 1). However, due to the π-shift in the JTF (equation (10)), $G(e^{j\omega})$ has a high-pass characteristic that results in amplification of high frequency transmit jitter. This effect is illustrated in Fig. 4, which shows the receive jitter due to a 1 ps step in transmit jitter for two data rates. The amplifying effect of the channel is apparent from the overshoot and ringing in the step response. As data (and hence clock) rates increase, $F_c(e^{j\omega})$ becomes increasingly low-pass in nature resulting in a larger amplification of transmit jitter (by equation (10)). This is illustrated in Fig. 5, which shows that the rms jitter of the transmit clock can be amplified by $> 3X$ under appropriate conditions (high data rate and/or high jitter bandwidth). The consequences of this jitter amplification for source-synchronous signaling are explored in a section 3.

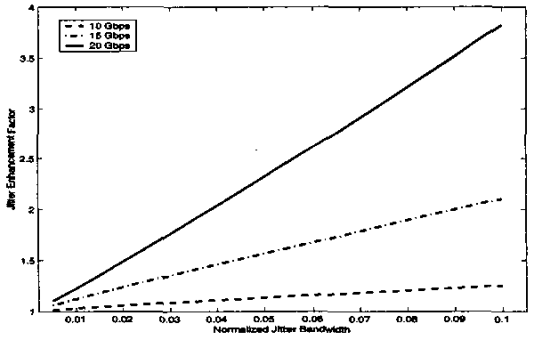

Fig. 5. Dependence of jitter amplification factor (ratio of the receive rms jitter to the transmit rms jitter) on the normalized jitter bandwidth (ratio of jitter bandwidth to data rate) for a 20" FR4 channel. It can be seen that the effect of the channel on jitter increases dramatically with data rate.

2.2.2. Frequency Domain Analysis

In this section, we approximate the clock waveform to be sinusoidal and derive the effect of the channel on the phase noise in the clock. The clock waveform modulated by phase noise can be expressed as ,

$$c(t) = Acos(2\pi f_c t + \beta sin 2\pi f_m t) \tag{11}$$

where f_c is the clock frequency, f_m is the phase modulation frequency, and β is the amplitude of the phase noise. For small β, we may approximate equation (11) as follows :

$$c(t) \approx Acos(2\pi f_c t) - \frac{\beta A}{2}(cos(2\pi f_L t) - cos(2\pi f_H t))$$

(12)

where $f_H = f_c + f_m$, and $f_H = f_c - f_m$. The Fourier transform $C(f)$ of $c(t)$ is symmetric about $f = 0$ and is given for positive frequencies by,

$$C(f) \approx \frac{A}{2}\delta(f-f_c) - \frac{\beta A}{4}[\delta(f-f_L) - \delta(f-f_H)] \quad (13)$$

We will assume a linear phase channel $H(f)$ with zero group delay (the results can be easily shown to hold for non-zero group delay) and denote $H(f_c)$ by α_c, $H(f_L)$ by α_L, and $H(f_H)$ by α_H. The receive clock spectrum $S(f)$ is given by,

$$S(f) = \frac{\alpha_c A}{2}\delta(f-f_c) - \frac{\beta A}{4}[\alpha_L\delta(f-f_L) - \alpha_H\delta(f-f_H)] \quad (14)$$

We may express the received clock $s(t)$ as,

$$s(t) = A_r cos(2\pi f_c t + \beta_r sin 2\pi f_m t) \quad (15)$$

where A_r is the received clock amplitude, and β_r is the received phase modulation amplitude. Equating equation (15) and the inverse Fourier transform of equation (14), and assuming small amplitude phase noise, we get

$$A_r \approx \alpha_c A \quad (16)$$

$$\beta_r \approx (\frac{\alpha_L + \alpha_H}{2\alpha_c})\beta \quad (17)$$

If $\beta_r > \beta$, we have phase noise amplification. This can happen if the channel response has a strong frequency roll-off near the clock frequency f_c. For example, if $H(f)$ varies exponentially as $e^{-\gamma f}$ near f_c, the amplification factor is $cosh(\gamma f_m)$ and phase noise will get amplified at all frequency offsets. As I/O data rates increase, the channel exhibits significant frequency dependent attenuation near f_c and hence the effect of the channel on phase noise (and hence jitter) becomes more pronounced.

Thus, both the time and frequency domain analysis show that the effect of the channel can be significant at high data rates and for high frequency transmit jitter.

2.3. Complete jitter model

We can now relate the jitter in the sampling clock, $\{s_n\}$, to the jitter in the transmit clock, $\{q_n\}$. If the clock propagation delay in the receiver is D symbols, the sampling jitter sequence $\{s_n\}$ is defined by,

$$s_n = r_{n-D} + u_n \quad (18)$$

where r_n is given by equation (8), and $\{u_n\}$ is the additional jitter (independent of the transmit jitter $\{q_n\}$) introduced by the receive clock path (DLL and clock distribution network). Typical values for D range from 5-10 symbol periods. In this paper, D is assumed to equal 5 symbol periods. The sampling jitter $\{s_n\}$ is zero-mean and its second-order statistical properties can be related to those of $\{q_n\}$ and $\{u_n\}$ as follows (assuming jitter to be wide-sense stationary):

$$R_{sq}(\Delta) = \frac{\sum_k (-1)^k f_{c,k} R_{qq}(k - \Delta + D)}{\sum_k (-1)^k f_{c,k}} \quad (19)$$

$$R_{ss}(\Delta) = \frac{\sum_k \sum_l (-1)^{k+l} f_{c,k} f_{c,l} R_{qq}(\Delta - k + l)}{\sum_k \sum_l (-1)^{k+l} f_{c,k} f_{c,l}} + R_{uu}(\Delta) \quad (20)$$

These relationships capture the effect of the channel and transmit jitter PSD on the sampling jitter PSD and transmit-receive jitter tracking.

A discrete-time system model that can be used to analyze jitter in a source-synchronous link is shown in Fig. 6. Both transmit pre-emphasis ($P(z)$) and receive equalization ($C(z)$) are included in the model. $H(z)$ and $F(z)$ are the channel pulse and impulse responses respectively, and $K(z) = 1 - z^{-1}$. $G(z)$ represents the jitter transfer function and $\{z_n\}$ is the additive white gaussian noise. We will use this model in later sections to analyze the effect of jitter on the performance of various equalization schemes.

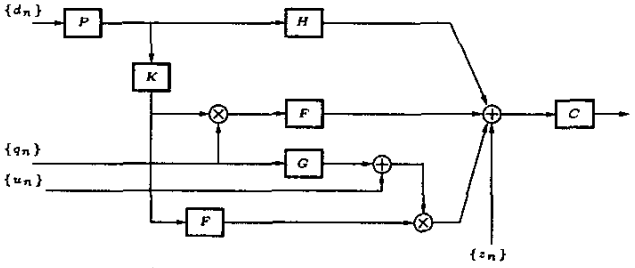

Fig. 6. A discrete-time system model to analyze the effect of jitter in source-synchronous I/O links. P represents the transmit pre-emphasis filter, F (H) the channel impulse (pulse) response, G the jitter transfer function, and C the receive linear equalizer.

3. EFFECT OF JITTER ON EQUALIZATION AND MODULATION

Many recent high-speed I/O links employ equalization and multi-level signaling ([1], [2], [6]) to combat ISI and increase data rates. The effect of jitter on these signaling enhancements has however not been studied. In this section, we analyze the effect of jitter on the performance of transmit/receive equalization and multi-level modulation schemes. We first present the I/O noise model used in this paper to quantify the effect of jitter.

3.1. I/O Noise Source Models

The prinicipal sources of voltage noise in an I/O link are the thermal noise in the termination resistors, the sampler, and

the input amplifier. The voltage noise PSD (in V^2/Hz) due to these sources can be expressed as [7],

$$N_{0,v} = 4kT(R_{term} + R_{sw} + \frac{\alpha}{g_m}) \quad (21)$$

where R_{term} is the termination resistance, R_{sw} is the switch resistance, g_m is the input stage transconductance, and α is a technology-dependent parameter. In this paper, we used typical values of 50 Ω, 200 Ω, 1 mA/V and unity for R_{term}, R_{sw}, g_m, and α respectively, which gives a noise PSD of 2×10^{-17} V^2/Hz. The main sources of timing noise are jitter introduced by the transmit PLL/clock distribution, and the receive DLL. The transmit PLL output noise [5] due to reference and VCO noise can be modeled reasonably well by a white gaussian noise (WGN) source filtered by a first order Butterworth filter. In this paper, the 1σ value of the transmit jitter is assumed to be 0.03 UI, which is consistent with rms jitter values that have been observed in I/O links. The receive DLL noise is modeled as WGN with a 1σ value of 0.02 UI.

3.2. Jitter and Equalization

Recent I/O links have reported significant improvements in data rates through the use of transmit and receive linear equalizers([1], [2], [6]). Transmit equalizers are subject to a peak transmit power constraint that leads to reduction in signal energy, while receive equalizers suffer from the noise enhancement problem. However, due to the relative simplicity of their implementation, we can expect to see increasingly complex transmit and receive equalizers in multi-Gbps I/O links. Hence it is important to study the effectiveness and scalability of these techniques in the presence of jitter.

The performance of receive equalization in the presence of jitter can be derived using the system model shown in Fig. 6 and the Weiner-Hopf equation [8] for achievable SNR. The bit error rate (BER) can be estimated from SNR as follows :

$$P_b \approx \frac{2(M-1)}{Mlog_2M} Q(\sqrt{\frac{3SNR}{M^2-1}}) \quad (22)$$

where M is the number of signaling levels, and $Q(x) = 0.5erfc(x/\sqrt{2})$. The maximum achievable data rates (MADR) assuming a target BER of 10^{-18} for various equalizer lengths is shown in Fig. 7. It can be seen that jitter causes a significant degradation in MADR as the number of equalizer taps increases. This is because the reduction in ISI due to additional equalizer taps is countered by the enhancement of jitter noise at higher data rates, leading to a premature saturation of performance as seen in Fig. 7. The noise enhancement problem does not exist with transmit pre-emphasis, which results in a smaller degradation in performance due to jitter as shown in Fig. 7.

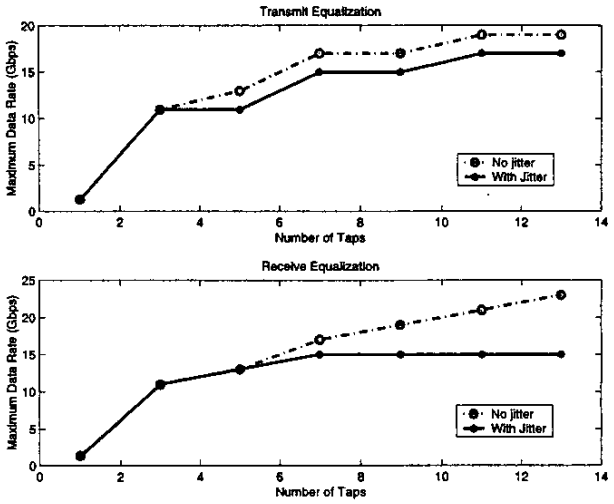

Fig. 7. Variation of maximum achievable data rate (MADR) with number of equalizer taps, when using receive LE (top) and transmit pre-emphasis (bottom). The 1σ value of transmit (receive) jitter is 0.03 UI (0.02 UI) and the transmit jitter bandwidth normalized to the data rate is 0.05. The target BER is 10^{-18}.

3.3. Jitter and Multi-level Modulation

Multi-level modulation (also called pulse amplitude modulation or PAM) is a means to combat ISI by transmitting multiple bits per symbol. While early I/O links used binary signaling (2-PAM), recent I/O systems have used 4-PAM and even 8-PAM. The MADR for various modulation schemes can be computed as in the previous subsection using equation (22). The results are plotted in Fig. 8. It can be seen that the effect of jitter becomes more significant as the number of signaling levels increases. While 2-PAM suffers a 23% degradation in MADR, the corresponding figure for 8-PAM is 73%, when we have 13 equalizer taps. This is because the addition of jitter causes the MADR to be determined by additive noise rather than ISI, and multi-level signaling schemes are more vulnerable to noise due to the closer spacing of signal levels. Fig. 8 shows that binary signaling can achieve near-optimum performance when significant amount of jitter is present.

4. MITIGATION OF JITTER

Jitter can cause a significant degradation in achievable data rates as shown in the previous section. From the previous sections, we can conclude that the effect of transmit jitter can be mitigated by decreasing the high frequency component of jitter. This can be done by careful design of the transmit PLL (comprehending the effect of the channel on jitter) and the transmit clock distribution network. In this section, we present two design techniques that can be used

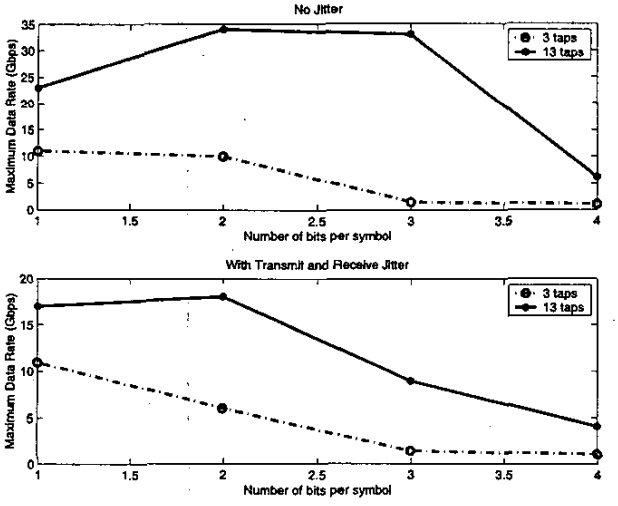

Fig. 8. Variation of maximum achievable data rate (MADR) with number of signaling levels for two different equalizer lengths. The top plot shows the behavior in the absence of jitter, while the bottom plot assumes 0.03 UI (0.02 UI) transmit (receive) jitter (1σ). The jitter bandwidth normalized to the data rate is 0:05.

to mitigate the loss in performance. Both the techniques require minimal modification to the existing transceiver circuits.

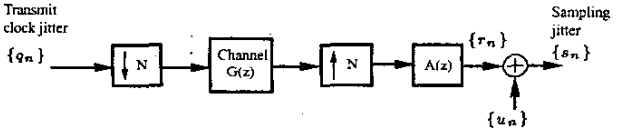

Fig. 9. Dicrete-time model to analyze the effect of transmitting a divided source-synchronous clock. The division factor is N, $G(z)$ is the channel jitter transfer function, and the filter $A(z) = \sum_{i=0}^{N-1} z^{-i}$.

4.1. Reduction of Transmit Clock Frequency

The effect of the channel on transmit jitter is a strong function of the transmit clock frequency as described in section 2 and as shown in Fig. 5. By reducing the transmit clock frequency (and performing clock multiplication at the receiver), we can mitigate jitter amplification by the channel. This benefit has to be traded off against the additional noise introduced by the clock multiplication circuitry required at the receiver. Clock multiplication can be accomplished using a PLL or DLL. A discrete-time model for a source-synchronous link transmitting a divided clock is shown in Fig. 9. Using results from multi-rate signal processing [9], the receive jitter PSD can be derived to be,

$$S_r(\omega) = \frac{1}{N^2} A(\omega)^2 G(\omega N)^2 \sum_{i=0}^{N-1} S_q(\frac{\omega N - 2\pi i}{N}) \quad (23)$$

where N is the clock division factor, $G(\omega)$ is the channel JTF, and $S_q(\omega)$ is the transmit jitter spectrum.

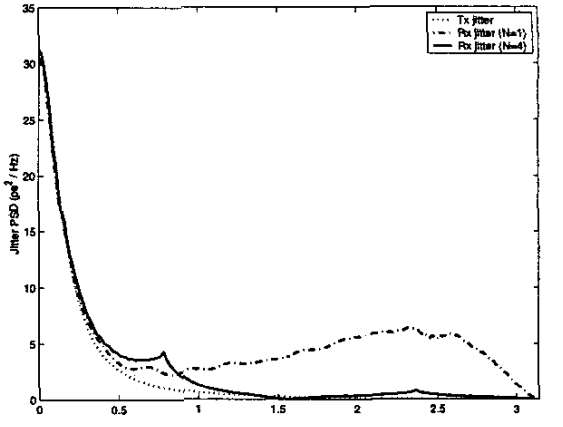

Fig. 10. Effect of transmission of a divided clock on the receive jitter PSD for a data rate of 20 Gbps. ω in the x-axis is the radian frequency. Transmitting a slower clock results in a significant reduction in the high-frequency jitter.

Fig. 10 shows the reduction of high frequency jitter due to the transmission of a divided clock. This in turn can lead to an increase in MADR, as shown in Fig. 11. The improvement is however dependent on the additional jitter introduced at the receiver due to the need for clock multiplication. If this is small (as is the case when receiver jitter is dominated by the clock distribution network), reducing the transmit clock frequency is advantageous. A 13% improvement in MADR is obtained for a 20" FR4 channel as shown in Fig. 11.

4.2. Jitter Equalization

At high data rates, typical I/O channels tend to amplify transmit clock jitter as shown in section 2. A jitter equalizer attempts to change the jitter transfer function (equation 10) to a more benign response and mitigate the effect of transmit jitter. Jitter equalizers can be realized using a PLL at the receiver instead of the conventional simpler DLL shown in Fig 2. However, a simpler realization using a phase interpolator is shown in Fig. 12. This implementation, which is the time-domain analog of a discrete-time equalizer, has the advantage of using circuits that already exist in a conventional receiver. The additional DLL serves to store jitter samples, and the interpolator mitigates high frequency jitter through averaging. While the implementation shown in Fig. 12 has

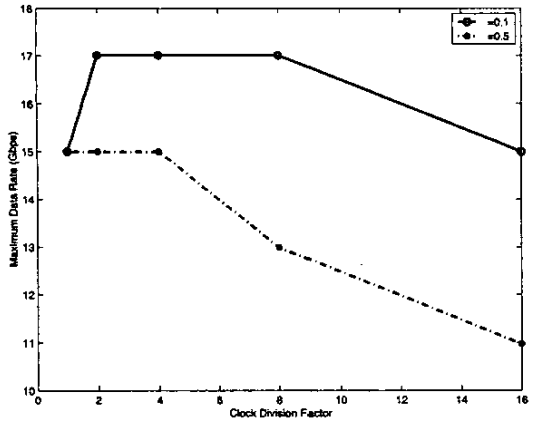

Fig. 11. Variation of maximum achievable data rate (MADR) with transmit clock division factor. ρ refers to the fraction of receiver jitter that scales with the receive clock period. The 1σ value of transmit (receiver) jitter is 0.03 UI (0.02 UI) and the transmit jitter bandwidth normalized to the data rate is 0.05.

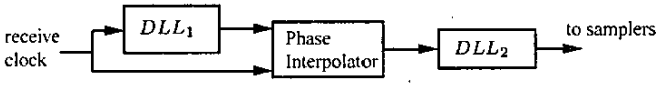

Fig. 12. Possible implementation of a jitter equalizer using an additional DLL and a phase interpolator.

a 2-tap FIR structure, extensions to a longer filter and an IIR sturcture are obvious. The improvement in MADR obtained with just a 2-tap FIR jitter equalizer for various equalizer lengths is shown in Fig. 13. As the equalizer complexity increases, jitter (rather than ISI) determines MADR, and a jitter equalizer has significant impact on MADR. The MADR when using a 9-tap linear equalizer improves by 13%, from 15 Gbps to 17 Gbps, by the use of a simple jitter equalizer.

5. CONCLUSIONS

In this paper, we presented a simple model for jitter in high-speed I/O links. We used the model to analyze the effect of the channel on clock-data jitter tracking when using source-synchronous signaling. We showed that the amplification of high-frequency jitter by the channel makes it important to consider the frequency distribution of jitter in performance analysis. We analyzed the performance of conventional equalization and modulation techniques in the presence of jitter and showed that there is significant loss in performance due to jitter. We also presented two design techniques to mitigate the effect of jitter in source-synchronous I/O links.

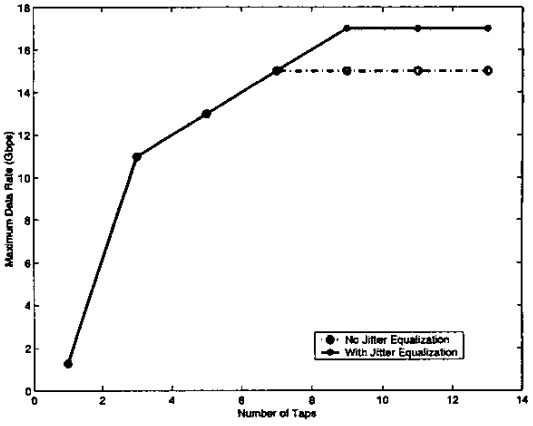

Fig. 13. Variation of maximum achievable data rate (MADR) with number of equalizer taps with and without jitter equalization. The 1σ value of transmit (receiver) jitter is 0.03 UI (0.02 UI) and the transmit jitter bandwidth normalized to the data rate is 0.05.

6. REFERENCES

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