A 0.79 pJ/K-gate, 83% Efficient Unified Core and Voltage Regulator Architecture for Sub/Near-Threshold Operation in 130nm CMOS

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Abstract

This paper presents the compute voltage regulator module (C-VRM), an architecture that embeds the information processing subsystem into the energy delivery subsystem for ultra-low power (ULP) platforms. The C-VRM employs multiple voltage domain stacking and core swapping to achieve high total system energy efficiency in near/sub-threshold region. Energy models for the C-VRM are derived, and employed in system simulations to compare the energy efficiency benefits of the C-VRM over a switched capacitor VRM (SC-VRM). A prototype IC incorporating a C-VRM and a SC-VRM supplying energy to an 8-tap fully folded FIR filter core is implemented in a $1.2\,\mathrm{V}$, $130\,\mathrm{nm}$ CMOS process. Measured results indicate that the C-VRM has up to 44.8% savings in system-level energy per operation (E_{op}) compared to the SC-VRM system, and an efficiency η ranging from 79% to 83% over an output voltage range of $0.52\,\mathrm{V}$ to $0.6\,\mathrm{V}$. Measured values of the E_{op} and η match those predicted by system simulations thereby validating the energy models.

Index Terms

Sub/Near Threshold, Low Power, Energy Efficient Digital, Voltage Regulator, VLSI Architecture

I. Introduction

The emerging applications in mobile computing, including environment surveillance, location and tracking, and healthcare monitoring, require the design of ultra low power (ULP) information processing platforms. Energy per operation (E_{op}) of such systems must be minimized through system-level design. The total system E_{op} is equal to the energy extracted from the battery per operation E_{bat} and is given by $E_{bat} = E_{op} = E_{vrm} + E_{core}$, where E_{vrm} and E_{core} are the energy consumption per instruction by the VRM and the core, respectively. The conventional approach is to design the VRM to maximize its efficiency η at a pre-specified core supply voltage V_{dd} and core/load current I_{load} (see Fig. 1).

Sub/near-threshold computing (NTC) has been proposed [1], [2] to minimize E_{core} by operating the core close to its minimum energy operating point (MEOP) where V_{dd} is regulated in the $400\,\mathrm{mV}$-to-$600\,\mathrm{mV}$ range. The battery voltage V_{bat} is typically in the range of $1.2\,\mathrm{V}$ to $3.6\,\mathrm{V}$ [3]. This large gap between V_{bat} and V_{dd} requires the voltage regulator module (VRM) to achieve a high step-down ratio. Among the VRM topologies, the switched capacitor VRM (SC-VRM) is attractive as it can achieve high conversion ratio and is amenable to on-chip integration [4], [5]. Design of high-efficiency VRM for ULP platforms is challenging due to the large step-down ratio [6], [7] and light load conditions, due to NTC.

Various approaches have been proposed to address the efficiency issue in SC-VRM under light load conditions. SC-VRM with pulse frequency modulation (PFM) control [6], [7] has been employed to boost light load efficiency up to 74%. A hybrid converter [8] has been proposed to address energy delivery for loads in the range of $5\,\mathrm{nA}$-to-$500\,\mathrm{nA}$, with efficiency up to 56%. The stacked voltage domain approach [9] has been proposed where multiple cores are connected in series to lower the step-down ratio. This approach needs push and pull linear regulators in order to compensate for voltage fluctuation in the intermediate supply nodes caused by current mismatch.

In this paper, we propose the compute VRM (C-VRM) which exploits the similarity between charge transfer in an SC-VRM and CMOS logic. Computation in CMOS occurs via transfer of

charge between supply/ground nodes and capacitive output nodes. This transfer is controlled by MOS transistor switches. Energy delivery in a SC-VRM occurs in a similar manner with power switches controlling the transfer of charge from the battery to the core. The C-VRM exploits this similarity by replacing the power switches in a SC-VRM with CMOS compute cores. In doing so, the proposed C-VRM provides the following advantages: 1) eliminates driver loss, bottom plate capacitor loss, and charge transfer loss to enhance voltage conversion efficiency, and 2) seamlessly integrates energy delivery and computation to provide a unified platform that enables the minimization of total system (VRM+core) energy E_{op}. The C-VRM does have certain disadvantages. These include increase in area and loss in throughput. These disadvantages, particularly the loss in throughput, are not critical in low throughput sensor applications. The C-VRM is similar to the stacked voltage domain approach [9], but with several key differences. Unlike [9]: 1) the C-VRM does not need linear regulators to balance the charge and thereby eliminates the additional standby loss, and 2) the efficiency of C-VRM is independent of the activity mismatch between the cores.

The C-VRM concept is validated by: a) developing energy models for the C-VRM and the SC-VRM, and employing these in system simulations to evaluate the benefits of C-VRM in energy per operation E_{op} and efficiency η, and b) implementing a prototype IC incorporating a C-VRM and a SC-VRM supplying energy to an 8-tap folded FIR filter core in a $1.2\,\mathrm{V}$, $130\,\mathrm{nm}$ CMOS process to verify the benefits of C-VRM via measured results.

The rest of the paper is organized as follows: Section II describes the background of the conventional SC-VRM and develops energy models to evaluate its efficiency. Section III presents the C-VRM and develops energy models to compare with the conventional SC-VRM. Section IV describes the prototype IC consisting of both the conventional SC-VRM system and the C-VRM. Test results in Section V demonstrate the improvement in energy and converter efficiency. Conclusions and future work are addressed in Section VI.

II. Background

This section reviews the design of a conventional SC-VRM system. An energy model is derived to reveal the fundamental loss mechanisms in a SC-VRM. A core energy model is also derived for use in system simulations in the following sections.

A. Intrinsic loss in SC-VRM

A block diagram of a 2:1 SC-VRM is shown in Fig. 2(a), where a set of charge transfer capacitors and switches are connected in different configurations in each clock phase to convert the voltage. Since the charge transfer procedure involves direct connection of voltage sources and capacitors, the current will be impulsive and lead to an intrinsic charge transfer loss E_{CTL}. As pointed out in [10], [11], E_{CTL} depends on the operational domain of the SC-VRM, i.e., complete charge, partial-charge, or no-charge. In near/sub-threshold operation with light load, driver loss will degrade light load efficiency severely and should be minimized. Thus, we assume that the SC-VRM is operating in the complete charge operation domain so as to maximize the charge transferred to the output per converter switching cycle. Figure 2(b) illustrates the source of E_{CTL} in the context of a simple 1:1 SC-VRM where the charge is transferred from V_{bat} to V_{dd} with a flying capacitor C_{sc}. In Fig. 2(b), it can be shown that in each phase ($\Phi 1$ and $\Phi 2$), the energy loss due to charge sharing is $\frac{1}{2}C_{sc}(V_{bat} - V_{dd})^2$. Thus, the intrinsic charge transfer loss during every switching cycle is:

$$E_{CTL} = C_{sc}(V_{bat} - V_{dd})^2 \tag{1}$$

Note that (1) does not depend on switch resistances $R1$ and $R2$. Therefore, E_{CTL} in (1) represents a fundamental loss mechanism in a conventional SC-VRM. The C-VRM extracts useful computation from this loss and thereby improves E_{op}.

B. SC-VRM Energy Model

In order to evaluate the converter efficiency under different load conditions, a power model for the SC-VRM is necessary. For simplicity of analysis, we choose a 2:1 ladder SC-VRM as shown in Fig. 2(a). However, the analysis method can be extended to a higher conversion ratio. There are four major loss components in the conventional SC-VRM:

1) Charge Transfer Loss (E_{CTL}): As with any SC-VRM, there is the loss E_{CTL} during each charge transfer. In [4], [12], SC-VRM is modeled as an ideal transformer (see Fig. 2(c)) representing a conversion ratio of N, and E_{CTL} is captured by a series resistance R_{ctl}, and is given by:

$$E_{CTL} = I_{core}^2 R_{ctl} T_{sw} \tag{2}$$

where I_{core} is the load current and T_{sw} is the switching period. Substituting $I_{core} = \frac{2C_{sc}\Delta V}{T_{sw}}$ and $R_{ctl} = \frac{1}{4C_{sc}f_{sw}}$ into (2), we get:

$$E_{CTL} = \frac{I_{core}^2}{4C_{sc}f_{sw}} T_{sw} = C_{sc}(\Delta V)^2 \tag{3}$$

where f_{sw} is the switching frequency of the SC-VRM, and ΔV is the difference between $\frac{V_{bat}}{N}$ (ideal output) and regulated V_{dd}. Note that (1) and (3) are identical when $\Delta V = V_{bat} - V_{dd}$.

2) Gate Drive Loss (E_{GDL}): The SC-VRM requires explicit power switches to transfer charge. A driver circuit, such as a super buffer, is therefore needed, resulting in additional losses. Assuming the gate capacitance of the power switch is C_{switch}, the gate drive loss per instruction E_{GDL} can be expressed as:

$$E_{GDL} = C_{switch} V_{bat}^2 f_{sw} / f_{clk-S} \tag{4}$$

where E_{GDL} is calculated per one core clock period $T_{clk-S} = 1/f_{clk-S}$, and f_{clk-S} is the core clock frequency. This definition of E_{GDL} allows a direct comparison with the energy consumption of the core E_{core}.

3) Bottom Plate Capacitor Loss (E_{BPCL}): The bottom plate capacitor C_{bottom} is the parasitic capacitor between the bottom plate of C_{sc} and the substrate (see Fig. 2(a)). C_{bottom} scales with the area of C_{sc} and can be as high as 5% of C_{sc} [13]. Since the bottom plate of the C_{sc} is not always grounded, during every switching cycle, C_{bottom} will be charged and discharged, as shown in Fig. 2(a). Assuming the ratio of C_{bottom} to C_{sc} is γ, this will lead to an energy loss given by:

$$E_{BPCL} = \gamma C_{sc} V_{dd}^2 f_{sw} / f_{clk-S} \tag{5}$$

4) Control Loss (E_{CL}): Control loss represents a constant loss in the SC-VRM and will degrade light load efficiency. Assuming the effective load capacitance of control circuit is C_{ctrl}, and the control circuit frequency is f_{ctrl}, the control loss can be expressed as:

$$E_{CL} = C_{ctrl} V_{bat}^2 f_{ctrl} / f_{clk-S} \tag{6}$$

C. Core Energy Model

There are two types of energy consumption in a core operating in near/sub-threshold region: dynamic energy and leakage energy. A unified model that accounts for both components has been proposed in [14]:

$$E_{core} = \alpha C_{core} V_{dd}^2 + V_{dd} I_{leak}(V_{dd}) \frac{1}{f_{clk}} \tag{7}$$

$$I_{leak}(V_{dd}) = \mu C_{ox} \frac{W}{L} (m-1) V_T^2 e^{\frac{-V_t}{mV_T}} e^{\frac{-\eta_d V_{dd}}{mV_T}} (1 - e^{\frac{-V_{dd}}{V_T}}) \tag{8}$$

where α is the core activity factor, C_{core} is the load capacitance in the core, V_{dd} is the supply voltage, V_t is the threshold voltage, V_T is the thermal voltage, μ is the carrier mobility, C_{ox} is the gate capacitance per W/L, m is a constant related with sub-threshold slope factor, and η_d is the drain induced barrier lowering (DIBL) coefficient. This model captures the trade-off between the dynamic and leakage energy, which leads to the MEOP [14], as defined via the 3-

tuple ($E^*_{core}, V^*_{dd}, f^*_{clk}$), where E^*_{core} is the energy at MEOP, V^*_{dd} is the optimum voltage, and f^*_{clk} is the energy optimum frequency. The core is modeled as a resistor R_{core} in parallel with a leakage current source $I_{leak}(V_{dd})$ (see Fig. 2(c)).

III. C-VRM SYSTEM DESIGN

This section presents the system design of the proposed C-VRM. An analytical energy model for the C-VRM is developed to compare its efficiency with the conventional SC-VRM system.

A. Principle of Operation of the C-VRM

C-VRM utilizes computational cores as switches to perform computation and transfer charge. A conceptual diagram of the C-VRM is shown in Fig. 3. The C-VRM uses compute cores as distributed power switches. Thus, the cores perform the dual functions of energy transfer and information processing.

The proposed C-VRM operates in principle the same as an interleaved SC-VRM. To illustrate this, Fig. 4 describes the operation of an interleaved 2:1 SC-VRM and a 2:1 C-VRM. For the interleaved SC-VRM, in the first phase (Φ_1), charge is stored in the flying capacitor C_1 and released by C_2; in the second phase (Φ_2), charge is released by C_1 and stored in C_2. The 2:1 C-VRM implements the same charge transfer function described above but without explicit power switches/drivers. In Φ_1, the core in the high voltage domain (CH) is clock gated while the core in low voltage domain (CL) is active. Thus, charge is stored in C_1 and released by C_2. In Φ_2 , CL is clock gated while CH is active, so that charge is released by C_1 and stored in C_2. The C-VRM achieves improved energy efficiency compared to the conventional SC-VRM as the losses associated with the driver, bottom plate capacitor, and intrinsic charge transfer are eliminated. Furthermore, it incorporates computation as an intrinsic part of its energy delivery functionality.

The out-of-phase operation of CH and CL (core swapping) requires data transfer between two voltage domains, as shown in Fig. 5. At the end of Φ_1 and Φ_2, data is transferred between CL

and CH by adding an extra core swapping cycle. The core swapping has negligible effect on total throughput, so long as the swap frequency is low compared to C-VRM core clock frequency f_{clk-C}. To ensure this condition, CH and CL employ continuous voltage and frequency scaling (CVFS), where f_{clk-C} tracks the decaying voltage (V_{CH} or V_{CL}) across the active core. The voltage of the intermediate node (V_{mid}) is permitted to vary by $80\,\mathrm{mV}$-$200\,\mathrm{mV}$. As a result, V_{CH} and V_{CL} varies between $500\,\mathrm{mV}$-to-$700\,\mathrm{mV}$, and f_{clk-C} tracks the instantaneous voltage by employing an on-chip critical path replica (CPR) oscillator.

B. C-VRM Energy Model

An energy model of the C-VRM is necessary to compare its system level energy consumption E_{op} with that of the SC-VRM system. The C-VRM eliminates driver loss and charge transfer loss associated with the conventional SC-VRM system. However, the variable core voltage results in data transfer loss and increased core energy. There are three major energy components in the C-VRM: core energy (E_{core-C}), data transfer loss (E_{DTL}), and control loss (E_{CL-C}), all of which need to be characterized.

Since the V_{dd} across each core during its operation varies, E_{core-C} is time varying, as shown in Fig. 6. Assume that M operations are completed during M clock cycles that comprise the active period. In the m^{th} ($m = 1, 2, ...M$) cycle, the average voltage across the core is denoted as $V_{dd}(m)$ and the clock period during the m^{th} operation is denoted as $T_{clk-C}(m)$. The supply voltage V_{dd} drops from a pre-defined voltage $V_{dd}(0)$ to another pre-defined voltage $V_{dd}(M)$ over M clock cycles, as shown in Fig. 6. In the test chip, $V_{dd}(0)$ and $V_{dd}(M)$ are chosen to be 500 mV and 700mV, respectively, and the value of M ranges from 96 to 131 depending on the core activity factor α. We also assume that CH and CL see the same voltage profile ($V_{dd}(m)$) during active periods in order to simplify the analysis. Thus, E_{core-C}, E_{DTL}, and E_{CL-C} can be calculated as

$$E_{core-C} = \frac{1}{M}\sum_{m=1}^{M}[\alpha C_{core}V_{dd}^2(m) + I_{leak}(m)V_{dd}(m)]T_{clk-C}(m) \tag{9}$$

$$E_{DTL} = \frac{C_{reg-C}V_{bat}^2}{M} \tag{10}$$

$$E_{CL-C} = \frac{C_{ctrl-C}V_{bat}^2 f_{ctrl-C}}{f_{clk-C}} \tag{11}$$

where α is the core activity factor, $I_{leak}(m)$ is the leakage current at the supply voltage of $V_{dd}(m)$, C_{reg-C} is the total load capacitance of data transfer logic, C_{ctrl-C} is the load capacitance of the control circuitry, f_{ctrl-C} is the equivalent control frequency, and f_{clk-C} is the core clock frequency. Figure 7 shows a C-VRM with N cores (thus N voltage domains). From the principle of charge conservation, the following set of equations hold:

$$Q = \alpha C_{core}V_{dd}(m) \tag{12}$$

$$Q\frac{N-1}{N} = \frac{C_{sc}}{N}V_{dd}(m-1) - \frac{C_{sc}}{N}V_{dd}(m) \tag{13}$$

where (12) describes the charge consumed by the core in the m^{th} clock cycle, and (13) describes the charge conservation at node **a** in Fig. 7. Equation (12) and (13) can be used to solve for $V_{dd}(m)$ ($m = 1..., M$) to obtain:

$$V_{dd}(m) = [\frac{C_{sc}}{(N-1)\alpha C_{core} + C_{sc}}]^m V_{dd}(0) \tag{14}$$

Next, substituting $m = M$ in (14), we solve for M as follows:

$$M = \frac{\ln\frac{V_{dd}(M)}{V_{dd}(0)}}{\ln[\frac{C_{sc}}{(N-1)C_{core}+C_{sc}}]} \tag{15}$$

The clock period $T_{clk-C}(m)$ is obtained as the average of the critical path delays at $V_{dd}(m)$

($T_d(V_{dd}(m))$) and $V_{dd}(m-1)$ ($T_d(V_{dd}(m-1))$):

$$T_{clk-C}(m) = \frac{T_d(V_{dd}(m)) + T_d(V_{dd}(m-1))}{2} \tag{16}$$

Therefore, the E_{op} of the conventional SC-VRM system is given by:

$$E_{op-SC} = E_{core} + E_{CTL} + E_{GDL} + E_{BPCL} + E_{CL} \tag{17}$$

where E_{core}, E_{GDL}, E_{BPCL}, and E_{CL} are defined in (2)-(7). Similarly, the E_{op} of the C-VRM is obtained as:

$$E_{op-C} = E_{core-C} + E_{DTL} + E_{CL-C} \tag{18}$$

where E_{core-C}, E_{DTL}, and E_{CL-C} are defined in (9)-(11), and V_{dd}, M and $T_{C,CLK}$ are obtained from (14)-(16). Measured results from a prototype test chip in $130\,\mathrm{nm}$ CMOS (See Fig. 22) indicate that (17) and (18) accurately models the energy consumption of the SC-VRM and the C-VRM, respectively. Energy saving can be obtained if $E_{op-C} < E_{op-SC}$. Next, we determine conditions under which the C-VRM is more energy efficient, as compared to an SC-VRM system.

C. C-VRM System Design

In the rest of this paper, we will assume that the C-VRM has $N = 2$ cores to simplify the analysis. System simulations are performed to compare the energy efficiencies of the C-VRM and the SC-VRM system. The battery voltage V_{bat} is assumed to be $1.2\,\mathrm{V}$. For the SC-VRM, we use an $N = 2$ ladder topology as shown in Fig. 2(a), with flying capacitor C_{sc} chosen to be $500\,\mathrm{pF}$. C_{switch} is chosen such that the SC-VRM is operating in slow switching limit (SSL) and fast switching limit (FSL) boundary to balance shunt and series losses. The bottom plate capacitance C_{bottom} is assumed to be 2% of C_{sc} and C_{ctrl} is assumed to be 1% of C_{sc}. For the C-VRM, we also choose

the $N = 2$ topology as shown in Fig. 4. For fairness of comparison, we constrain the total charge transfer capacitance ($C_1 + C_2$) in the C-VRM to equal C_{sc} in the SC-VRM. The $500\,\mathrm{pF}$ capacitor is split equally between C_1 and C_2. Each $250\,\mathrm{pF}$ capacitance supplies one of the cores. We also keep the control loss of the C-VRM the same as the SC-VRM. We assume the same $100\,\mathrm{pF}$ C_{core} for both the SC-VRM system and the C-VRM. The average activity factor α is assumed to be 0.3. The switching frequency f_{sw} is swept to generate V_{dd} in the range of $0.42\,\mathrm{V}$ to $0.6\,\mathrm{V}$. Energy losses and core energy are calculated via the energy model developed in previous sections.

To compare energy efficiency of the SC-VRM and C-VRM, we define the effective V_{dd} ($V_{dd,eff}$) as the V_{dd} under which the MAC core in the SC-VRM will give the same throughput as the MAC core in the C-VRM, i.e., the SC-VRM clock period $T_{clk-S}(V_{dd,eff})$ equals the average C-VRM clock period:

$$T_{clk-S}\left(V_{dd,eff}\right) = \frac{1}{M}\sum_{i=1}^{M} T_{clk-C}\left(i\right) \tag{19}$$

where $T_{clk-C}(i)$ is the C-VRM clock period in the i^{th} cycle. Substituting (15), (16) into (19) for N = 2, we obtain:

$$T_{clk-S}\left(V_{dd,eff}\right) = \frac{ln[\frac{C_{sc}}{C_{core}+C_{sc}}]}{ln\frac{V_{dd}(M)}{V_{dd}(0)}} \sum_{i=1}^{M} \frac{T_d(V_{dd}\left(i\right)) + T_d\left(V_{dd}\left(i-1\right)\right)}{2} \tag{20}$$

Substituting (14) into (20), we obtain the relation between $V_{dd,eff}$ and $V_{dd}(0)$ and $V_{dd}(M)$ as follows:

$$T_{clk-S}\left(V_{dd,eff}\right) = \frac{ln[\frac{C_{sc}}{C_{core}+C_{sc}}]}{ln\frac{V_{dd}(M)}{V_{dd}(0)}} \sum_{i=1}^{M} \frac{T_d(\left[\frac{C_{sc}}{\alpha C_{core}+C_{sc}}\right]^{i} V_{dd}(0)) + T_d\left(\left[\frac{C_{sc}}{\alpha C_{core}+C_{sc}}\right]^{i-1} V_{dd}(0)\right)}{2} \tag{21}$$

Under the assumption that CH and CL see the same voltage profile $V_{dd}(m)$ during their active

periods, we can substitute $\frac{V_{bat}}{2}+\Delta V$ and $\frac{V_{bat}}{2}-\Delta V$ into (21) to obtain:

$$T_{clk-S}\left(V_{dd,eff}\right)=\frac{ln[\frac{C_{sc}}{C_{core}+C_{sc}}]}{ln\frac{\frac{V_{bat}}{2}-\Delta V}{\frac{V_{bat}}{2}+\Delta V}}\sum_{i=1}^{M}\frac{T_d(\left[\frac{C_{sc}}{\alpha C_{core}+C_{sc}}\right]^{i}(\frac{V_{bat}}{2}+\Delta V))+T_d\left(\left[\frac{C_{sc}}{\alpha C_{core}+C_{sc}}\right]^{i-1}(\frac{V_{bat}}{2}+\Delta V)\right)}{2}$$

For near threshold operation, it is difficult to obtain a precise analytical expression for this delay. Simulation results were used to extract the delay vs. V_{dd} curve of the critical path and $V_{dd,eff}$ can be solved numerically for different values of ΔV. Figure 8 shows that while the actual voltage range might go beyond $V_{bat}/2$ ($0.6\,\mathrm{V}$ in the simulation), the effective voltage is less than the ideal output voltage $V_{bat}/2$.

In the first experiment, we assume C_{reg-C} is only 1% of C_{core} so that the data transfer overhead is small. Figure 9(a) shows the different energy components for the conventional SC-VRM as a function of V_{dd}. We denote $E_{SHUNT}=E_{GDL}+E_{BPCL}+E_{CL}$ since driver loss, bottom capacitance loss and control loss can all be denoted as parallel equivalent resistors in Fig. 2(c). From Fig. 9(a), we can see that as V_{dd} increases, E_{CTL} increases due to reduced ΔV according to (3); but E_{SHUNT} increases due to increased f_{sw}. In super threshold region, as V_{dd} decreases, E_{core} decreases because dynamic energy dominates. As V_{dd} further decreases to sub/near-threshold region, E_{core} increases due to the exponential increase of propagation delay. Due to the trade-off between E_{SHUNT}, E_{CTL} and E_{core}, the system MEOP (S-MEOP) voltage $V^{*}_{dd,S-MEOP}$ is around $0.46\,\mathrm{V}$. The E_{op} increases as the V_{dd} deviates from $V^{*}_{dd,S-MEOP}$.

Figure 9(b) shows the different energy components of the C-VRM as a function of V_{dd}, where E_{DTL} and E_{CL-C} are lumped together as E_{LOSS} for simplicity. The V_{dd} value for the C-VRM is the $V_{dd,eff}$ defined in (19). Figure 9(b) illustrates that compared with the conventional SC-VRM system, the C-VRM has a higher E_{core} due to its variable voltage operation. However, the C-VRM eliminates E_{GDL}, E_{BPCL} and E_{CTL} associated with the SC-VRM system. Furthermore, Fig. 9(b) indicates that E_{LOSS} becomes higher when V_{dd} is close to the ideal output ($\frac{1}{2}V_{bat}=0.6\,\mathrm{V}$) due to

the increased data transfer frequency. E_{LOSS} also increases as the core enters sub-threshold region due to increased delay.

Figure 9(c) compares the E_{op-SC} and E_{op-C}, as defined in (17) and (18), and shows that the C-VRM has lower E_{op} compared with the SC-VRM system across the entire operating point from $0.42\,\mathrm{V}$ to $0.6\,\mathrm{V}$. Large energy savings can be achieved either at high V_{dd} (close to ideal output of $0.6\,\mathrm{V}$) due to the elimination of E_{GDL} and E_{BPCL}, or when V_{dd} is further reduced beyond $V^*_{dd,S-MEOP}$ of $0.46\,\mathrm{V}$ due to the elimination of E_{CTL}.

Figure 9(d) shows the efficiency comparison of the SC-VRM system and the C-VRM. This figure illustrates that the C-VRM can maintain high efficiency ($\eta_{C-VRM} > 93\%$) across the operating range from $0.42\,\mathrm{V}$ to $0.6\,\mathrm{V}$, while the SC-VRM can only achieve $\eta_{SC-VRM} \approx 80\%$ at around $0.54\,\mathrm{V}$. As V_{dd} deviates from this efficiency maximum voltage, η_{SC-VRM} drops quickly due to increased E_{SHUNT} or E_{CTL}.

The energy benefit of the C-VRM depends on the assumption that the data transfer loss E_{DTL} is small. This assumption holds if the core swapping frequency f_{swap} is small compared to f_{clk-C}, and C_{reg-C} is small. To illustrate this point, we perform the same set of experiments as in Fig. 9 but with C_{reg-C} is increased to 10% of C_{core}. Figure 10 shows the resulting E_{op} and η. Figure 10(a) shows that when E_{DTL} is large, it is possible that the $E_{op-C} > E_{op-SC}$. However, energy savings are preserved when V_{dd} is close to the ideal output of $\frac{1}{2}V_{bat} = 0.6\,\mathrm{V}$ or when V_{dd} is in far below $V^*_{dd,S-MEOP}$ in sub-threshold. Figure 10(b) shows that when E_{DTL} is large, η_{C-VRM} decreases dramatically when V_{dd} increases due to the increased core swapping frequency. Therefore, to achieve maximum energy savings, E_{DTL} of the C-VRM needs to be kept to a minimum.

IV. C-VRM Prototype IC Design

A prototype IC was designed in a $1.2\,\mathrm{V}$, $130\,\mathrm{nm}$ CMOS process to compare the SC-VRM system and the C-VRM. This section describes the prototype IC.

A. Chip Architecture

To enable a direct comparison between the SC-VRM system and the C-VRM, we fix the charge transfer capacitor (C_{sc} in Fig. 2(a) and $C_1 + C_2$ Fig. 5) to $250\,\mathrm{pF}$ and employ an 8-bit multiply-accumulator (MAC) as the core in both systems. The SC-VRM system and the C-VRM are optimized to supply an I_{core} up to $1\,\mathrm{mA}$ at a nominal V_{dd} of $500\,\mathrm{mV}$. To reduce E_{DTL}, a folded MAC architecture is adopted.

Figure 11 shows the top level chip architecture. The chip consists of a 2:1 SC-VRM system, a 2:1 C-VRM and a test block. The 2:1 SC-VRM system consists of a ladder SC-VRM delivering energy to a core. The core is a MAC with an 8 bit array multiplier and a ripple carry adder. It is configured as an 8-tap folded FIR filter. The 2:1 C-VRM consists of cores MAC_H and MAC_L, which are identical to the core in the 2:1 SC-VRM system. A CPR oscillator with tunable delay is designed to continuously scale the core frequency f_{clk-C} with V_{dd}. The test block consists of a vector generator to feed input data to the cores and level shifters to transfer output data for off-chip processing.

B. SC-VRM Design

Figure 12 shows the detailed architecture of the 2:1 SC-VRM, which has a ladder topology containing four power switches and one $250\,\mathrm{pF}$ on-chip MIM flying capacitor C_{sc}. C_{sc} is chosen to supply maximum I_{core} of $1\,\mathrm{mA}$ with maximum f_{sw} of $10\,\mathrm{MHz}$. The transistor M1 and M2 are chosen to be PMOS and NMOS, respectively, to remove the threshold voltage drop. M3 and M4 are chosen to be NMOS because the regulated output V_{dd} is always lower than $\frac{1}{2}V_{bat}$. The power switches are sized to balance shunt and series loss according to [4], [15]. Figure 12 also shows the control loop of the SC-VRM. A hysteresis PFM control [16] is realized via a strong ARM comparator and a current starved oscillator. The output of the oscillator is passed through the driver circuitry and converted to non-overlapping two phase clock signals.

Figure 13 shows the circuit diagram of the strong ARM comparator and the current starved

oscillator. We adopt the dynamic comparator to avoid steady state current, which degrades light load efficiency. In the pre-charge phase, MP1-MP4 pre-charges the output node and the drain of MN3 and MN4 to V_{dd}. In the evaluation phase, the drain of MN3 and MN4 are discharged at different rates according to input V_{ip} and V_{in}, respectively. If V_{ip} is higher than V_{in}, MN1 will turn on prior to MN2, and the positive feedback formed by MN1, MN2, MP5 and MP6 will discharge V_{on} and charge V_{op} back to V_{dd}. The pre-charge transistors are kept minimum size to reduce the load capacitance. The input pair and cross coupled inverter MN1, MN2, MP5 and MP6 are sized to trade off speed and offset. The current starved oscillator contains mirror transistor MN1-MN3 and MP1-MP3. Transistor MN4-MN6 and MP4-MP6 form a 3 stage ring oscillator. They are sized to minimize the power consumption while providing sufficient driver speed.

Figure 14 shows the non-overlapping circuit with an embedded driver. The complementary clock signal is fed into a cross coupled NOR gate to add dead time, t_p, between $\Phi 1$ and $\Phi 2$. The t_p is adjusted by changing the number of the buffer chain stages. A super buffer is added at the end of the buffer chain to drive the power switches.

C. C-VRM Design

Figure 15 shows the design of the C-VRM. The 2:1 C-VRM contains MAC_H and MAC_L as the two compute cores, level shifters (LS) for data transfer, and a control block to switch the compute cores from active to inactive modes.

Figure 16(a) shows the circuit diagram of the control block. The shaded blocks operate in the low voltage domain , while the unshaded blocks operate in the high voltage domain. The control block consists of an RC delay based frequency detector, a latch and a pulse generator for core swapping. Figure 16(b) shows the operation of the frequency detection block. During the pre-charge phase, C_2 is connected to V_{mid}; during the evaluation phase, C_2 is discharged through the RC circuit formed by R_2 and C_2, with discharging time determined by $\frac{1}{2f_{clk}}$. If during this period, V_a drops below the threshold, V_b will rise to V_{mid} and state of the latch (**ENl**) will be set to 0, disabling MAC_L. The

pulse generator is realized via NOR **ENl** and a delayed version of the signal, so that during the 1-0 transition of **ENl**, a pulse is generated. The pulse will force the state of latch in high voltage domain (**ENh**) to be 1 through the pull down transistor M1, thus enabling MAC_H by turning **ENh** to 1.

Figure 17 shows the level shifter used in the C-VRM. The level shifter will perform bidirectional transfer of the data between MAC_H and MAC_L. The conventional level shifter design shown in Fig. 17(a) is not suitable for two reasons: 1) two different circuit topologies are needed to perform high-to-low and low-to-high level conversion, respectively, and 2) there are direct paths current through MN1, MP1 or MN2, MP2 during shift. Both of these will result in additional E_{DTL} in (18). Therefore, we adopt a capacitor coupling based dynamic level shifter in Fig. 17(b). Figure 17(b) also shows the operation during high-to-low data transfer. In the pre-charge phase, the capacitor C_{ls} is pre-charged to V_{mid}. When MAC_H is disabled by changing **ENh** from 1 to 0, a one clock cycle pulse **shift_hl** is inserted before **ENl** goes high. This will turn on the transmission gate and shift *data_h* from MAC_H to MAC_L. After the shift operation, C_{ls} is charged to V_{mid} before the next operation. The dynamic level shifter achieves bidirectional shifting and removes the direct path loss associated with the conventional design.

D. CPR Oscillator

The CPR oscillator we employed in this paper is similar to the one used in [17], which is an inverter chain based ring oscillator with tunable delay cells (See Fig. 18(a)). A chain of inverters are used instead of a direct mapping of the core critical path components to provide a near-50% duty cycle clock. The number of inverters is calculated based on a first-order approximation using the Elmore delay formula for a resistor-capacitor network. In this design, 68 inverters are used to replicate the critical path. To account for PVT variation, a tuning circuit is added to adjust the delay margin provided by the CPR oscillator to ensure the clock period is greater than the actual critical path. A digital control is chosen over voltage control for simplicity and reliable bias in different

voltage domains. Figure 18(b) shows the detail of the inverter delay cell. Each delay cell consists of a long path and a short path, the selection of the paths is controlled by MUX. Each delay cell uses a single-bit control to minimize the capacitive loading at the output of the delay cell. In the design, 4 delay cells are added to provide tuning range of 16 inverter delays.

Figure 19(a) shows the post layout simulation of MAC unit critical path delay and the CPR oscillator clock period in different process corners. It can be seen that the CPR oscillator is able to track the MAC unit critical path and ensure that the clock period is larger than the MAC unit critical path delay across all process corners. Figure 19(b) shows the CPR oscillator clock period with different tuning settings. The 8 delay cells provide sufficient large tuning range to account for the delay variations.

V. Test Results

Figure 20 shows the operation of the SC-VRM during start up and steady state. During steady state, PFM control is employed to scale the switching frequency f_{sw} with I_{core} to reduce the driver and bottom plate capacitance loss.

Figure 21 shows the operation of the C-VRM including core swapping and data transfer. The startup circuitry for the C-VRM is implemented on the board. When the MAC core voltage in one voltage domain decreases to $500\,\mathrm{mV}$, core swapping is performed by employing the on-chip generated enable signal **ENh** and **ENl** for MAC_H and MAC_L, respectively. During data transfer, when MAC_L is enabled by **ENl,** a one cycle switching signal **sw_h2l** is generated to shift data from the high voltage to the low voltage domain.

Figure 22 compares the measured E_{op} and the efficiency of the fabricated 2:1 SC-VRM system and the 2:1 C-VRM. The simulated results according to the energy model in Section III are also shown as dashed lines to demonstrate the accuracy of the model in Section III. The efficiency vs. V_{dd} is obtained by changing the reference voltage for the SC-VRM, and by changing the RC time constant of the frequency detector in the C-VRM controller. To perform efficiency measurements

for the C-VRM, the compute core in the C-VRM, and the controller and level shifter of the C-VRM are provided separate supply pins, which allows the loss (control loss and data transfer loss) current I_{loss} and the core current I_o to be measured. The efficiency is then calculated using $\eta = I_o/(I_o + I_{loss})$. As shown in Fig. 22(a), the C-VRM has lower E_{op} across all measured V_{dd} from $0.52\,\mathrm{V}$ to $0.59\,\mathrm{V}$. Since C-VRM has a continuously varying voltage, the V_{dd} is the effective output voltage delivering the same throughput ($11\,\mathrm{MHz}$-to-$20\,\mathrm{MHz}$) as the SC-VRM system. V_{dd} of C-VRM cannot extend below $0.52\,\mathrm{V}$ due to the limitations of the capacitively coupled level shifter. The SC-VRM system has high system energy overhead both in high V_{dd}, due to increased driver loss E_{GDL}, and in low V_{dd}, due to control loss E_{CL} and low f_{clk-C}. This is also indicated by the system level simulations in Fig. 9(a). The absence of the driver circuits and the use of a low power frequency detection scheme enables the C-VRM to achieve a maximum of 44.8% energy savings compared to the SC-VRM system. Figure 22(b) shows that the C-VRM achieves efficiency $> 79\%$ across the entire tested V_{dd} range. As a comparison, the SC-VRM has a peak efficiency of only 54% due to E_{SHUNT} and E_{CTL}. Figure 22(b) also plots the efficiency of previously published SC-VRM designs operating at power levels of $1\mu W$-100s of μW range from [2], [8], [18].

Table I shows the design specifications and performance of C-VRM compared with previously published works. The system energy per instruction/K-gate is calculated by dividing the system EPI by the estimated number of gates for [1] and [2]. For [7] and [8], since no compute cores are included on-chip, the system energy per instruction/K-gate is estimated using the core EPI and gate count of our design and the efficiency reported in [7] and [8]. The comparison in Fig. 22(b) and in Table I shows that the C-VRM achieves the highest efficiency (83%) in the designed power level and the lowest EPI/k-gate of $0.79\,\mathrm{pJ}$.

Figure 23 shows the die photo of the test chip. The test chip is fabricated in a $1.2\,\mathrm{V}$, $130\,\mathrm{nm}$ CMOS process and has an area of $2\,\mathrm{mm} \times 2\,\mathrm{mm}$, including the pad frame. Note that the SC-VRM requires $2\,\mathrm{nF}$ off-chip decoupling capacitor. This capacitor, if integrated on-chip, will present as large as $0.49\,\mathrm{mm}^2$ additional area to the SC-VRM system.

VI. Conclusion and Future Work

In this paper, we propose the C-VRM, a unified architecture for energy delivery and computation, to overcome the intrinsic loss and drive circuit overhead of the conventional SC-VRM. The C-VRM employs multiple voltage domain stacking, core swapping, and CVFS to achieve high energy efficiency in sub/near-threshold region. A test chip consisting of a conventional SC-VRM system and a C-VRM is fabricated in a $130\,\mathrm{nm}$ CMOS process.

This work shows that by combining the compute core and the energy delivery block, the system energy efficiency can be significantly improved. It opens the possibilities of embedding more sophisticated computational blocks into SC-VRM and other switching power delivery blocks. Further study is necessary to develop C-VRM architectures based on multi-ratio SC-VRM or multi-phase SC-VRM. This work also opens the possibility of incorporating an error-resilient core [17], [19] into the VRM to further enhance energy efficiency.

Acknowledgment

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CAPTIONS OF FIGURES AND TABLES

Figure 1: Conventional design approach addresses VRM design and core design separately. Due to the tradeoff between dynamic and leakage energy, minimum energy operation point (MEOP) of compute cores usually lie in near or sub-threshold regime. However, the resulting high conversion ratio often results in poor VRM efficiency.

Figure 2: Conventional SC-VRM architecture: (a) block diagram of a 2:1 SC-VRM, (b) charge sharing loss mechanism, and (c) a simplified energy transfer model.

Figure 3: Conceptual block diagram of the C-VRM with $N = 2$ compute switches.

Figure 4: The C-VRM principle for $N = 2$.

Figure 5: Data transfer in the C-VRM during core swapping.

Figure 6: The variable supply voltage $V_{dd}(m)$ results in a time varying clock period $T_{clk-C}(m)$.

Figure 7: The principle of charge conservation in the C-VRM.

Figure 8: The effective voltage $V_{dd,eff}$ as a function of $\Delta V = V_{bat}/2 - V_{dd}(M)$.

Figure 9: Comparison of SC-VRM system and C-VRM with 1% data transfer overhead: (a) energy vs. output V_{dd} of SC-VRM, (b) energy vs. V_{dd} of C-VRM, (c) E_{op} comparison of SC-VRM and C-VRM, and (d) efficiency comparison of SC-VRM and C-VRM.

Figure 10: System comparison between SC-VRM system and C-VRM with 10% data transfer overhead: (a) E_{op} comparison of SC-VRM and C-VRM, and (b) efficiency comparison of SC-VRM and C-VRM.

Figure 11: The C-VRM prototype IC architecture.

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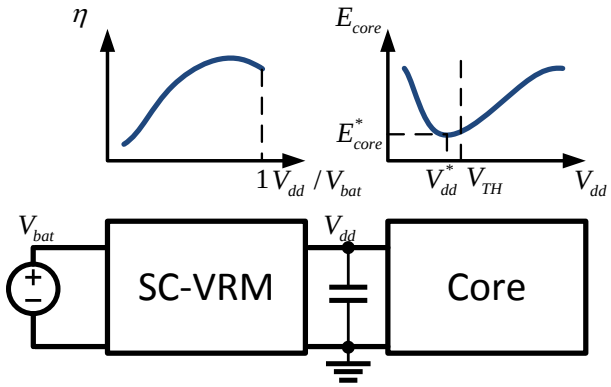
Figure 16: Control block of the C-VRM: a) circuit schematic, and b) principle of operation.



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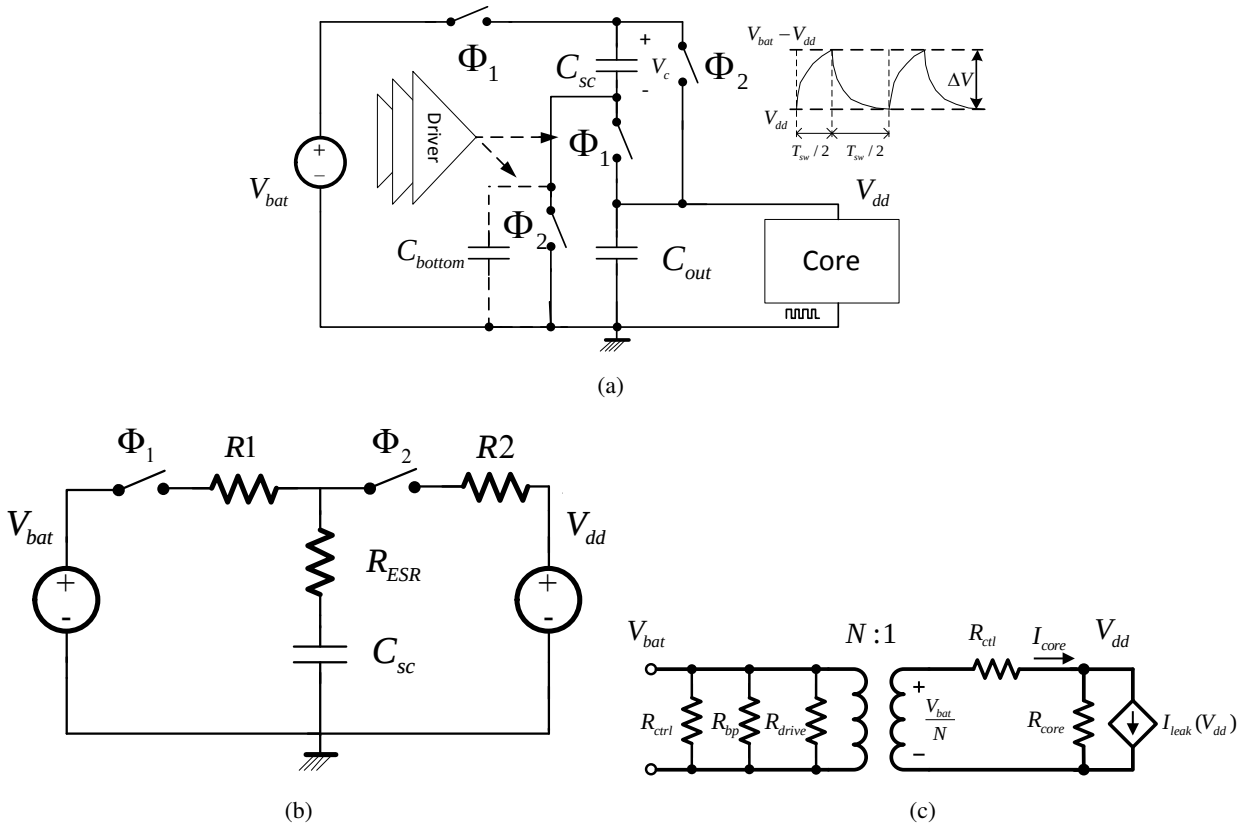

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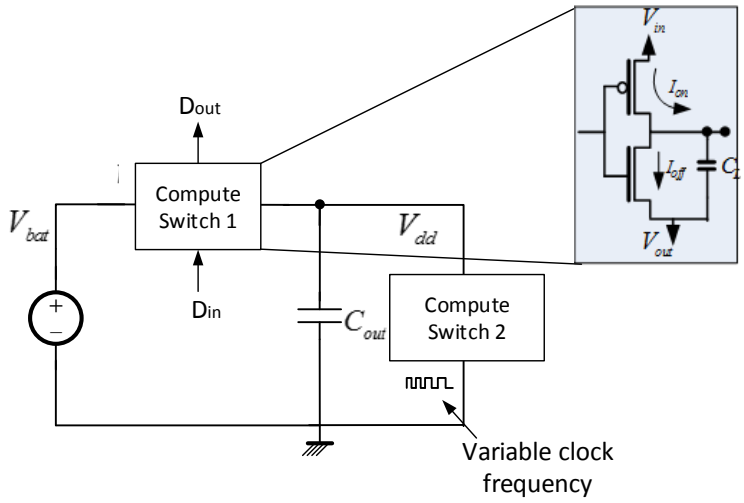

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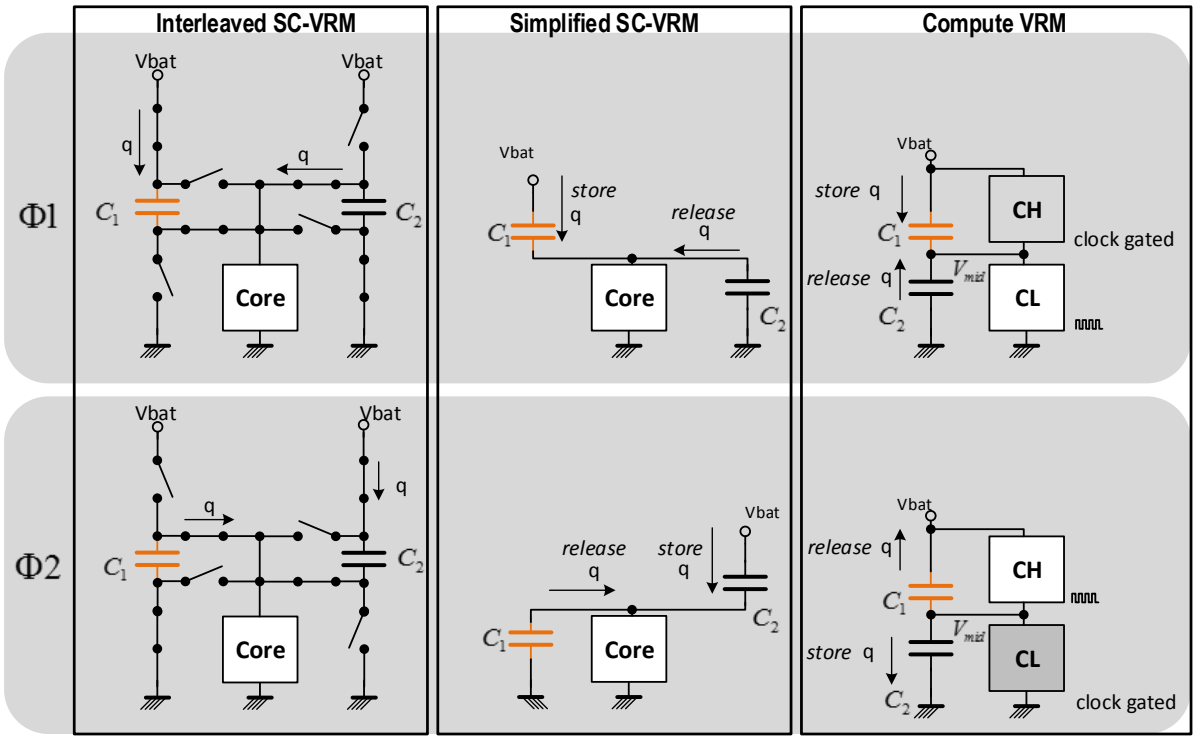


Fig. 4. The C-VRM principle for $N = 2$.

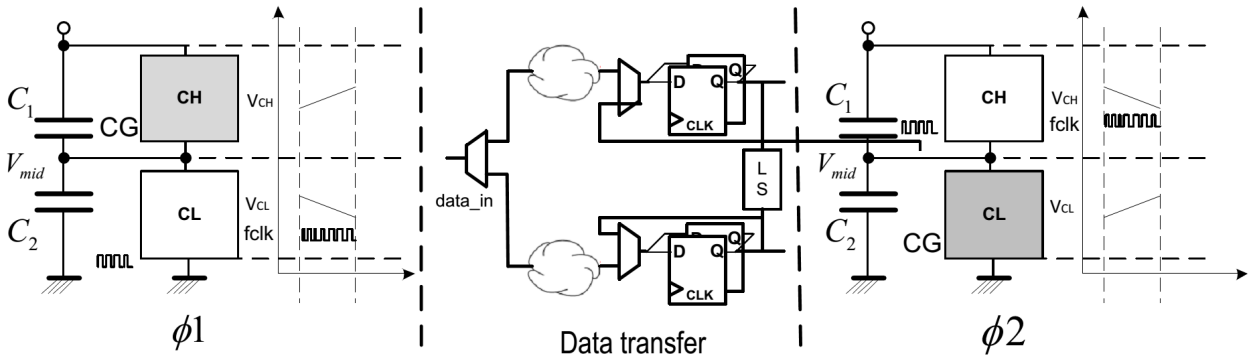
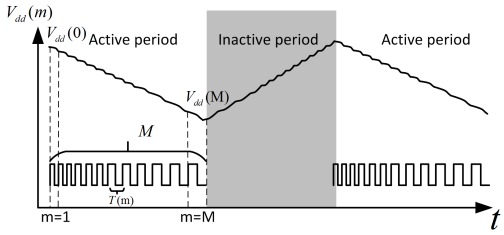


Fig. 5. Data transfer in the C-VRM during core swapping.



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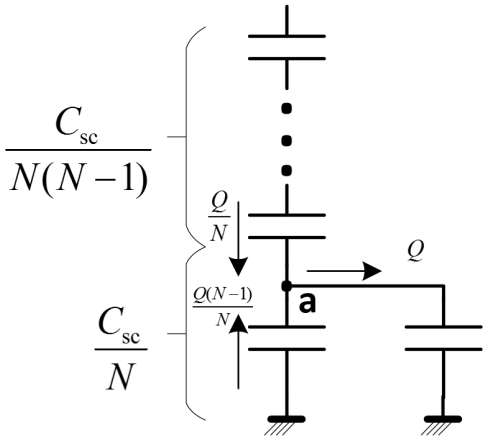

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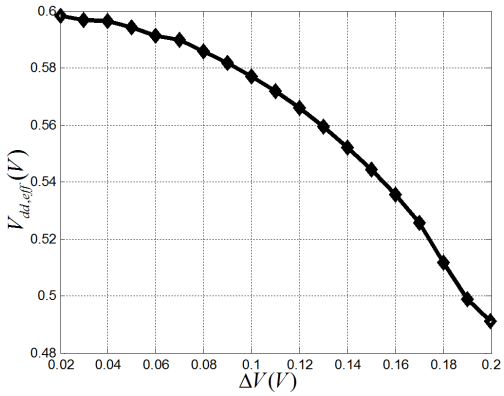

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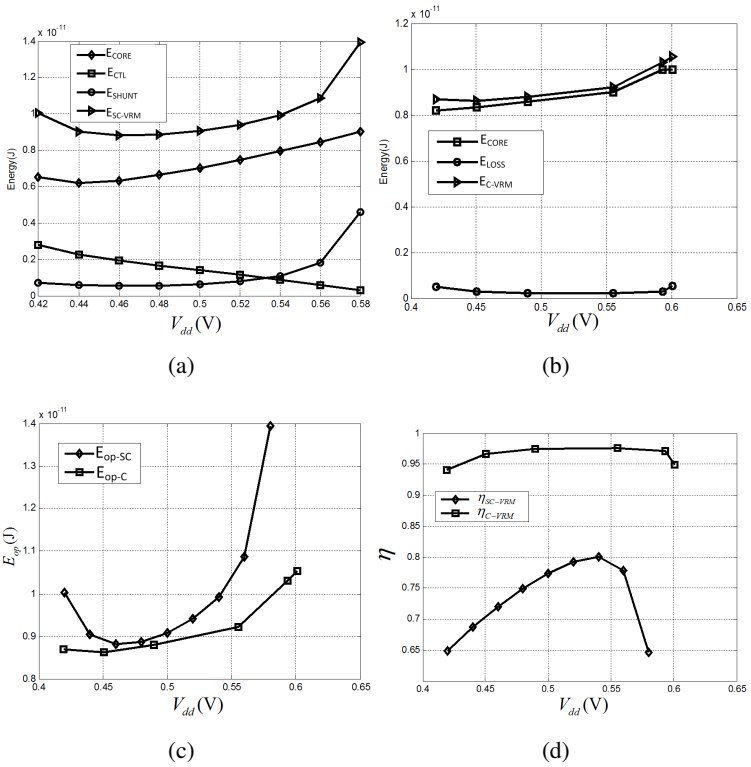

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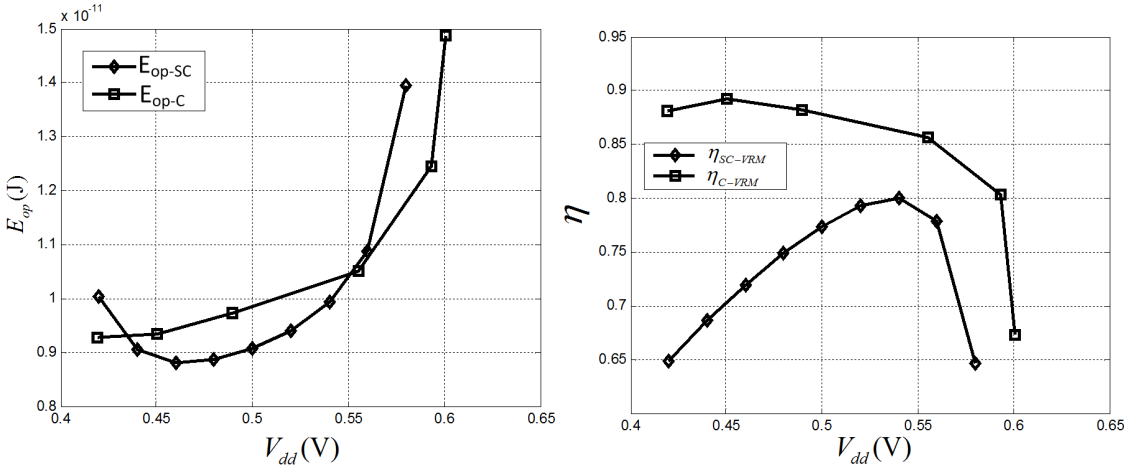
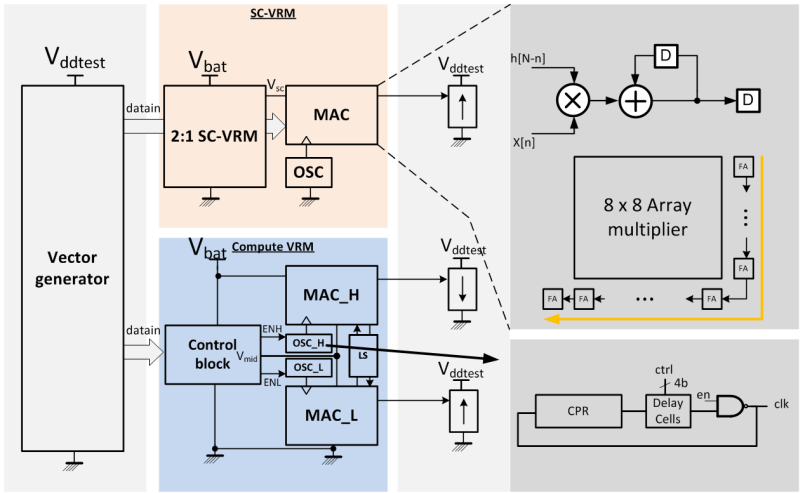


(a) (b)

Fig. 10. System comparison between SC-VRM system and C-VRM with 10% data transfer overhead: (a) E_{op} comparison of SC-VRM and C-VRM, and (b) efficiency comparison of SC-VRM and C-VRM.



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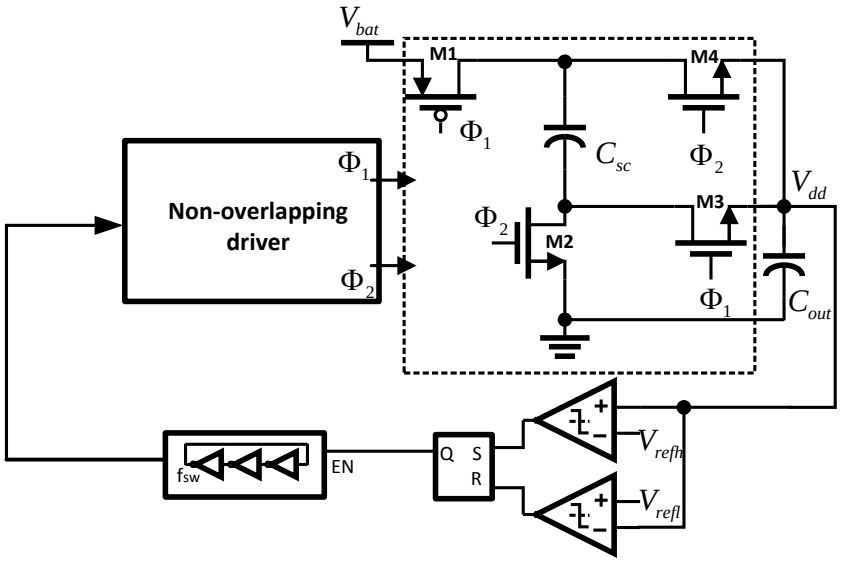
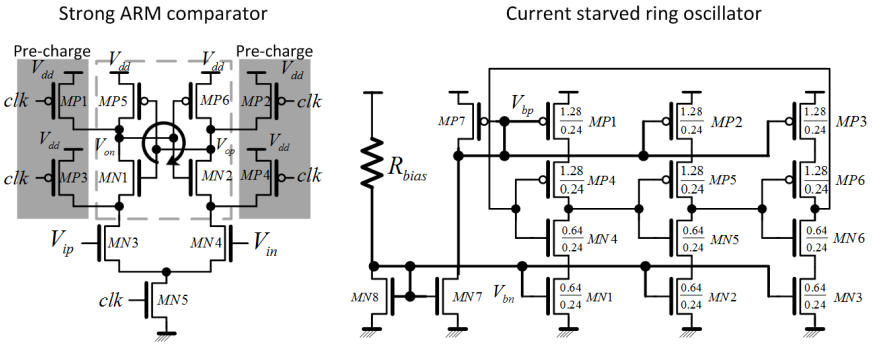


C_{sc}	250 pF
M1	100 µ/0.12 µ
M2	50 µ/0.12 µ
M3	100 µ/0.12 µ
M4	100 µ/0.12 µ

Fig. 12. The 2:1 ladder SC-VRM.



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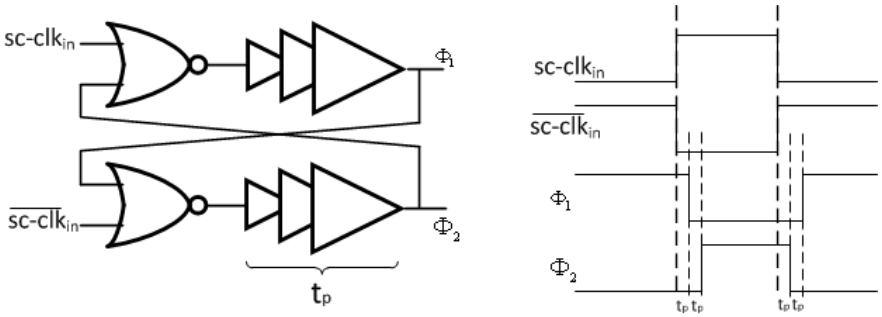
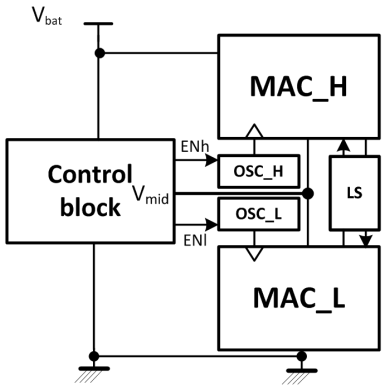


Fig. 14. Non-overlapping driver employed in the 2:1 SC-VRM.



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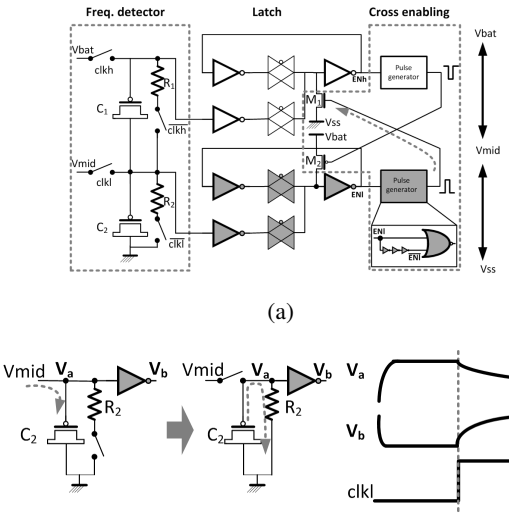

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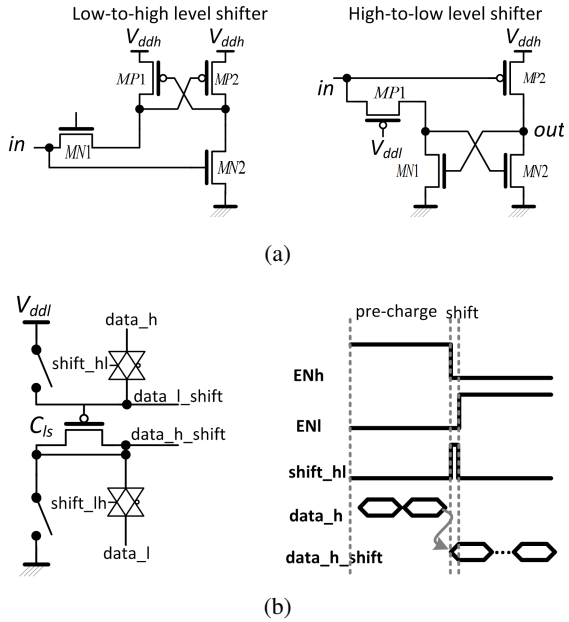


Fig. 17. Bidirectional level shifter: a) conventional design of low-to-high and high-to-low level shifters, and b) the proposed capacitor coupling based dynamic level shifter.

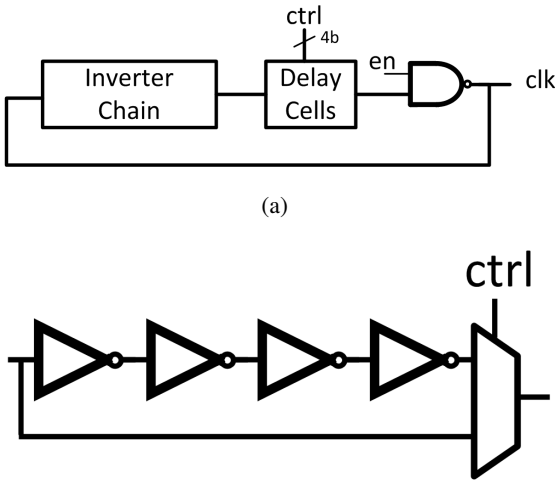


Fig. 18. Architecture of: a) the CPR oscillator, and b) the tunable delay cell.

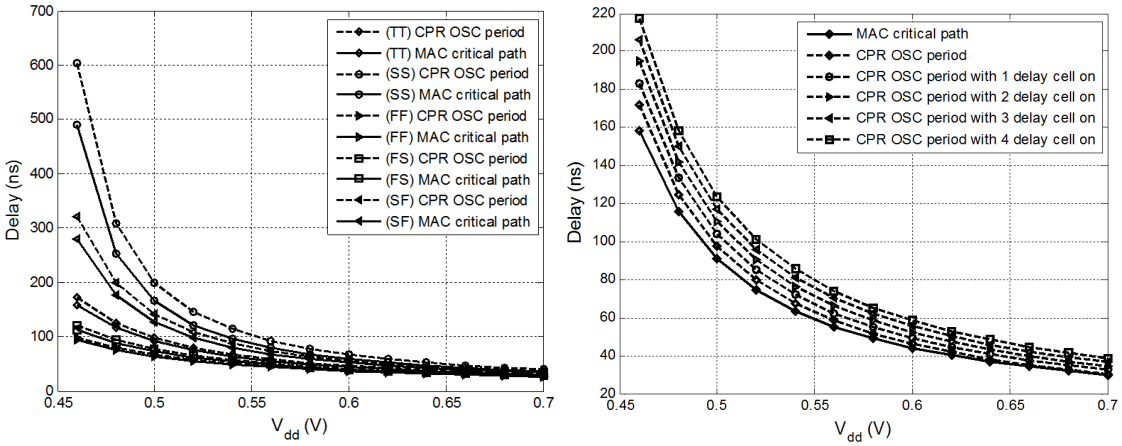


Fig. 19. Post layout simulations showing: a) the CPR oscillator clock period and MAC critical path delay, and b) the CPR oscillator clock period with different delay cells selected.

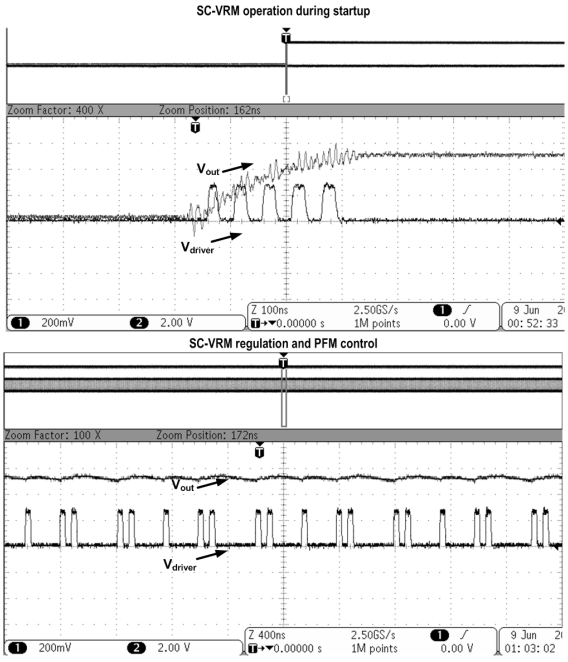


Fig. 20. Measured SC-VRM operation during start up and steady state.

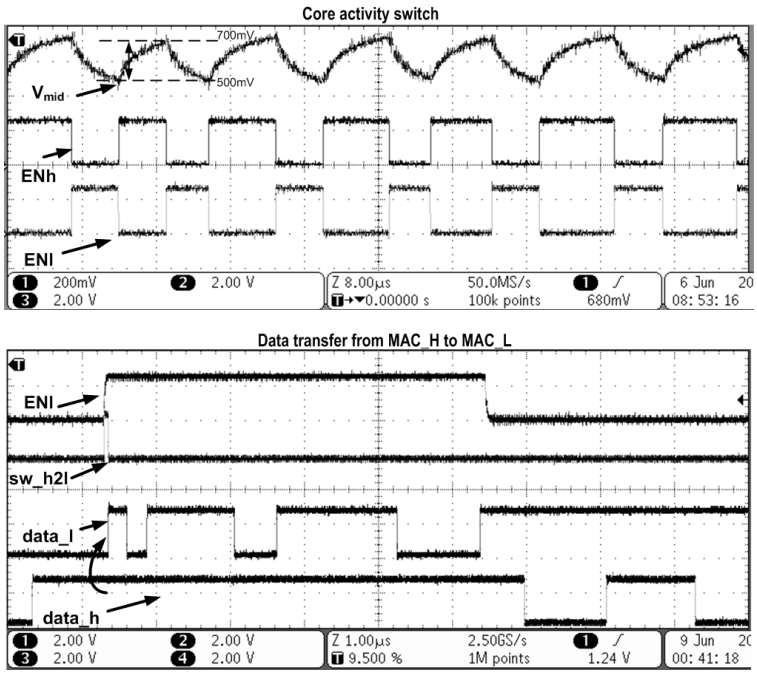
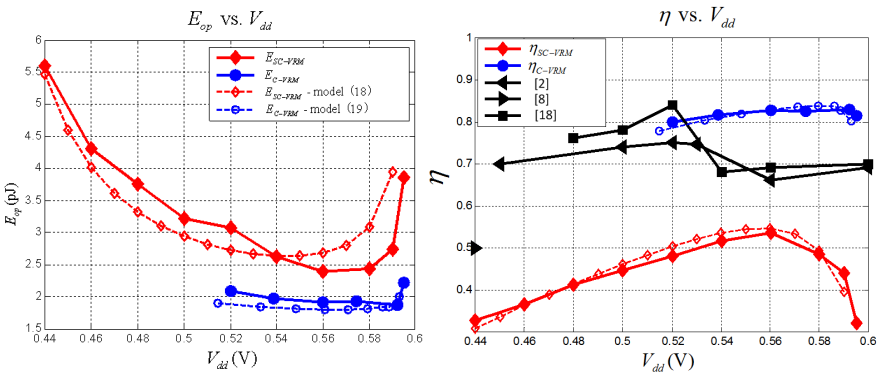


Fig. 21. Measured C-VRM core swapping and data transfer.



(a) (b)

Fig. 22. The C-VRM test chip measurement results: a) E_{op} comparison, and b) efficiency comparison.

TABLE I
COMPARISON WITH PREVIOUSLY PUBLISHED WORK

	[2]	[7]	[8]	[1]	[20]	This work (C-VRM)
Technology	65 nm	45 nm	130 nm	180 nm	32 nm	130 nm
Conversion Ratio	1/3, 1/2, 2/3, 3/4, 1	2/3	1/5	1/6	1/2, 2/3	1/2
VRM Topology	SC-VRM	SC-VRM	SC-VRM+LDO	SC-VRM+LDO	SC-VRM	Compute VRM
Input Voltage	1.2 V	1.8 V	3.6 V	3.6 V	1.8 V	1.2 V
Output power /current level	$1-500\,\mu$W	100 μA-9 mA	2.5 nW-254 nW	550 pW-7.7 μW	840 mW	$1-60\,\mu$A
C_{sc}	600 pF	534 pF	800 pF	NA	1nF	250 pF
C_{out}	NA	700 pF	NA	NA	0	0
Maximum driver switching freq.	15 MHz	30 MHz	2 KHz	1.2 MHz	125 MHz	No driver
Efficiency	75% @V_{dd}=0.5 V I_o= 100 μA	55% @V_{dd} = 0.9 V I_o= 200 μA	56% @V_{dd} = 0.44 V I_o= 300 nA	41.6% @V_{dd}= 0.4 V	90% @V_{dd} = 1.1 V	83% @V_{dd} = 0.5 V-0.7 V I_o= 40 μA
System Energy per Instruction/k-gate	1.09 pJ	1.19 pJ[1]	1.17 pJ[1]	0.88 pJ	NA	0.79 pJ

[1]System energy per instruction is calculated based on core power of the filter core in this work and the reported efficiency

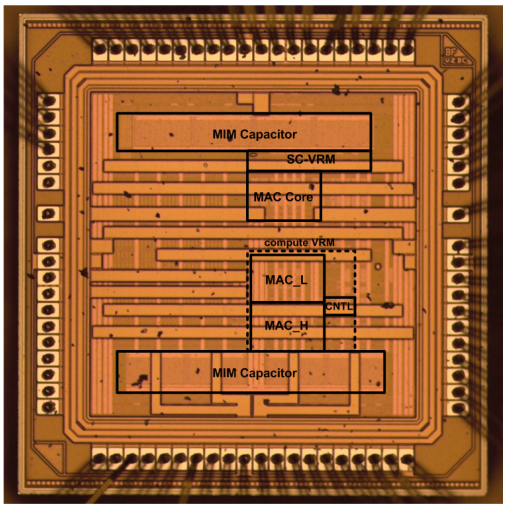


Fig. 23. Die photo of the test chip.