Naresh Shanbhag

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Education:

- 1990-93: Ph.D. in Electrical Engineering from University of Minnesota, Minneapolis.
  Area of Research: VLSI Signal Processing and Communications
- 1988-90: M.S. in Electrical Engineering from Wright State University, Dayton, Ohio.
  Area of Research: Digital Integrated Circuit Design
- 1984-88: B. Tech. in Electrical Engineering from Indian Institute of Technology, Delhi.

Professional Experience:

- **University of Illinois at Urbana-Champaign, Department of Electrical and Computer Engineering**
  - Jack Kilby Professor of Electrical and Computer Engineering: 2012-present
  - Director: Systems on Nanoscale Information fabriCs (SONIC): 2013-present.
  - Professor: 2004-present
  - Associate Professor: 2000-2004
  - Assistant Professor: 1995-2000
- **Stanford University**
  - Visiting faculty: 08/2014-12/2014
- **National Taiwan University (NTU), Taipei, Taiwan**
  - Visiting faculty: 08/2007-12/2007
- **Finisar Corporation**
  - Senior scientist (part-time): 2007-2009
- **Intersymbol Communications, Inc.**
  - Co-founder and Chief Technology Officer: 2000-2007
- **Communications IC industry**
  - Consultant: 1995-2000
- **AT&T Bell Laboratories, Murray Hill, New Jersey**
  - Member of Technical Staff: 1993-1995

- **University of Minnesota, Minneapolis, Minnesota**
  - Research Assistant: 1990-1993

- **Wright State University, Dayton, Ohio**
  - Teaching Assistant: 1988-1990

Awards and Honors:

- IEEE International Conference on Acoustics, Speech and Signal Processing, Best Student Paper Award (2016)
- IEEE International Symposium on Circuits and Systems Best Paper Award (2015)
- The D. J. Gandhi Distinguished Visiting Professorship from the Indian Institute of Technology, Mumbai, India (2015-present)
- Jack S. Kilby Professorship, Department of Electrical and Computer Engineering (2012)
- ISLPED Low-power Design Contest Award (2012)
- University of Illinois Incomplete List of Teachers Ranked Excellent, Fall 2011 (ECE 342, 483), Fall 2012 (ECE 482)
- 2010 Richard Newton GSRC Industrial Impact Award
- 2008 IEEE Solid-State Society's ISSCC Outstanding Special Evening Topic Award
- 2006 IEEE Solid-State Society Best Paper of the Year Award
- 2006 IEEE Fellow
- IRPS paper recognized as one of the 'Jewels of IRPS' in 2006.
- 2001 IEEE Transactions on VLSI Best Paper Award.
- 1999 IEEE Leon K. Kirchmayer Best Paper Award.
- 1999 Xerox Faculty Research Award.
- 1997-99, 99-01 Distinguished Lecturership of IEEE Circuits and Systems Society.
- 1996 National Science Foundation CAREER Award.
- 1994 Darlington Best Paper Award from the IEEE Circuits and Systems Society.

Patents:

- P. T. Krein, R. H. Campbell, and N. R. Shanbhag, "System and method for improving power conversion of advanced electronic circuits," *US Patent and Trademark Office*, Patent No. 9,116,692 B1, awarded August 25, 2015.

- A. C. Singer and N. R. Shanbhag, "Method and System having adjustable analog-to-digital conversion levels," *US Patent and Trademark Office*, Patent No. 8,462,037, awarded June 11, 2013.

- H.-M. Bae, N. R. Shanbhag, and A. C. Singer, "Baseband phase-locked loop," *US Patent and Trademark Office*, Patent No. 8,358,729, awarded January 22, 2013.

- J. Ashbrook, A. Singer, N. Shanbhag, and R. Drost, "A tuning system method using a simulated bit error rate for use in an electronic dispersion compensator," *US Patent and Trademark Office*, Patent No. 8,102,938, awarded January 24, 2012.

- Phase Shift Keyed Modulation of Optical Signal Using Chirp Managed Laser Cole, Christopher R.; Mahgerefteh, Daniel; Nguyen, The'Linh; Singer, Andrew C.; Shanbhag, Naresh Ramnath, Assignee: Finisar Corporation, *US Patent and Trademark Office*, Patent No. 8,068,742, awarded November 29, 2011.

- H.-M. Bae, N. Shanbhag, A. Singer, and J. Ashbrook, “Phase detector utilizing analog-to-digital converter components, *US Patent and Trademark Office*, Patent No. 7,750,831, awarded July 6, 2010.

- H.-M. Bae, N. Shanbhag and A. Singer, “Variable gain amplifier having dual gain control,” *US Patent and Trademark Office*, Patent No. 7,592,869, awarded September 22, 2009.

- H.-M. Bae, N. Shanbhag and A. Singer, “Peak detector with active ripple suppression,” *US Patent and Trademark Office*, Patent No. 7834692, awarded November 16, 2010.

- N. Shanbhag, H.-M. Bae, P. Suppiah and J. Park, “Pattern-dependent phase-detector for clock data recovery,” *US Patent and Trademark Office*, Patent No. 7609102, awarded Oct. 27, 2009.

- N. Shanbhag, H.-M. Bae, J. Park, and P. Suppiah, “A noise-tolerant VCO,” *US Patent and Trademark Office*, Patent No. 7,298,226, awarded on 20 November, 2007.

- N. R. Shanbhag, ``A pipelined adaptive IIR filter'', *US Patent and Trademark Office*, Patent No. 5,745,396, awarded on 28 April, 1998.

- N. R. Shanbhag, ``Initial phase-loading circuit for a fractionally-spaced linear equalizer'', US Patent and Trademark Office , Patent No. 5,710,794, awarded on 28 January, 1998.

- G.-H. Im, N. R. Shanbhag and J. J. Werner, ``Burst-mode update for fractionally-spaced equalization'', *US Patent and Trademark Office*, Patent No. 5,646,957, awarded on 8 July 1997.

Professional Service:

- **Program Committees:**

  - General Chair of the 2013 IEEE Workshop on Signal Processing Systems
  - General Chair of the 2012 IEEE International Symposium on Low-Power Electronics Design (ISLPED)
  - Technical Program co-Chair of the 2010 IEEE International Symposium on Low-Power Electronics Design (ISLPED)
  - Chair: System Design Subcommittee in IEEE International Conference on Computer Aided-Design (ICCAD) (2005-2008), System Design and Methodologies Subcommittee of ISLPED (2007-2008).
  - Technical Program Committee Member for IEEE International Solid-State Circuits Conference (ISSCC) Wireline Subcommittee (2006-2011), IEEE International Conference on Computer Aided-Design (ICCAD), IEEE Workshop on Signal Processing Systems (SiPS) (1999-present), IEEE International Symposium on Low-Power Electronics Design (ISLPED) (1998,99,05,06-present), IEEE International Symposium on Circuits and Systems (2000-present).
  - Member of: the VLSI Systems and Applications Technical Committee of the IEEE Circuits and Systems Society (96-present), the Design and Implementation of Signal Processing Systems (DISPS) Technical Committee of the IEEE Signal Processing

Society (99-present), and VLSI in Communications Technical Committee of the IEEE Circuits and Systems Society (99-present).

- Technical Program Chair for the 2002 IEEE Signal Processing Systems Workshop.
- Member of Technical Program Committee: 1998 Great Lakes Symposium on VLSI, 2005 IEEE Conference on Computer-Aided Design, 2000 IEEE Conference on Computer Design.

- **Editorial Boards:**

  - Associate Editor for IEEE Journal of Exploratory Solid-State Computation Devices and Circuits (2014-present)
  - Associate Editor for IEEE Transactions on VLSI (2009-2011)
  - Guest editor for special issue of the *Springer* Journal of VLSI Signal Processing on "Signal Processing for Broadband Communications" 2005.
  - 2001-2003: Associate Editor for the IEEE Transactions on VLSI Systems.
  - 1997-99: Associate Editor of IEEE Transactions on Circuits and Systems, Part II.
  - Guest editor for special issue of the Journal of VLSI Signal Processing on "Adaptive Computing for Signal Processing Systems" in 2000.

Invited Lectures and Presentations

- "Low-power techniques for next generation wireless systems," *University of California at Berkeley*, *Berkeley Wireless Research Center*, April 22, 1999.
- "Low-power multimedia communication systems," *University of California at Davis, ECE Department*, April 22, 1999.
- "Multimedia VLSI Communication Systems: Current and Future Trends," *IEEE Circuits and Systems Society Distinguished Lecturer Program*, *National Taiwan University*, IEEE Chapter of Taipei, Taiwan, Oct. 18, 1999.
- "Low-power multimedia communication systems," *National Central University*, Taiwan, Oct. 19, 1999.
- "Multimedia VLSI Communication Systems: Current and Future Trends," *IEEE Circuits and Systems Society Distinguished Lecturer Program*. *Indian Institute of Technology*, Delhi, IEEE Chapter of New Delhi, India, Oct. 28, 1999.
- "Low-power Digital Signal Processing," Invited Short Course. Mead Microelectronics. Monterey, CA, March 8, 1999.
- Invited to give a plenary talk at the 2001 IEEE Workshop on Signal Processing Systems, Antwerp, Belgium on "Reliable Low-power Multimedia Communication Systems".
- Tutorial at the IEEE Conference on Electronics, Circuits and Systems on ``Low-power Microsystems for Multimedia Technology", December 2000.
- ``Reliable Low-power Communication Systems," invited presentation at the Indian Institute of Technology, Mumbai, India, December 2002.
- ``Reliable Systems: A Communication-Theoretic Paradigm" presentation at the Gigascale Silicon Research Center Workshop, Anaheim, CA, May 2003.
- ``Reliable Systems: A Communication-Theoretic Paradigm" invited presentation at Carnegie-Mellon University, October 2003.
- ``Reliable Systems-on-a-Chip Design," invited presentation at National Chiao-Tung University, Taiwan, January 2004.

- ``Reliable Systems-on-a-Chip Design," invited presentation at IBM T. J. Watson Research Center, Yorktown Heights, NY, March 19, 2004.
- ``The Networks-on-a-Chip Design Paradigm," invited presentation at Zhejiang University, Hangzhou, China, December 23, 2004.
- ``Networks-on-a-Chip Design Paradigm," invited presentation at Intel Corporation, Bangalore, India, January 4th, 2005.
- ``Reliable and Energy-efficient Computation," invited presentation at the *Reversible Computing Workshop*, MIT, February 14th, 2005.
- ``Reliable and Energy-efficient Computation," invited presentation at the *Law of Large Numbers System Design*, Institute of Defense Analysis, March 11th, 2005.
- ``On Achieving Energy-Efficiency and Soft Error-Tolerance," invited presentation at Intel Corporation, Boston, Massachusetts, March 21st, 2005.
- ``Pushing the Limits of Interconnect Performance: A Communication-Centric Approach," invited tutorial at the *IEEE Workshop on Signal Propagation on Interconnect*, May 10-11, 2005.
- "Trusted Integrated Circuits: A Communications Perspective," invited presentation at *DARPA Workshop on Trusted ICs*, Aug. 1, 2005.
- ``Ultra Low-Power Wireless Systems," invited presentation at *DARPA Workshop on Ultra Low-Power Wireless Communications*, Aug. 4, 2005.
- "Extending Moore's Law into the Nanometer Era," invited graduate seminar at University of Minnesota, September 15th, 2005.
- "Fundamentals of Communications System-on-a-Chip Design," two-day short course at National Chiao-Tung University, Taiwan, 23-24 December, 2005.
- "Communications-inspired Design of Communications ICs," invited seminar at National Taiwan University, Taipei, Taiwan, 22 December, 2005.
- "Communications-inspired SOC Design Paradigm for Extending Moore's Law into the Nanometer Regime," invited talk at International Conference on Communications, Circuits and Systems, Guilin, China, June 2006.
- "Communications-inspired Paradigm for Ultra Low-Power Systems," invited talk at DARPA's Extreme Low-power Opportunities Workshop, Washington DC, June 2006.
- "Communications-inspired design of nanometer SOCs," invited talk at EPFL, Lausanne, September 2006.
- "Extending Moore's Law: A communications-inspired perspective," invited talk at IBM, Yorktown Heights, NY, October 2006.
- "Robust and energy-efficient design via error-resiliency," invited talk at Texas Instruments, Inc., Dallas, TX, November 2006.
- "Communications-inspired design of nanometer SOCs," invited talk at Cadence Design Systems, Inc.'s Distinguished Lecture Series, February 2007.
- "Fundamentals of Electronic Dispersion Compensation," invited tutorial at the 2007 International Solid-State Circuits Conference, San Fransisco, February 11, 2007.
- "Communications-inspired design of nanometer SOCs," invited talk at Yonsei University, South Korea, Joint UIUC-Yonsei Workshop, February 2007.
- "Communications-inspired design of interconnect," invited talk at the IEEE Lasers and Electro-optics Society Workshop on Interconnections within High-Speed Digital Systems, Santa Fe, NM, May 2007.
- "A communications-inspired paradigm for reliable and low-power SOCs in the nanometer era," invited talk at the Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, October 12, 2007.
- "Advanced Communication IC Design," invited talk at MediaTek, Hsinchu, Taiwan, Nov. 21, 2007.

- "Advanced Communication IC Design," invited talk at RealTek, Hsinchu, Taiwan, Nov. 21, 2007.
- "Communications-inspired Paradigm for Reliable and Low-power SOCs in the Nanometer Era," invited talk at the National Dong Hwa University, Hualien, Taiwan, Nov. 30th, 2007.
- "Advanced Communications SOC Design," short course (sponsored by the SOC Center) at the National Taiwan University, December 14, 2007.
- "Algorithms and Architectures for Next-Generation Optical Fiber Communications: A New Frontier for Signal Processing," IEEE Conference on Acoustics, Speech and Signal Processing, Las Vegas, March 20-April 4, 2008.
- "Advanced High-Speed I/O design," invited seminar at Advanced Micro Devices (AMD), Sunnyvale, CA, March 19, 2008.
- "Signal Processing for High-Speed I/O," invited talk at Rambus, Inc., Palo Alto, CA, March 20, 2008.
- "DSP and ICs for 40G and 100G fiber optic links," invited talk at Finisar Corp, Sunnyvale, CA, March 21, 2008.
- "Designing error-resilient communications systems-on-a-chip," invited talk at Texas Instruments, Inc., Dallas, TX, April 7, 2008.
- "Digital signal processing in optical and back-plane links," invited talk at the 2nd IBM Conference on Analog Design, Technology, Modeling and Tools, IBM, Yorktown Heights, NY, May 12, 2008.
- "Communications-inspired Design for the Deep Nanoscale Era," invited talk at the Virtual Immersion Applications Forum organized by NSF/SRC/ITRS, July 10-11, 2008, Santa Cruz, CA.
- "Communications-inspired reliable system design", invited talk at the Forum on Emerging Reliability Issues for the IC Industry organized by SRC/NIST/ISMI, November 6-7, 2008.
- "A Communications-inspired design paradigm for nanoscale SOCs," invited seminar at Columbia University, November 20, 2009.
- "Mixed-signal Reliability Challenges: A Communications-inspired view," invited presentation at the NSF Workshop on Failure and Uncertainty in Mixed-Signal Circuits and Systems, Washington, DC, July 2010.
- "A Communications-inspired design paradigm for nanoscale SOCs," invited seminar at the University of Texas at Dallas, January 28, 2011.
- "Robust and energy-efficient system design," invited seminar at Texas Instruments, Inc., Dallas, TX, February 17, 2011.
- "A Communications-inspired SOC Design Paradigm for the Nanoscale and Post-Silicon Era," invited seminar at Intel's Circuits Research Laboratory, August 25th, 2011.
- "Stochastic Computing", invited talk at Intel's FCRP Design Sciences Executive Research Review, August 26th, 2011.
- "Stochastic Computing: A design sciences driven approach to Moore's Law," invited talk at the 2nd Berkeley Symposium on Energy Efficient Electronic Systems, Nov. 3-4, 2011, UC Berkeley.
- "A Communications-inspired SOC Design Paradigm for the Nanoscale and Post-Silicon Era," invited seminar at UCLA, EE Department, November 14th, 2011.
- "Statistical Information Processing Systems: Communications-inspired SOC Design," tutorial presentation, Design Automation and Test in Europe, March 2012.
- Invited panelist on "Will Reliability be the Death of Scaling" panel at Design Automation Conference, June 3-7th, 2012.
- "Computing for the Nanoscale Era," invited ESE Colloquium at U. Penn, March 21, 2013.
- "Systems on Nanoscale Information fabriCs", Intel Corporation, webinar, OR, July 19th, 2013.
- "Systems on Nanoscale Information fabriCs", IBM, webinar, August, 2013.

- “Systems on Nanoscale Information fabriCs”, Intel Corporation, Portland, OR, September 6th, 2013.
- “Systems on Nanoscale Information fabriCs”, DARPA, Arlington, VA, September 18th, 2013.
- “Computing in the Nanoscale Era – A Shannon-inspired Perspective,” invited ECE Colloquium at University of Minnesota, September 26th, 2013.
- “Systems on Nanoscale Information fabriCs”, Intel Corporation, Bangalore, India, October 21th, 2013.
- "Computing in the Nanoscale Era – A Shannon-inspired Perspective", EPFL, Nano Tera Keynote, January 9, 2014.
- "Information-based metrics for Design on Nanoscale Fabrics", SONIC e-tutorial, Webinar, February 25, 2014.
- “Systems on Nanoscale Information fabriCs,” STARnet Scientific Advisory Board Meeting, Dallas, TX, April 30, 2014.
- “Systems on Nanoscale Information fabriCs,” IBM Corporation, Yorktown Heights, NY, May 30, 2014.
- “Shannon-inspired Statistical Computing,” Design Automation Conference, June 1, 2014.
- “Systems on Nanoscale Information fabriCs”, Intel Corporation, SONIC Center Review, Hillsboro, Oregon, September 4, 2014.
- “Circuits for energy-efficient inference kernels,” Intel Corporation, invited seminar, Hills boro, Oregon, September 3, 2014.
- “Systems on Nanoscale Information fabriCs”, Intel Corporation, SONIC Center Review, Hillsboro, Oregon, September 4, 2014.
- “Systems on Nanoscale Information fabriCs”, SONIC Center Annual Review Meeting, Urbana, October 9, 2014.
- “Systems on Nanoscale Information fabriCs”, GlobalFoundaries, SONIC Center Overview, November 1 & 19, 2014
- “Shannon-inspired Statistical Computing,” University of Texas A&M, invited seminar, Eminent Speaker Series, A&M, November 3, 2014.
- “Shannon-inspired Statistical Computing,” University of California at Santa Barbara, Invited Seminar, Computer Engineering Seminar Series, November 13, 2014.
- “Shannon-inspired Statistical Computing,” Stanford University, Invited Seminar, December 3, 2014.
- “Shannon-inspired Statistical Computing,” HGST, Invited Seminar, San Jose, CA, December 16, 2014.
- “Shannon-inspired Statistical Computing,” Tata Institute of Fundamental Research, Invited Seminar, January 12, 2015.
- “Systems on Nanoscale Information fabriCs,” International Technology Roadmap for Semiconductors, Emerging Research Devices and Architectures Workshop, Invited Seminar, February 26-27, 2015.
- “Shannon-inspired Statistical Computing,” Joint IEEE Solid-State Circuits Society and IEEE Information Theory Society organized invited seminar, Santa Clara Valley Lecture Series, February 27, 2015.
- “Systems on Nanoscale Information fabriCs”, DARPA, SONIC Center Overview, March 17, 2015.
- “Systems on Nanoscale Information fabriCs”, Intel, SONIC Center Overview, April 2, 2015 and September 17, 2015.
- “Systems on Nanoscale Information fabriCs”, STARnet Scientific Advisory Board, SONIC Center Overview, April 7, 2015.
- “Statistical Information Processing – Extending the Limits of Approximate Computing,” Workshop on Approximate Computing, June 13, 2015.

- "Systems on Nanoscale Information fabriCs", DARPA, SONIC Center Overview, November 12, 2015.
- "Shannon-inspired Statistical Computing," Indian Institute of Technology, Mumbai, January 12, 2016.
- "Systems on Nanoscale Information fabriCs", Micron Technologies, Inc., SONIC Center Overview, March 21, 2016.
- "Systems on Nanoscale Information fabriCs and In-memory Computing", Intel, SONIC Center Overview, April 13, 2016.
- "Systems on Nanoscale Information fabriCs and In-memory Computing", Raytheon, SONIC Center Overview, June 3, 2016.
- "Enabling Spin via Shannon-inspired Statistical Information Processing," Workshop on Spintronics, sponsored by STARnet C-SPIN Center, June 5, 2016.
- "Machine Learning in Silicon – A Communications-inspired Perspective," International Conference on Machine Learning (ICML) Workshop on On-device Intelligence, New York City, June 24, 2016.

Featured Magazine Articles:

- "Is Subthreshold all that?" by Chris Edwards, *www.electronicsweekly.com*, January 4, 2012.
- "The Era of Error-tolerant Computing," by David Lammers, *IEEE Spectrum*, 2010.
- "Computing without Guarantees," DAC 2010 Roundtable featured in the *IEEE Design and Test of Computers*, September/October 2010.

List of Publications:

- **Books/Monographs**

  - N. R. Shanbhag, *Systems and Integrated Circuit Architectures for Communications*. Springer (in progress, 2015 target completion date).
  - N. R. Shanbhag and K. K. Parhi, *Pipelined Adaptive Digital Filters*. Kluwer Academic Publishers, 1994.

- **Book Chapters**

  - N. Shanbhag, A. Singer, and H.-M. Bae, ``Signal processing for High-Speed Links," *Handbook of Signal Processing Systems*, Springer, 2010.
  - A. Ahmed, S.-J. Lee, M. Mansour, and N. R. Shanbhag, "VLSI architectures for Forward Error-Control Decoders," *The VLSI Handbook*, CRC Press, 2007.
  - N. R. Shanbhag, ``High-Speed Data Transmission over Twisted-Pair Channels," *Digital Signal Processing for Multimedia Systems*, Marcel Dekker, Inc., 1998.
  - N. R. Shanbhag and K. K. Parhi, ``Pipelined Adaptive Digital Filters Using Relaxed Look-ahead", *Microsystems Technology for Multimedia Application: An Introduction*, IEEE Press, 1995.
  - N. R. Shanbhag and K. K. Parhi, ``VLSI implementation of a 100 MHz pipelined ADPCM codec chip", *VLSI Signal Processing VI*, IEEE Press, Oct. 1993, pp. 114-122.

■ Journal Publications

- M. Kang and N. R. Shanbhag, “In-memory computing architectures for sparse distributed memory,” *IEEE Transactions on Biomedical Circuits and Systems*, vol. 10, no. 4, pp. 855-863, August 2016.
- Y. Lin, M.-S. Keel, A. Faust, A. Xu, N. R. Shanbhag, E. Rosenbaum, and A. Singer, “A study of BER optimal ADC based receivers for serial links,” *IEEE Transactions on Circuits and Systems*, vol. 63, no. 5, pp. 693-704, May 2016.
- S. Zhang and N. R. Shanbhag, "Embedded error compensation for DSP and machine learning systems,” *IEEE Transactions on Signal Processing*, vol. 64, no. 13, pp. 3338-3350, July 2016.
- E. Kim, J. Choi, N. R. Shanbhag, and R. Rutenbar, “Error resilient and energy efficient MRF message passing based stereo image matching,” *IEEE Transactions on VLSI*, vol. 24, no. 3, pp. 897-908, March 2016.
- S. Zhang, J. Tu, N. R. Shanbhag, and P. Krein, “A 0.79 pJ/K-gate, 83% efficient unified core and voltage regulator architecture for sub/near-threshold operation in 130nm CMOS,” *IEEE Journal of Solid-State Circuits*, vol. 49, no. 11, pp. 2644-2657, November 2014.
- S. Zhang, N. R. Shanbhag, and P. Krein, “System-Level Optimization of Switched-Capacitor VRM and Core for Sub/Near-Vt Computing,” *IEEE Transactions on Circuits and Systems - II*, vol. 61, no. 9, pp. 726-730, September 2014.
- R. A. Abdallah, and N. R. Shanbhag, “Reducing energy at the minimum energy operating point (MEOP) via statistical error compensation,” *IEEE Transactions on VLSI*, vol. 22, no. 6, pp. 1328-1337, June 2014.
- E. P. Kim, D. Baker, S. Narayanan, N. R. Shanbhag, D. L. Jones, “A 3.6-mW 50-MHz PN code acquisition filter via statistical error compensation in 180nm CMOS,” *IEEE Transactions on VLSI*, April 2014 (Early Access).
- R. A. Abdallah, and N. R. Shanbhag, “An energy-efficient ECG processor in 45nm CMOS using statistical error compensation,” *IEEE Journal of Solid-State Circuits*, vol. 48, no. 11, pp. 2882-2893, November 2013.
- R. A. Abdallah, and N. R. Shanbhag, “Robust and energy-efficient multimedia systems via likelihood processing,” *IEEE Transactions on Multimedia*, vol. 15, no. 2, pp. 257-267, February 2013.
- R. Narasimha, M. Lu, N. R. Shanbhag, and A. Singer, “BER-Optimal Analog-to-Digital converters for communication links,” *IEEE Transactions on Signal Processing*, vol. 60, no. 7, pp. 3683-3691, July 2012.
- A. Ahmed, R. Koetter, and N. R. Shanbhag, “VLSI architectures for soft-decision decoding of Reed-Solomon codes,” *IEEE Transactions on Information Theory*, vol. 57, no. 2, pp. 648-667, February, 2011.
- E. Kim and N. R. Shanbhag, “Soft N-modular redundancy,” *IEEE Transactions on Computers*, vol. 61, no. 3, pp. 323-336, March 2012.
- R. A. Abdallah, and N. R. Shanbhag, “Minimum energy operation via error-resiliency,” *IEEE Embedded Systems Letter*, vol. 2, no. 4, pp. 115-118, December 2010.
- G. Varatkar, S. Narayanan, N. Shanbhag and D. Jones, “The stochastic networked computation,” *IEEE Transactions on VLSI*, vol. 18, no. 10, pp. 1421-1432, October 2010.
- S. Narayanan, G. Varatkar, D. L. Jones, and N. R. Shanbhag, “Computation as estimation: A general framework for robustness and energy-efficiency in SoCs,” *IEEE Transactions on Signal Processing*, vol. 58, no. 8, pp. 4416-4421, August 2010.

- R. Narasimha and N. R. Shanbhag, “Design of energy-efficient high-speed links via forward error-correction (FEC),” *IEEE Transactions on Circuits and Systems-II*, vol. 57, no. 5, pp. 359-363, May 2010.
- R. Abdallah and N. R. Shanbhag, “Error-resilient low-power Viterbi decoder architectures,” *IEEE Transactions on Signal Processing*, vol. 57, no. 12, pp. 4906-4917, December 2009.
- H.-M. Bae, J. B. Ashbrook, N. R. Shanbhag, and A. C. Singer, “Fast power transient management for OC-192 add/drop networks,” *IEEE Journal of Solid-State Circuits*, vol. 43, no. 12, pp. 2958-2966, December 2008.
- A. Singer, N. Shanbhag and H.-M. Bae, “Electronic dispersion compensation,” *IEEE Signal Processing Magazine*, vol. 25, no. 6, pp. 110-130, November 2008.
- N. Shanbhag, S. Mitra, G. D. Veciana, M. Orshansky, R. Marculescu, J. Roychowdhury, D. Jones, and J. Rabaey, “The search for alternative computational paradigms for the post-silicon era,” *IEEE Design and Test of Computers*, pp. 334-343, July/August 2008.
- G. Varatkar and N. Shanbhag, “Error-resilient motion-estimation architecture,” *IEEE Transactions on VLSI*, vol. 16, no. 10, pp. 1399-1412, October 2008.
- S. Sridhara, G. Balamurugan, and N. R. Shanbhag, “Joint equalization and coding for on-chip bus communications,” *IEEE Transactions on VLSI*, vol. 16, no. 3, pp. 314-318, March 2008.
- S. Sridhara and N. R. Shanbhag, ``Coding for reliable on-chip busses: A class of fundamental bounds and practical codes,” *IEEE Transactions on CAD*, vol. 26, no. 5, pp. 977-982, May 2007.
- M. Zhang and N. R. Shanbhag, “Dual sampling skewed CMOS design for soft error-tolerance,” *IEEE Transactions on CAS II*, vol. 53, no. 12, pp. 1461-1465, Dec. 2006.
- M. Zhang, S. Mitra, T. M. Mak, N. Seifert, Q. Shi, K.-S. Kim, N. R. Shanbhag, N. Wang, and S. Patel, “Robust sequential element design with built-in soft-error resilience,” *IEEE Transactions on TVLSI*, vol. 14, no. 12, pp. 1368-1378, December 2006.
- H.-M. Bae, J. B. Ashbrook, J. Park, N. R. Shanbhag, A. C. Singer, and S. C. Chopra, “An MLSE receiver for electronic dispersion compensation of OC-192 fiber links,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 11, pp. 2541-2554, Nov. 2006.
- M. Zhang and N. R. Shanbhag, “Soft error-rate analysis (SERA) methodology,” *IEEE Transactions on CAD*, vol. 25, no. 10, pp. 2140-2155, Oct. 2006.
- B. Shim and N. R. Shanbhag, ``Energy-efficient soft-error tolerant digital signal processing,” *IEEE Trans. on VLSI*, vol. 14, no. 4, pp. 336-348, April 2006.
- M. Mansour and N. R. Shanbhag, “A 640-Mb/s 2048-bit programmable LDPC decoder chip,” *IEEE Journal of Solid-State Circuits*, vol. 41, no. 3, pp. 684-698, March 2006.
- S. Sridhara and N. R. Shanbhag, ``Coding for system-on-chip networks: A unified framework,” *IEEE Transactions on VLSI*, vol. 13, no. 2, pp. 655-667, June 2005.
- Seok-Jun Lee, Naresh R. Shanbhag, and Andrew C. Singer, "A 285-MHz MAP decoder in 0.18µm CMOS," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 8, pp. 1718-1725, August 2005.
- Seok-Jun Lee, Andrew C. Singer, and Naresh R. Shanbhag, "Linear turbo equalization analysis via linearized BER transfer and EXIT charts," *IEEE Tran. Signal Processing*, vol. 53, no. 8, pp. 2883-2897, August 2005.
- S.-J. Lee, N. R. Shanbhag and A. C. Singer, ``Area-efficient, high-throughput MAP decoder architectures,” *IEEE Trans. on VLSI Systems*, vol. 13, no. 8, pp. 921-933, August 2005.
- J. E. Jaussi, G. Balamurugan, D. R. Johnson, B. Casper, A. Martin, J. Kennedy, N. Shanbhag, R. Mooney, “8-Gb/s source-synchronous I/O link with adaptive receiver

equalization, offset cancellation, and clock de-skew," *IEEE Journal of Solid-State Circuits*, vol. 40, no. 1, pp. 80-88, January 2005.

- M. Mansour and N. R. Shanbhag, ``A novel design methodology for high-performance programmable decoder cores for AA-LDPC codes," *Journal of VLSI Signal Processing*, pp. 371-382, 2005.
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