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Education:

- 1990-1993: Ph.D. in Electrical Engineering from University of Minnesota, Minneapolis.
  Area of Research: VLSI Signal Processing and Communications
- 1988-1990: M.S. in Electrical Engineering from Wright State University, Dayton, Ohio.
  Area of Research: Digital Integrated Circuit Design
- 1984-1988: B. Tech. in Electrical Engineering from Indian Institute of Technology, Delhi.

Professional Experience:

- **University of Illinois at Urbana-Champaign, Department of Electrical and Computer Engineering**
  - Jack Kilby Professor of Electrical and Computer Engineering: 2012-present
  - Director: Systems on Nanoscale Information fabriCs (SONIC): 2013-2018
  - Professor: 2004-present
  - Associate Professor: 2000-2004
  - Assistant Professor: 1995-2000

- **Stanford University**
  - Visiting faculty: 08/2014-12/2014

- **National Taiwan University (NTU), Taipei, Taiwan**
  - Visiting faculty: 08/2007-12/2007

- **Finisar Corporation**
  - Senior scientist (part-time): 2007-2009

- **Intersymbol Communications, Inc.**
  - Co-founder and Chief Technology Officer: 2000-2007

- **Communications IC industry**
  - Consultant: 1995-2000

- **AT&T Bell Laboratories, Murray Hill, New Jersey**
  - Member of Technical Staff: 1993-1995

- **University of Minnesota, Minneapolis, Minnesota**
  - Research Assistant: 1990-1993

- **Wright State University, Dayton, Ohio**
  - Teaching Assistant: 1988-1990

Awards and Honors:

- IEEE MICRO Top Picks – honorable mention (2019)
- IEEE International Symposium on Circuits and Systems Best Paper Award (2019)
- IEEE International Symposium on Circuits and Systems Best Paper Award (2018)
- 2018 SIA-SRC University Researcher Award, Semiconductor Industry Association, (November 2018)
- IEEE International Symposium on Circuits and Systems Best Paper Award (2018)
- IEEE Signal Processing Systems, Bob Owens Best Student Paper Award (2016)
- IEEE International Conference on Acoustics, Speech and Signal Processing, Best Student Paper Award (2016)
- IEEE International Symposium on Circuits and Systems Best Paper Award (2015)
- The D. J. Gandhi Distinguished Visiting Professorship from the Indian Institute of Technology, Bombay, India (2015-20)
- Jack S. Kilby Professorship, Department of Electrical and Computer Engineering (2012)
- ISLPED Low-power Design Contest Award (2012)
- University of Illinois Incomplete List of Teachers Ranked Excellent, Fall 2011 (ECE 342, 483), Fall 2012, 2018 (ECE 482), Fall 2019 (ECE 498NSU), Fall 2020 (ECE 598NSG)
- 2010 Richard Newton GSRC Industrial Impact Award
- 2008 IEEE Solid-State Society's ISSCC Outstanding Special Evening Topic Award
- 2006 IEEE Solid-State Society Best Paper of the Year Award
- 2006 IEEE Fellow
- IRPS paper recognized as one of the 'Jewels of IRPS' in 2006
- 2001 IEEE Transactions on VLSI Best Paper Award
- 1999 IEEE Leon K. Kirchmayer Best Paper Award
- 1999 Xerox Faculty Research Award
- 1997-1999, 1999-2001 Distinguished Lecturership of IEEE Circuits and Systems Society
- 1996 National Science Foundation CAREER Award
- 1994 Darlington Best Paper Award from the IEEE Circuits and Systems Society

Patents:

- N. R. Shanbhag, M. Kang, and M.-S. Keel, "Compute Memory", *US Patent and Trademark Office*, Patent No. 9,697,877 B2, awarded July 4, 2017.
- P. T. Krein, R. H. Campbell, and N. R. Shanbhag, "System and method for improving power conversion of advanced electronic circuits", *US Patent and Trademark Office*, Patent No. 9,116,692 B1, awarded August 25, 2015.
- A. C. Singer and N. R. Shanbhag, "Method and System having adjustable analog-to-digital conversion levels", *US Patent and Trademark Office*, Patent No. 8,462,037, awarded June 11, 2013.
- H.-M. Bae, N. R. Shanbhag, and A. C. Singer, "Baseband phase-locked loop", *US Patent and Trademark Office*, Patent No. 8,358,729, awarded January 22, 2013.
- J. Ashbrook, A. Singer, N. Shanbhag, and R. Drost, "A tuning system method using a simulated bit error rate for use in an electronic dispersion compensator", *US Patent and Trademark Office*, Patent No. 8,102,938, awarded January 24, 2012.
- Phase Shift Keyed Modulation of Optical Signal Using Chirp Managed Laser
  Cole, Christopher R.; Mahgerefteh, Daniel; Nguyen, The'Linh; Singer, Andrew C.; Shanbhag, Naresh Ramnath, Assignee: Finisar Corporation, *US Patent and Trademark Office*, Patent No. 8,068,742, awarded November 29, 2011.
- H.-M. Bae, N. Shanbhag, A. Singer, and J. Ashbrook, "Phase detector utilizing analog-to-digital converter components", *US Patent and Trademark Office*, Patent No. 7,750,831, awarded July 6, 2010.
- H.-M. Bae, N. Shanbhag and A. Singer, "Variable gain amplifier having dual gain control", *US Patent and Trademark Office*, Patent No. 7,592,869, awarded September 22, 2009.
- H.-M. Bae, N. Shanbhag and A. Singer, "Peak detector with active ripple suppression", *US Patent and Trademark Office*, Patent No. 7834692, awarded November 16, 2010.
- N. Shanbhag, H.-M. Bae, P. Suppiah and J. Park, "Pattern-dependent phase-detector for clock data recovery", *US Patent and Trademark Office*, Patent No. 7609102, awarded October 27, 2009.
- N. Shanbhag, H.-M. Bae, J. Park, and P. Suppiah, "A noise-tolerant VCO", *US Patent and Trademark Office*, Patent No. 7,298,226, awarded November 20, 2007.
- N. R. Shanbhag, "A pipelined adaptive IIR filter", *US Patent and Trademark Office*, Patent No. 5,745,396, awarded April 28, 1998.
- N. R. Shanbhag, "Initial phase-loading circuit for a fractionally-spaced linear equalizer", US Patent and Trademark Office Patent No. 5,710,794, awarded January 28, 1998.

- G.-H. Im, N. R. Shanbhag and J. J. Werner, "Burst-mode update for fractionally-spaced equalization", *US Patent and Trademark Office*, Patent No. 5,646,957, awarded July 8, 1997.

Professional Service:

- **Program Committees:**
  - General Chair of the 2013 IEEE Workshop on Signal Processing Systems
  - General Chair of the 2012 IEEE International Symposium on Low-Power Electronics Design (ISLPED)
  - Technical Program co-Chair of the 2010 IEEE International Symposium on Low-Power Electronics Design (ISLPED)
  - Chair: System Design Subcommittee in IEEE International Conference on Computer Aided-Design (ICCAD) (2005-2008), System Design and Methodologies Subcommittee of ISLPED (2007-2008).
  - Technical Program Committee Member for IEEE International Solid-State Circuits Conference (ISSCC) Wireline Subcommittee (2006-2011), IEEE International Conference on Computer Aided-Design (ICCAD), IEEE Workshop on Signal Processing Systems (SiPS) (1999-present), IEEE International Symposium on Low-Power Electronics Design (ISLPED) (1998, 1999, 2005, 2006-present), IEEE International Symposium on Circuits and Systems (2000-present).
  - Member of: the VLSI Systems and Applications Technical Committee of the IEEE Circuits and Systems Society (1996-present), the Design and Implementation of Signal Processing Systems (DISPS) Technical Committee of the IEEE Signal Processing Society (1999-present), and VLSI in Communications Technical Committee of the IEEE Circuits and Systems Society (1999-present).
  - Technical Program Chair for the 2002 IEEE Signal Processing Systems Workshop.
  - Member of Technical Program Committee: 1998 Great Lakes Symposium on VLSI, 2005 IEEE Conference on Computer-Aided Design, 2000 IEEE Conference on Computer Design.

- **Editorial Boards:**
  - Associate Editor for IEEE Journal of Exploratory Solid-State Computation Devices and Circuits (2014-present)
  - Associate Editor for IEEE Transactions on VLSI (2009-2011)
  - Guest editor for special issue of the *Springer* Journal of VLSI Signal Processing on "Signal Processing for Broadband Communications" 2005.
  - 2001-2003: Associate Editor for the IEEE Transactions on VLSI Systems.
  - 1997-1999: Associate Editor of IEEE Transactions on Circuits and Systems, Part II.
  - Guest editor for special issue of the Journal of VLSI Signal Processing on "Adaptive Computing for Signal Processing Systems" in 2000.

Invited Lectures and Presentations

- "Overcoming Noise and Enhancing the Accuracy of Analog-based IMCs," Invited talk at the 2021 DARPA Electronic Resurgence Initiative, October 19, 2021.
- "Facilitating Devices-to-Systems Research at Scale via CMOS+X," Invited Panelist at the NSF Workshop on CMOS+C, August 17-18, 2021.
- "In-memory Architectures for Machine Learning and RF Communications – Prospects and Challenges," Invited Speaker at the International Microwave Symposium (IMS)/RFIC Workshop on Machine Learning and AI Techniques with Intelligent Systems for Wireless Communication, Sensing and Computation, June 20, 2021.
- "In-memory Computing – A Shannon-inspired Perspective," Invited Panelist at the 2021 NSF Workshop on Devices-to-Systems for In-memory Computing, May 11, 2021.
- "In-memory Computing – Trends and Prospects," Invited Panelist at the 2021 NSF Workshop on Processing-in-Memory, March 17, 2021.
- "What Technologies Will Shape the Future of Computing," Invited Panelist, IEEE International Solid-State Circuits Conference (ISSCC), February 19, 2021.
- "Fundamental Limits on the Precision of In-memory Architectures," Invited talk, IEEE International Conference on Computer-Aided Design, November 2020.
- "Deep In-memory Architectures and Algorithms for Automatic Target Recognition," A4H Virtual Field Day, Sandia National Labs, August 4, 2020.
- "Minimum Precision Requirements of Deep Neural Networks," Invited talk, Numerical Verification Software, July 20, 2020.

- "Deep Learning in Hardware," Invited Short Course, Indian Institute of Technology, Bombay, January 6-10, 2020.
- "Accuracy, Robustness, Complexity Trade-offs in Deep Learning," SRC IBM Executive Review, T. J. Watson Research Center, November 8, 2019.
- "Bringing AI to the Edge via Shannon-inspired Statistical Computing", IBM/IEEE AI Compute Symposium, T. J. Watson Research Center, October 17, 2019.
- "Computing for the Nanoscale Era", SRC/SIA/DoE Decadal Plan Workshop on New Compute Trajectories for Energy-Efficient Computing, Sandia National Labs, Livermore, CA, October 15-16, 2019.
- "Understanding the Accuracy, Robustness, Complexity Trade-offs in Deep Learning," C-BRIC Annual Meeting, Purdue University, October 7-8, 2019.
- "MRAM-based Deep In-memory Architectures," The Electronics Resurgence Initiative Summit, Detroit, MI, July 15-17, 2019.
- "Bringing Artificial Intelligence to the Edge – A Shannon-inspired Approach," Tutorial at the IEEE Symposium on Circuits and Systems, Sapporo, Japan, May 26, 2019.
- "Bringing Artificial Intelligence to the Edge – A Shannon-inspired Approach," Toshiba Corporation, Kawasaki, Japan, May 23, 2019.
- "Bringing Artificial Intelligence to the Edge – A Shannon-inspired Approach," Peking University, Beijing, China, May 14, 2019.
- "Bringing Artificial Intelligence to the Edge – A Shannon-inspired Approach," Tsinghua University, Beijing, China, May 15, 2019.
- "Shannon-inspired Deep In-memory Computing," Forum on Alternative Models of Computation using Analog/Mixed-signal Substrates at the IEEE Custom Integrated Circuits Conference, Austin, TX, April 17, 2019.
- "Choices and Consequences for Neural Network Hardware and Systems", Panel at the IEEE Custom Integrated Circuits Conference, Austin, TX, April 16, 2019.
- "The Deep In-memory Architecture for Energy-efficient Machine Learning," Sunday Forum at IEEE Solid-State Circuits Conference, San Fransisco, CA, February 17, 2019.
- "Bringing Artificial Intelligence to the Edge – A Shannon-inspired Approach," Samsung, November 30, 2018.
- "Designing AI Systems at the Edge - Shannon-inspired Deep In-memory Architectures," Hardware and Algorithms for Learning On-a-Chip (HALO) Workshop, ICCAD 2018, November 15, 2018.
- "Bringing Artificial Intelligence to the Edge – A Shannon-inspired Approach," Qualcomm, November 14, 2018.
- "MRAM-based Deep In-memory Architectures," The Electronics Resurgence Initiative Summit, San Francisco, CA, July 24, 2018.
- "How can circuit and technology experts drive advances leading to the next wave of machine learning and artificial intelligence?", Lunch Panel at VLSI Symposium, Honolulu, HI, June 22, 2018.
- "The Deep In-memory Architecture for Energy Efficient Machine Learning", Friday Forum at VLSI Symposium, HI, June 22, 2018.
- "Nanoscale Information Processing" (with L. Varshney), International Symposium on Information Theory, Vail, CO, June 17, 2018.
- "Bringing Artificial Intelligence to the Edge – A Shannon-inspired Approach", Northwestern University, Distinguished Lecture, May 9, 2018.
- "Systems on Nanoscale Information fabriCs – Outcomes and Future Prospects", GOMACTech, Miami, FL, March 15, 2018.
- "Cognitive Computing at the Limits", NSF Nanoscale Science and Engineering Grantees Workshop, December 13, 2017.
- "Systems on Nanoscale Information fabriCs", National Taiwan University, Taiwan, August 18, 2017.
- "Systems on Nanoscale Information fabriCs", Zhejiang University, China, August 14, 2017.
- "Systems on Nanoscale Information fabriCs and In-memory Computing", GLOBALFOUNDRIES, SONIC Center Overview, August 4, 2017.
- "Computing in the nanoscale era – A Shannon-inspired perspective", SPIE Defense + Commercial Sensing, Anaheim, CA, April 9, 2017
- "A systems approach to computing in beyond CMOS fabrics", Design Automation Conference , Austin, TX, June 20, 2017
- "Machine Learning in Silicon" Guest Lecture Series, Indian Institute of Technology Bombay, Mumbai, India, December 27, 2016 – January 10, 2017
- "Systems on nanoscale information fabrics (SONIC)", DARPA STARnet: University Day, Los Angeles, CA, October 19, 2016
- "Shannon-inspired Concepts in Spin Computing", Intel STARnet Review, Hillsboro, OR, September 9, 2016.
- "Connecting systems-to-devices – The SONIC journey", Nanotechnology-inspired Information Processing Systems of the Future workshop, Washington DC, September 1, 2016.

- "Connecting Systems-to-Devices – The SONIC Journey", Visioning Workshop on Nanotechnology-inspired Future of Information Processing, Washington DC., August 31-September 1, 2016.
- "Enabling Spin via Shannon-inspired Statistical Information Processing", Joint LEAST-SONIC Workshop on Beyond CMOS Circuits and Systems, Notre Dame, IN, August 8, 2016.
- Panelist on the Semiconductor R&D Round Table organized by the White House Office of Science and Technology Policy (OSTP), Washington DC, July 29, 2016.
- "Machine Learning in Silicon – A Communications-inspired Perspective", International Conference on Machine Learning (ICML) Workshop on On-device Intelligence, New York City, NY, June 24, 2016.
- "Enabling Spin via Shannon-inspired Statistical Information Processing", Workshop on Spintronics, sponsored by STARnet C-SPIN Center, June 5, 2016.
- "Systems on Nanoscale Information fabriCs and In-memory Computing", Raytheon, SONIC Center Overview, June 3, 2016.
- "Systems on Nanoscale Information fabriCs and In-memory Computing", Intel, SONIC Center Overview, April 13, 2016.
- "Systems on Nanoscale Information fabriCs", Micron Technologies, Inc., SONIC Center Overview, March 21, 2016.
- "Shannon-inspired Statistical Computing", Indian Institute of Technology, Mumbai, January 12, 2016.
- "Systems on Nanoscale Information fabriCs", DARPA, SONIC Center Overview, November 12, 2015.
- "Systems on Nanoscale Information fabriCs", Intel, SONIC Center Overview, April 2, 2015 and September 17, 2015.
- "Statistical Information Processing – Extending the Limits of Approximate Computing", Workshop on Approximate Computing, June 13, 2015.
- "Systems on Nanoscale Information fabriCs", STARnet Scientific Advisory Board, SONIC Center Overview, April 7, 2015.
- "Systems on Nanoscale Information fabriCs", DARPA, SONIC Center Overview, March 17, 2015.
- "Shannon-inspired Statistical Computing", Joint IEEE Solid-State Circuits Society and IEEE Information Theory Society organized invited seminar, Santa Clara Valley Lecture Series, February 27, 2015.
- "Systems on Nanoscale Information fabriCs", International Technology Roadmap for Semiconductors, Emerging Research Devices and Architectures Workshop, Invited Seminar, February 26-27, 2015.
- "Shannon-inspired Statistical Computing", Tata Institute of Fundamental Research, Invited Seminar, January 12, 2015.
- "Shannon-inspired Statistical Computing", HGST, Invited Seminar, San Jose, CA, December 16, 2014.
- "Shannon-inspired Statistical Computing", Stanford University, Invited Seminar, December 3, 2014.
- "Shannon-inspired Statistical Computing", University of California at Santa Barbara, Invited Seminar, Computer Engineering Seminar Series, November 13, 2014.
- "Shannon-inspired Statistical Computing", University of Texas A&M, invited seminar, Eminent Speaker Series, November 3, 2014.
- "Systems on Nanoscale Information fabriCs", GlobalFoundaries, SONIC Center Overview, November 1 & 19, 2014
- "Systems on Nanoscale Information fabriCs", SONIC Center Annual Review Meeting, Urbana, October 9, 2014.
- "Systems on Nanoscale Information fabriCs", Intel Corporation, SONIC Center Review, Hillsboro, OR, September 4, 2014.
- "Circuits for energy-efficient inference kernels", Intel Corporation, invited seminar, Hillsboro, OR, September 3, 2014.
- "Systems on Nanoscale Information fabriCs", Intel Corporation, SONIC Center Review, Hillsboro, OR, September 4, 2014.
- "Shannon-inspired Statistical Computing", Design Automation Conference, June 1, 2014.
- "Systems on Nanoscale Information fabriCs", IBM Corporation, Yorktown Heights, NY, May 30, 2014.
- "Systems on Nanoscale Information fabriCs", STARnet Scientific Advisory Board Meeting, Dallas, TX, April 30, 2014.
- "Information-based metrics for Design on Nanoscale Fabrics", SONIC e-tutorial, Webinar, February 25, 2014.
- "Computing in the Nanoscale Era – A Shannon-inspired Perspective", EPFL, Nano Tera Keynote, January 9, 2014.
- "Systems on Nanoscale Information fabriCs", Intel Corporation, Bangalore, India, October 21, 2013.
- "Computing in the Nanoscale Era – A Shannon-inspired Perspective", invited ECE Colloquium at University of Minnesota, September 26, 2013.
- "Systems on Nanoscale Information fabriCs", DARPA, Arlington, VA, September 18, 2013.
- "Systems on Nanoscale Information fabriCs", Intel Corporation, Portland, OR, September 6, 2013.
- "Systems on Nanoscale Information fabriCs", IBM, webinar, August, 2013.
- "Systems on Nanoscale Information fabriCs", Intel Corporation, webinar, July 19, 2013.
- "Computing for the Nanoscale Era", invited ESE Colloquium at U. Penn, March 21, 2013.
- Invited panelist on "Will Reliability be the Death of Scaling" panel at Design Automation Conference, June 3-7, 2012.
- "Statistical Information Processing Systems: Communications-inspired SOC Design", tutorial presentation, Design Automation and Test in Europe, March 2012.

- "A Communications-inspired SOC Design Paradigm for the Nanoscale and Post-Silicon Era", invited seminar at UCLA, EE Department, November 14, 2011.
- "Stochastic Computing: A design sciences driven approach to Moore's Law", invited talk at the 2nd Berkeley Symposium on Energy Efficient Electronic Systems, November 3-4, 2011, UC Berkeley.
- "Stochastic Computing", invited talk at Intel's FCRP Design Sciences Executive Research Review, August 26, 2011.
- "A Communications-inspired SOC Design Paradigm for the Nanoscale and Post-Silicon Era", invited seminar at Intel's Circuits Research Laboratory, August 25, 2011.
- "Robust and energy-efficient system design", invited seminar at Texas Instruments, Inc., Dallas, TX, February 17, 2011.
- "A Communications-inspired design paradigm for nanoscale SOCs", invited seminar at the University of Texas at Dallas, January 28, 2011.
- "Mixed-signal Reliability Challenges: A Communications-inspired view", invited presentation at the NSF Workshop on Failure and Uncertainty in Mixed-Signal Circuits and Systems, Washington, DC, July 2010.
- "A Communications-inspired design paradigm for nanoscale SOCs", invited seminar at Columbia University, November 20, 2009.
- "Communications-inspired reliable system design", invited talk at the Forum on Emerging Reliability Issues for the IC Industry organized by SRC/NIST/ISMI, November 6-7, 2008.
- "Communications-inspired Design for the Deep Nanoscale Era", invited talk at the Virtual Immersion Applications Forum organized by NSF/SRC/ITRS, Santa Cruz, CA, July 10-11, 2008.
- "Digital signal processing in optical and back-plane links", invited talk at the 2nd IBM Conference on Analog Design, Technology, Modeling and Tools, IBM, Yorktown Heights, NY, May 12, 2008.
- "Designing error-resilient communications systems-on-a-chip", invited talk at Texas Instruments, Inc., Dallas, TX, April 7, 2008.
- "DSP and ICs for 40G and 100G fiber optic links", invited talk at Finisar Corp, Sunnyvale, CA, March 21, 2008.
- "Signal Processing for High-Speed I/O", invited talk at Rambus, Inc., Palo Alto, CA, March 20, 2008.
- "Advanced High-Speed I/O design", invited seminar at Advanced Micro Devices (AMD), Sunnyvale, CA, March 19, 2008.
- "Algorithms and Architectures for Next-Generation Optical Fiber Communications: A New Frontier for Signal Processing", IEEE Conference on Acoustics, Speech and Signal Processing, Las Vegas, NV, March 20-April 4, 2008.
- "Advanced Communications SOC Design", short course (sponsored by the SOC Center) at the National Taiwan University, December 14, 2007.
- "Communications-inspired Paradigm for Reliable and Low-power SOCs in the Nanometer Era", invited talk at the National Dong Hwa University, Hualien, Taiwan, November 30, 2007.
- "Advanced Communication IC Design", invited talk at RealTek, Hsinchu, Taiwan, November 21, 2007.
- "Advanced Communication IC Design", invited talk at MediaTek, Hsinchu, Taiwan, November 21, 2007.
- "A communications-inspired paradigm for reliable and low-power SOCs in the nanometer era", invited talk at the Industrial Technology Research Institute (ITRI), Hsinchu, Taiwan, October 12, 2007.
- "Communications-inspired design of interconnect", invited talk at the IEEE Lasers and Electro-optics Society Workshop on Interconnections within High-Speed Digital Systems, Santa Fe, NM, May 2007.
- "Communications-inspired design of nanometer SOCs", invited talk at Yonsei University, South Korea, Joint UIUC-Yonsei Workshop, February 2007.
- "Fundamentals of Electronic Dispersion Compensation", invited tutorial at the 2007 International Solid-State Circuits Conference, San Francisco, CA, February 11, 2007.
- "Communications-inspired design of nanometer SOCs", invited talk at Cadence Design Systems, Inc.'s Distinguished Lecture Series, February 2007.
- "Robust and energy-efficient design via error-resiliency", invited talk at Texas Instruments, Inc., Dallas, TX, November 2006.
- "Extending Moore's Law: A communications-inspired perspective", invited talk at IBM, Yorktown Heights, NY, October 2006.
- "Communications-inspired design of nanometer SOCs", invited talk at EPFL, Lausanne, September 2006.
- "Communications-inspired Paradigm for Ultra Low-Power Systems", invited talk at DARPA's Extreme Low-power Opportunities Workshop, Washington DC, June 2006.
- "Communications-inspired SOC Design Paradigm for Extending Moore's Law into the Nanometer Regime", invited talk at International Conference on Communications, Circuits and Systems, Guilin, China, June 2006.
- "Communications-inspired Design of Communications ICs", invited seminar at National Taiwan University, Taipei, Taiwan, December 22, 2005.

- "Fundamentals of Communications System-on-a-Chip Design", two-day short course at National Chiao-Tung University, Taiwan, December 23-24, 2005.
- "Extending Moore's Law into the Nanometer Era", invited graduate seminar at University of Minnesota, September 15, 2005.
- "Ultra Low-Power Wireless Systems", invited presentation at DARPA Workshop on Ultra Low-Power Wireless Communications, August 4, 2005.
- "Trusted Integrated Circuits: A Communications Perspective", invited presentation at DARPA Workshop on Trusted ICs, August 1, 2005.
- "Pushing the Limits of Interconnect Performance: A Communication-Centric Approach", invited tutorial at the IEEE Workshop on Signal Propagation on Interconnect, May 10-11, 2005.
- "On Achieving Energy-Efficiency and Soft Error-Tolerance", invited presentation at Intel Corporation, Boston, Massachusetts, March 21, 2005.
- "Reliable and Energy-efficient Computation", invited presentation at the Law of Large Numbers System Design, Institute of Defense Analysis, March 11, 2005.
- "Reliable and Energy-efficient Computation", invited presentation at the Reversible Computing Workshop, MIT, February 14, 2005.
- "Networks-on-a-Chip Design Paradigm", invited presentation at Intel Corporation, Bangalore, India, January 4, 2005.
- "The Networks-on-a-Chip Design Paradigm", invited presentation at Zhejiang University, Hangzhou, China, December 23, 2004.
- "Reliable Systems-on-a-Chip Design", invited presentation at IBM T. J. Watson Research Center, Yorktown Heights, NY, March 19, 2004.
- "Reliable Systems-on-a-Chip Design", invited presentation at National Chiao-Tung University, Taiwan, January 2004.
- "Reliable Systems: A Communication-Theoretic Paradigm" invited presentation at Carnegie-Mellon University, October 2003.
- "Reliable Systems: A Communication-Theoretic Paradigm" presentation at the Gigascale Silicon Research Center Workshop, Anaheim, CA, May 2003.
- "Reliable Low-power Communication Systems", invited presentation at the Indian Institute of Technology, Mumbai, India, December 2002.
- Tutorial at the IEEE Conference on Electronics, Circuits and Systems on "Low-power Microsystems for Multimedia Technology", December 2000.
- Invited to give a plenary talk at the 2001 IEEE Workshop on Signal Processing Systems, Antwerp, Belgium on "Reliable Low-power Multimedia Communication Systems".
- "Low-power Digital Signal Processing", Invited Short Course. Mead Microelectronics. Monterey, CA, March 8, 1999.
- "Multimedia VLSI Communication Systems: Current and Future Trends", IEEE Circuits and Systems Society Distinguished Lecturer Program. Indian Institute of Technology, Delhi, IEEE Chapter of New Delhi, India, October 28, 1999.
- "Low-power multimedia communication systems", National Central University, Taiwan, October 19, 1999.
- "Multimedia VLSI Communication Systems: Current and Future Trends", IEEE Circuits and Systems Society Distinguished Lecturer Program, National Taiwan University, IEEE Chapter of Taipei, Taiwan, October 18, 1999.
- "Low-power multimedia communication systems", University of California at Davis, ECE Department, April 22, 1999.
- "Low-power techniques for next generation wireless systems", University of California at Berkeley, Berkeley Wireless Research Center, April 22, 1999.

Featured Magazine Articles:

- "DARPA Picks its First Set of Winners in Electronic Resurgence Initiative," by S. K. Moore, *IEEE Spectrum*, July 2018.
- "To Speed-up AI, Mix Memory and Processing", by Katherine Bourzac, *IEEE Spectrum*, March 2018.
- "7 Ideas for AI Silicon from ISSCC," by Rick Merritt, *EE Times*, February 2018.
- "Is Subthreshold all that?" by Chris Edwards, *www.electronicsweekly.com*, January 4, 2012.
- "The Era of Error-tolerant Computing", by David Lammers, *IEEE Spectrum*, 2010.
- "Computing without Guarantees", DAC 2010 Roundtable featured in the *IEEE Design and Test of Computers*, September/October 2010.

List of Publications:

- **Books/Monographs**

- M. Kang, S. Gonugondla, and N. R. Shanbhag, *Deep In-memory Architectures for Machine Learning*, Springer, 2020.
- N. R. Shanbhag and K. K. Parhi, *Pipelined Adaptive Digital Filters*. Kluwer Academic Publishers, 1994.

- **Book Chapters**

  - N. Shanbhag, A. Singer, and H.-M. Bae, "Signal processing for High-Speed Links", *Handbook of Signal Processing Systems*, Springer, 2010.
  - A. Ahmed, S.-J. Lee, M. Mansour, and N. R. Shanbhag, "VLSI architectures for Forward Error-Control Decoders", *The VLSI Handbook*, CRC Press, 2007.
  - N. R. Shanbhag, "High-Speed Data Transmission over Twisted-Pair Channels", *Digital Signal Processing for Multimedia Systems*, Marcel Dekker, Inc., 1998.
  - N. R. Shanbhag and K. K. Parhi, "Pipelined Adaptive Digital Filters Using Relaxed Look-ahead", *Microsystems Technology for Multimedia Application: An Introduction*, IEEE Press, 1995.
  - N. R. Shanbhag and K. K. Parhi, "VLSI implementation of a 100 MHz pipelined ADPCM codec chip", *VLSI Signal Processing VI*, IEEE Press, October 1993, pp. 114-122.

- **Journal Publications**

  - C. Sakr and N. R. Shanbhag, "Signal processing methods to enhance the energy efficiency of in-memory computing architectures," *IEEE Transactions on Signal Processing*, DOI: 10.1109/TSP.2021.3130488, 2021.
  - S. Gonugondla, C. Sakr, H. Dbouk, and N. R. Shanbhag, "Fundamental limits on energy-delay-accuracy of in-memory architectures in inference applications," *IEEE Transactions on Computer-Aided Design Integrated Circuits and System*, DOI: 10.1109/TCAD.2021.3124757, 2021.
  - H. Dbouk, S. K. Gonugondla, C. Sakr, and N. R. Shanbhag, "A 0.44 μJ/dec, 39.9 μs/dec, recurrent attention in-memory processor for keyword spotting," *IEEE Journal of Solid-State Circuits*, vol. 56, no. 7, pp. 2234-2244, July 2021.
  - M. Kang, S. K. Gonugondla, and N. R. Shanbhag, "Deep in-memory architectures in SRAM: An analog approach to approximate computing," *Proceedings of the IEEE*, vol. 108, no. 12, pp. 2251-2275, December 2020 (**invited**).
  - M. Kang, Y. Kim, A. Patil, and N. R. Shanbhag, "Deep in-memory architectures for machine learning – accuracy vs. efficiency trade-offs," *IEEE Transactions on Circuits and Systems*, January 2020.
  - M. Kang, P. Srivastava, V. Adve, N.-S. Kim, and N. R. Shanbhag, "An energy-efficient programmable mixed-signal accelerator for machine learning algorithms," *IEEE MICRO*, vol. 39, no. 5, pp. 64-72, September/October 2019.
  - A. D. Patil, S. Manupatruni, D. Nikonov, I. A. Young, and N. R. Shanbhag, "Error-resilient spintronics via Shannon-inspired model of computation," *IEEE Journal on Exploratory Solid-State Computational Devices and Circuits (JxCDC)*, April 2019.
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