

# A NOVEL FORWARD-BACKWARD PREDICTOR BASED LOW-POWER DSP SYSTEM

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## ABSTRACT

In this paper, we present a algorithmic noise tolerance (ANT) technique for low-power digital signal processing systems. The proposed technique employs a low-complexity forward-backward predictor to correct errors in a main DSP (MDSP) block due to *voltage overscaling*, which is an ultra low-voltage operating condition. For a frequency selective FIR filtering, it is shown that the proposed technique achieves up to 43% power savings over an optimally voltage scaled MDSP with a 5% area overhead.

## 1. INTRODUCTION

Growing demand for portable and wireless multimedia applications makes it important to achieve low-power consumption in DSP systems [1, 2]. Frequency selective filtering is a computational kernel commonly employed to reject unwanted frequency bands and to extract the desired input signal. Examples include bandpass filtering, subband decomposition, lowpass filtering for sampling rate conversion, and frequency division multiplexing. Filtering consumes a significant portion of total power consumption. Therefore, low-power filtering in these applications is of great interest.

Previously, we have shown that algorithmic noise tolerance (ANT) techniques combined with voltage overscaling (VOS) are effective in achieving low-power consumption [3]-[5] in digital filtering. VOS reduces power of the MDSP block dramatically but introduces timing errors at its output. A low-complexity estimator corrects these errors effectively thereby achieving low-power operation. The forward prediction (FP) based ANT [3] technique employs a low complexity forward predictor to estimate the current output  $y_o[n]$  of the MDSP block from the past outputs  $y_o[n-k]$ ,  $k > 0$ . Prediction is feasible since the adjacent outputs of a narrowband MDSP are highly correlated.

In this paper, we present an extension of the technique in [3] referred to as the forward-backward prediction (FBP) based ANT technique. The forward-backward predictor results in significantly improved performance. This paper is organized as follows. After briefly discussing FP ANT technique in Section 2, we present the FBP ANT technique in Section 3. Simulation results and discussion are given in Section 4.

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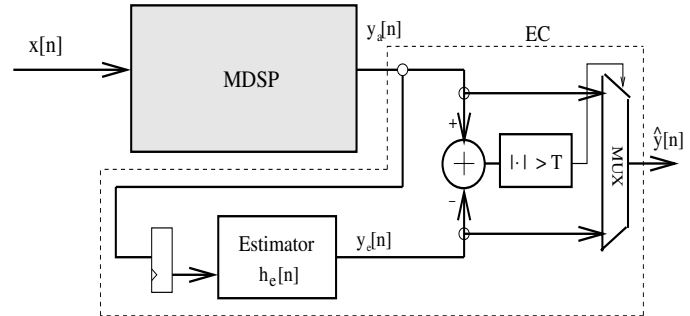


Fig. 1. The original FP ANT technique.

## 2. FP ANT

The FP ANT technique [3] exploits the correlation between output samples of a narrowband MDSP block. Thus, a linear forward predictor  $h_p[n]$  can produce an estimate  $y_p[n]$  of the MDSP output  $y_o[n]$ . Figure 1 shows the block diagram of the FP ANT technique where the output of the estimator  $y_p[n]$  is compared to the MDSP output  $y_o[n]$ .

The output of an  $N_p$ -tap forward predictor is given by

$$y_p[n] = \sum_{k=0}^{N_p-1} h_p[k] y_o[n-k-1] = \mathbf{H}^T \mathbf{Y} \quad (1)$$

where  $\mathbf{Y}$  and  $\mathbf{H}$  are the past output vector of the MDSP block and the predictor coefficient vector, respectively, as shown below

$$\mathbf{Y} = [y_o[n-1], \dots, y_o[n-N_p]]^T \quad (2)$$

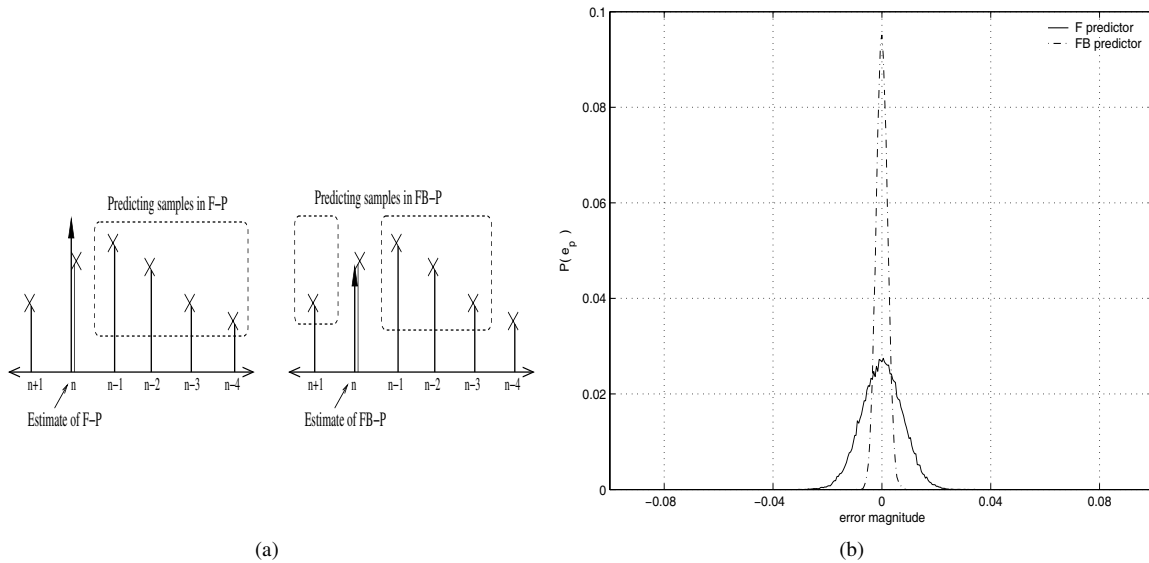
$$\mathbf{H} = [h_p[0], \dots, h_p[N_p-1]]^T. \quad (3)$$

The optimal coefficient vector minimizing the mean square error (MSE) is the well-known Wiener-Hopf solution given by [6]

$$\mathbf{H} = \mathbf{R}^{-1} \mathbf{P} \quad (4)$$

where  $\mathbf{P}^T = E[y_o[n] \mathbf{Y}^T]$  and  $\mathbf{R} = E[\mathbf{Y} \mathbf{Y}^T]$ .

The predicted output  $y_p[n]$  and actual MDSP output  $y_o[n] = y[n] + \gamma[n]$  in the presence of noise  $\gamma[n]$  are compared. In the absence of errors in the MDSP block, i.e., when  $y_o[n] = y[n]$ , the Euclidean distance  $d(y_o[n], y_p[n]) = |y_o[n] - y_p[n]|$  is the prediction error  $|e[n]|$ . However, in presence of an error with large



**Fig. 2.** The principle of the proposed FBP ANT technique: (a) predicting samples, and (b) *pdf* of prediction noise.

magnitude,  $d(y_a[n], y_p[n]) = |\gamma[n] + e[n]|$  is greater than a pre-defined threshold  $T_h$  accomplishing error detection. On the detection of an error,  $y_p[n]$  is used as a corrected output accomplishing error correction. The decision rule for the FP ANT technique is given by

$$\hat{y}[n] = \begin{cases} y_a[n] & \text{if } d(y_a[n], y_p[n]) \leq T_h \\ y_p[n] & \text{if } d(y_a[n], y_p[n]) > T_h \end{cases} \quad (5)$$

where  $T_h$  is a precomputed threshold satisfying the Neyman-Pearson criterion [7] given by

$$T_h = \arg \min_T [P_r(|y[n] - y_p[n]| > T) \leq P_{fer}]. \quad (6)$$

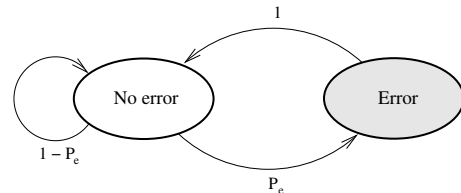
where  $P_{fer}$  is the false alarm probability. As the MDSP output feeds into the predictor input, it is evident that the predictor output will be in error for  $N_p$  samples. To resolve this issue, one can disable the error control mechanism or use the same corrected output  $y_p[n]$  for the next  $N_p$  cycles. Either way approach degrades the performance considerably.

### 3. THE FBP ANT TECHNIQUE

In this section, we present the FBP ANT technique for improving the error detection and correction accuracy. Fig. 2 motivates the new technique. For a 4-tap predictor, the FP ANT technique employs  $y[n-4]$  to predict  $y[n]$  while the proposed FBP ANT technique employs  $y[n+1]$  (see Fig. 2(a)). As shown in Fig. 2(b), the distribution of prediction noise  $e[n] = y[n] - y_p[n]$  is narrower for the FBP technique than the FP technique. Thus, the FBP technique provides much more accurate predictions than the FP technique because the distributions are centered around zero. Next, we describe the proposed FBP ANT and then present a performance analysis.

#### 3.1. The FBP ANT Technique

The error model for FBP ANT is shown in Fig. 3 where  $P_e$  is the probability of error at the MDSP output, and the two states indicate



**Fig. 3.** Error model for the FBP ANT technique.

if the error status of the MDSP output. We assume that the probability of two consecutive errors is very small. This assumption is true if the error rate  $P_e \ll 1$  and it simplifies the error control technique. We begin by assuming (see Fig. 4) that all the components of the prediction vector  $\mathbf{Y}_{fb} = [y[n+1], y[n-1], \dots, y[n-N_p+1]]$  and predicted output  $y_a[n]$  are error-free initially. The  $N_p$ -tap forward-backward predictor generates  $y_p[n]$  as follows

$$y_p[n] = \sum_{k=-1, k \neq 0}^{N_p-1} h_p[k] y[n-k] \quad (7)$$

where  $h_p[k]$  is given by (4). Next, we compare the Euclidean distance  $d(y_p[n], y_a[n])$  to a pre-specified threshold  $T_h$ . Note that  $y_a[n]$  and  $y_a[n-k], k > 0$  are error-free. Hence, if an error is detected, i.e.,  $d(y_p[n], y_a[n]) > T_h$  then the only conclusion that can be derived is that  $y_a[n+1]$  is erroneous. The next output  $y_a[n+2]$  will be error-free because of our assumption that two consecutive errors are very unlikely to occur. Thus, we employ  $\mathbf{Y}_{fb} = [y_a[n+2], y_a[n], \dots, y_a[n-N_p+2]]$  to compute  $y_p[n+1]$  which then is employed as the corrected value of  $y_a[n+1]$ . For subsequent predictions, we employ the corrected value of  $y_a[n+1]$ . This algorithm is summarized in Table 1.

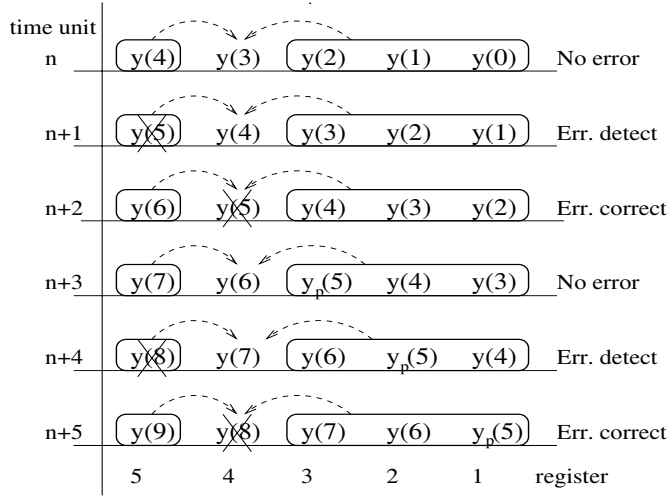


Fig. 4. Illustration of error control in F-B predictor.

Table 1. The FBP ANT Algorithm

Step	Procedure
1.	At $n = 0$ , initially reset error flag $er = 0$
2.	Increase $n$ by 1. Generate $\mathbf{Y}_{fb}$ using $y_a[n+1]$ and $N_p - 1$ latest $y_a[n-k]$ samples ( $k > 0$ ). Compute FB-P output $y_p[n]$ by using (7).
3.	If previous decision was an error, ( $er = 1$ ), then $\hat{y}[n] = y_p[n]$ .
4.	Else $\hat{y}[n] = y_o[n]$ If $d(y_p[n], y_a[n]) > T_h$ then $er = 1$ . else $er = 0$ .
5.	Go to step 2.

### 3.2. The FBP ANT Architecture

The Fig. 5 shows the proposed FBP architecture. In addition to the MDSP block, a forward-backward predictor is employed for generating an estimate of the MDSP output. A delay unit is employed at the output of the MDSP block in order to maintain causality. In that case,  $y[n-2]$  becomes the predicted sample and  $y[n-1]$ ,  $y[n-j]$ ,  $j = 3, \dots, n+1$  contribute to the computation of  $y_p[n-2]$ . For effective error control, the FBP ANT technique should satisfy following two conditions: 1) errors should be spaced apart by at least two samples, and 2) the predictor should be error free. Notice that these conditions are easily satisfied when  $P_e \ll 1$  and the critical path in the predictor is shorter than that of the MDSP block.

### 3.3. Residual Noise Power Analysis

We study the impact of the FBP ANT technique on the signal-to-noise ratio  $SNR$  of voltage overscaled frequency selective filters. Voltage overscaling (VOS) refers to the reduction of supply voltage beyond  $V_{dd-crit}$ , without sacrificing the throughput, where  $V_{dd-crit}$  is the supply voltage below which errors due to timing violations appear, i.e.,

$$V_{dd} = K_{vos} V_{dd-crit}, \quad 0 \leq K_{vos} < 1, \quad (8)$$

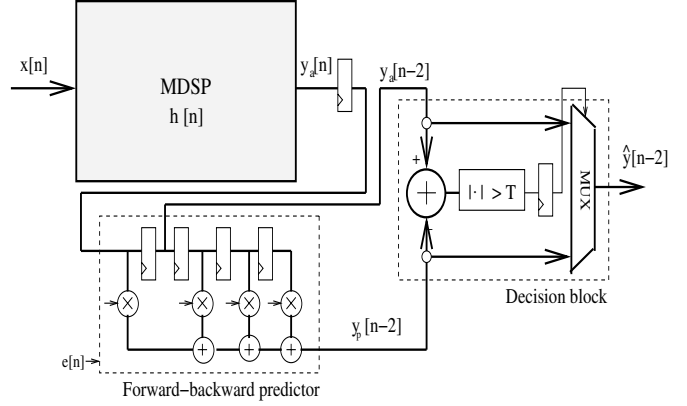


Fig. 5. Forward-backward predictor structure.

where  $K_{vos}$  is referred to as the VOS factor (VOSF). Under VOS, the critical path delay  $T_{cp}$  becomes greater than the sample period  $T_{samp}$  resulting in output errors occur whenever paths with delays longer than  $T_{samp}$  are excited. Most significant bit (MSB) errors appear first since arithmetic units typically are based on least significant bit (LSB) first computation.

A  $l+1$  bit representation of an error-free MDSP output  $y_o[n]$  in two's complement representation is given by

$$y_o[n] = -b_0 + \sum_{i=1}^l b_i 2^{-i}. \quad (9)$$

In contrast, the output of MDSP in the presence of errors is given by

$$y_a[n] = -\tilde{b}_0 + \sum_{i=B}^l \tilde{b}_i 2^{-i} + \sum_{i=1}^{B-1} b_i 2^{-i}. \quad (10)$$

where  $\tilde{b}_i$  are the erroneous bits and  $B$  is the lowest order bit in error. Figure 6 shows that the delay of each output bit in an  $8 \times 8$  bit Baugh-Wooley multiplier increases with reduction in supply voltage from its nominal value of 1.8V for a 0.18 $\mu$ m CMOS process. Also, it is clear that  $B$  decreases with  $K_{vos}$ . For example, there are no output bits in error at a nominal supply of  $V_{dd} = 1.8$  and when the sample period is  $4n_s$ . However, when  $V_{dd} = 1.44$ ,  $B = 14$ , which means that the top three MSBs can be in error. Further, when  $V_{dd} = 1.08$ , the top seven MSBs can be in error or  $B = 10$ . From (9) and (10), the actual MDSP output  $y_a[n]$  can be written as

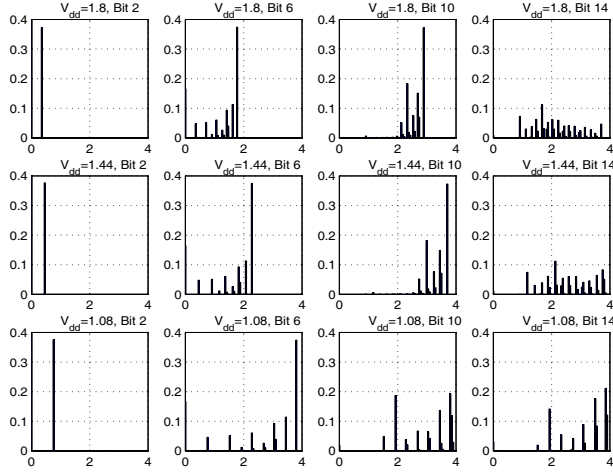
$$y_a[n] = y[n] + \gamma[n] = y[n] + \theta[n] 2^{B-l-1} \quad (11)$$

where  $\theta[n] \in \{-(2^{l-B+2} - 1), \dots, 2^{l-B+2} - 1\}$ .

The corrected output  $\hat{y}[n]$  in FBP ANT technique is written as

$$\hat{y}[n] = y_o[n] + \gamma_r[n] \quad (12)$$

where  $\gamma_r[n]$  is the residual error after error correction which can take values 0,  $\gamma[n]$ , or  $e[n]$ . The residual mean square error (rMSE)



**Fig. 6.** The delay distribution of  $8 \times 8$  signed Baugh-Wooley multiplier for various output bit position at various supply voltages (x-axis is nsec, y-axis is prob.).

is given by

$$\begin{aligned}
E[|Y_o - \hat{Y}|^2] &= \int (y_o - \hat{y})^2 f(y_o, \hat{y}) dy_o d\hat{y} \\
&= \int_{|y_o - y_p| < T_h} \underbrace{(y_o - y_o)^2}_0 f(y_o, y_p) dy_o dy_p \quad (\text{No error}) \\
&+ \int_{|y_a - y_p| < T_h} (y_o - y_a)^2 f(y_o, y_a) dy_o dy_a \quad (\text{Undetected error}) \\
&+ \int_{|y_o - y_p| > T_h} (y_o - y_p)^2 f(y_o, y_p) dy_o dy_p \quad (\text{False alarm}) \\
&+ \int_{|y_a - y_p| > T_h} (y_o - y_p)^2 f(y_o, y_p) dy_o dy_p \quad (\text{Detected error})
\end{aligned}$$

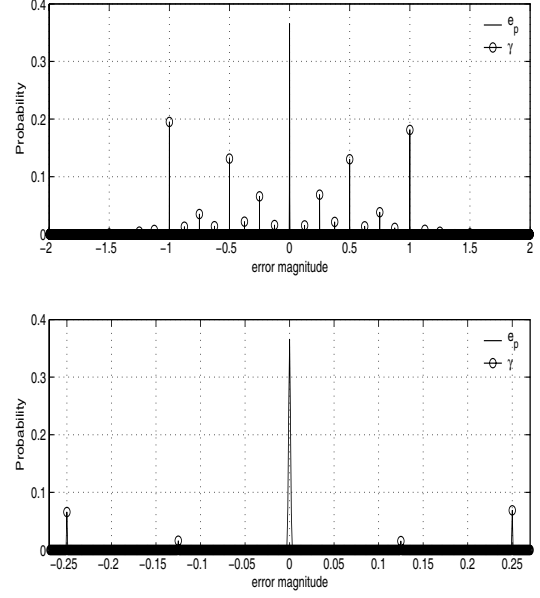
Recalling that  $e[n] = y_o[n] - y_p[n]$ ,  $\gamma[n] = y_a[n] - y_o[n]$ , and employing the statistical independence between  $e[n]$  and  $\gamma[n]$ , rMSE can be rewritten as

$$\begin{aligned}
E[|Y_o - \hat{Y}|^2] &= \sum_{\gamma} P_r(\gamma) \gamma^2 \int_{|\gamma+e| < T_h} f(e) de \\
&+ \int_{|e| > T_h} e^2 f(e) de + \sum_{\gamma} P_r(\gamma) \int_{|\gamma+e| > T_h} e^2 f(e) de \quad (13)
\end{aligned}$$

Integrating by parts, we obtain the power of undetected errors  $\sigma_{uer}^2$  as follows:

$$\begin{aligned}
\sigma_{uer}^2 &= \sum_{\gamma} P_r(\gamma) \gamma^2 \int_{|\gamma+e| < T_h} f(e) de \\
&= \sum_{\gamma} P_r(\gamma) \gamma^2 \left[ 1 - Q\left(\frac{T_h - \gamma}{\sigma_e}\right) - Q\left(\frac{T_h + \gamma}{\sigma_e}\right) \right] \quad (14)
\end{aligned}$$

where  $Q(x) = \int_x^{\infty} \frac{1}{\sqrt{2\pi}} \exp(-\frac{x^2}{2}) dx$ . In a similar way, the



**Fig. 7.** The distribution of VOS error and the prediction noise for  $l=15$ ,  $B=10$ bit (bottom is the picture zoomed around 0).

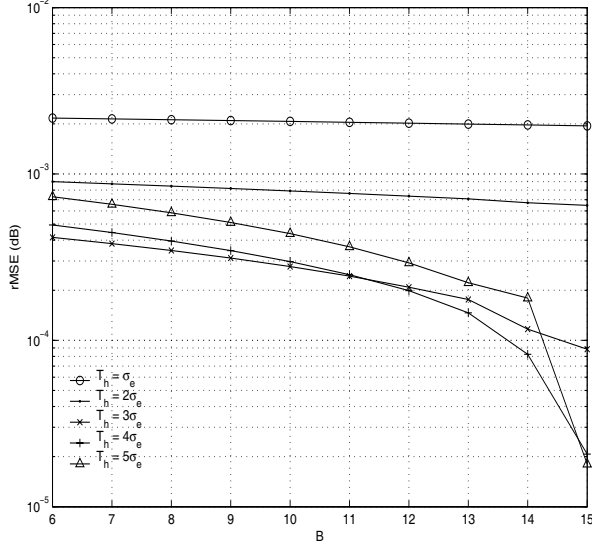
power of false alarm error  $\sigma_{fer}^2$  can be obtained as

$$\begin{aligned}
\sigma_{fer}^2 &= \int_{|e| > T_h} e^2 f(e) de \\
&= 2\sigma_e T_h G\left(\frac{T_h}{\sigma_e}\right) + 2\sigma_e^2 Q\left(\frac{T_h}{\sigma_e}\right) \quad (15)
\end{aligned}$$

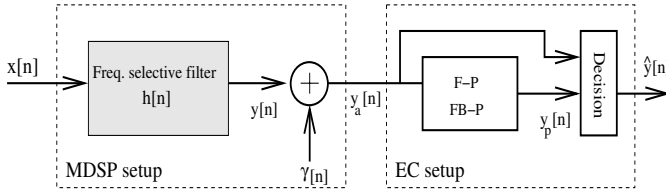
where  $G(x) = \frac{1}{\sqrt{2\pi}} \exp(-\frac{x^2}{2})$ . Finally, the power of detected error  $\sigma_{der}^2$  is given by

$$\begin{aligned}
\sigma_{der}^2 &= \sum_{\gamma} P_r(\gamma) \int_{|\gamma+e| > T_h} e^2 f(e) de \quad (16) \\
&= \sigma_e^2 \sum_{\gamma} P_r(\gamma) \left[ Q\left(\frac{T_h - \gamma}{\sigma_e}\right) + Q\left(\frac{T_h + \gamma}{\sigma_e}\right) \right] \\
&+ \frac{T_h - \gamma}{\sigma_e} G\left(\frac{T_h - \gamma}{\sigma_e}\right) + \frac{T_h + \gamma}{\sigma_e} G\left(-\frac{T_h + \gamma}{\sigma_e}\right)
\end{aligned}$$

We can deduce from the result of analysis that the residual error power depends on  $T_h$ . Further, the terms  $G(x)$  and  $Q(x)$  in (14) and (16) approach zero rapidly for large values of  $B$  because the value of  $\gamma[n]$  will be large. For example, in Fig. 7, the standard deviation of  $\gamma$  is much larger than that of the estimation error  $e[n]$  so that most errors are detected and hence  $\sigma_{uer}^2 \sim 0$ ,  $\sigma_{der}^2 \sim \sigma_e^2$ . Thus, the best performance can be obtained with a large value of  $T_h$  such as  $T_h \sim 5\sigma_e$  as shown in Fig. 8). However, for small values of  $B$ , the minimum values of  $\gamma$  becomes smaller and hence probability of undetected error increases. In this case,  $T_h$  should be determined carefully. If  $T_h$  is chosen to be too small, e.g.,  $T_h \sim \sigma_e$  in Fig. 8) then  $\sigma_{fer}^2$  dominates. On the other hand, if  $T_h$  is too large, e.g.,  $T_h \sim 5\sigma_e$  then  $\sigma_{uer}^2$  dominates. Given these trade-offs, we find that  $T_h \sim 3\sigma_e$  is a good value.



**Fig. 8.** rMSE analysis results for FBP ANT with respect to  $B$  with  $l = 15$ , a 32-tap LPF, and a 4-tap forward-backward predictor).



**Fig. 9.** Simulation setup for F-B predictor based ANT.

## 4. DISCUSSION AND SIMULATION RESULTS

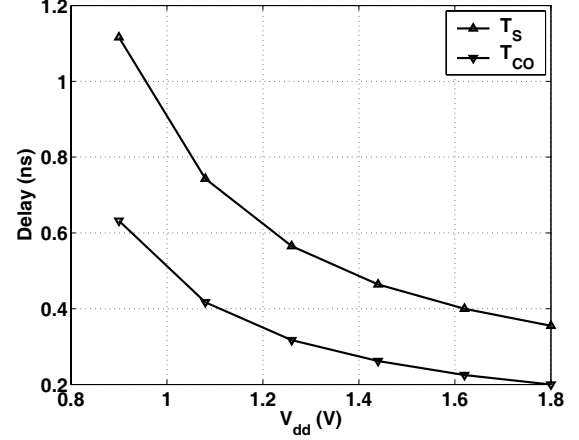
### 4.1. Simulation Setup

The setup employed to measure the  $SNR$  of the proposed technique is shown in Fig. 9, where a frequency selective filter  $h[n]$  is employed to generate a bandlimited signal  $y[n]$  from a narrowband input with Gaussian noise  $x[n] = d[n] + \eta[n]$ .

In the simulation, we design a 32-tap MDSP filter with a MAC unit consisting of a  $16 \times 16$  multiplier and a 33-bit accumulator. The length of the forward-backward predictor is  $N_p = 4$  taps with a  $8 \times$  slower clock, which guarantees that it will be error-free. These blocks are designed via event-driven Simulink schematic and the delay of each building block (adder and latch) is obtained

**Table 2.** Simulation parameters for the proposed FB-P ANT.

System	Specifications
Filter bandwidth	BPF with $0.2\pi - 0.4\pi$
Filter spec.	32-tap Parks-McClellan FIR
Desired output SNR	25 dB
Multiplier in MDSP MAC	$16 \times 16$
Accumulator in MDSP MAC	31+2 guard bits
Multiplier in FB-P MAC	$8 \times 8$
Accumulator in FB-P MAC	15+2 guard bits



**Fig. 10.** Full adder delay as a function of supply voltage in  $0.18 \mu\text{m}$  CMOS technology.

via HSPICE circuit simulation employing  $0.18 \mu\text{m}$  CMOS technology (see Fig. 10). The simulation parameters are summarized in Table 2.

### 4.2. Experimental Results

The dynamic power dissipation of the original MDSP at  $V_{dd-crit}$  is given by [8]

$$P_{org} = C_L V_{dd-crit}^2 f_{clk} \quad (17)$$

where  $C_L$  is the effective switching capacitance of MDSP and  $f_{clk}$  is the clock frequency. The dynamic power dissipation of FBP ANT is given by

$$P_{fbp} = C_L (K_{vos} V_{dd-crit})^2 f_{clk} + C_{fb} (K_{vos} V_{dd-crit})^2 \frac{f_{clk}}{N} \quad (18)$$

where  $C_{fb}$  is the effective switching capacitance of the predictor and decision block and  $N$  is the ratio of clock frequency between the predictor and the MDSP block. From (17) and (18), the power savings  $P_{sav}$  of the proposed FBP ANT is given by

$$\begin{aligned} P_{sav} &= \frac{P_{org} - P_{fbp}}{P_{ref}} \\ &= (1 - K_{vos})^2 - \frac{C_{fb}}{C_L} \frac{K_{vos}^2}{N} \end{aligned} \quad (19)$$

Note that  $C_L \gg C_{fb}$ ,  $K_{vos} < 1$  and  $N > 1$  indicating that significant power savings will occur.

In our simulations, we modified the delay of arithmetic units for every value of  $K_{vos}$  and performed simulations for 50,000 input vectors in each case. The output  $SNR$  of the FBP ANT technique is given by

$$SNR_{fbp} = 10 \log_{10} \frac{\sigma_d^2}{\sigma_{d-\hat{y}}^2} \quad (20)$$

The output  $SNR$  at  $K_{vos} = 1$ , i.e., error-free MDSP, is 25.5 dB. Figure 11 shows the output  $SNR$ s for the proposed FBP ANT, FP ANT [3], and MDSP without any error control. We see that the output  $SNR$  in the absence of error control drops dramatically, i.e., by more than 24dB as  $K_{vos}$  decreases from 1.0 to 0.9. The

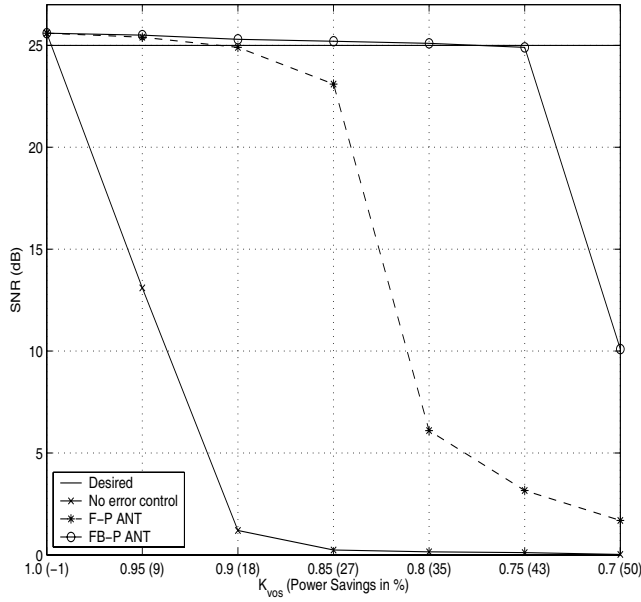


Fig. 11. SNR of proposed technique vs. power savings.

SNR of FP ANT [3] drops as  $K_{vos} < 0.9$  and does not achieve the desired performance at  $K_{vos} \leq 0.85$ . However, with proposed FBP ANT technique achieves an SNR loss that is less than 0.4 dB until  $K_{vos}$  approaches 0.75. The power savings of the proposed FBP ANT technique at  $K_{vos} = 0.75$  is about 43%.

### 4.3. Synthesized Circuits

In order to observe the area overhead of the proposed system over the conventional system, we synthesized layouts for both systems in  $0.18\mu\text{m}$  CMOS process technology. The design parameters are summarized in Table 2. The MAC unit is designed using VHDL and synthesized via *Synopsys Design Analyzer* and *Cadence Silicon Ensemble*. Figure 12 shows the synthesized layouts of the MAC units for the conventional and proposed systems. We define the area overhead  $\rho$  of the proposed scheme over the conventional filter as:

$$\rho = \left( \frac{A_{prop}}{A_{org}} - 1 \right) \times 100\% \quad (21)$$

Substituting  $A_{prop} = 0.1637\text{mm}^2$  and  $A_{org} = 0.1557\text{mm}^2$ , we obtained the area overhead of proposed technique as 5.1%.

## 5. REFERENCES

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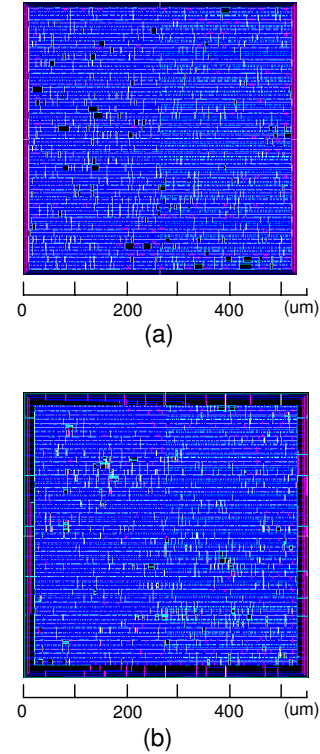


Fig. 12. Synthesized layout of MAC for: (a) original system, (b) proposed scheme.

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