The Twin-Transistor Noise-Tolerant Dynamic Circuit Technique

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Abstract—This paper describes a new circuit technique for designing noise-tolerant dynamic logic. It is shown that voltage scaling aggravates the crosstalk noise problem and reduces circuit noise immunity, motivating the need for noise-tolerant circuit design. In a 0.35-μm CMOS technology and at a given supply voltage, the proposed technique provides an improvement in noise immunity of $1.8\times$ (for an AND gate) and $2.5\times$ (for an adder carry chain) over domino at the same speed. A multiply–accumulate circuit has been designed and fabricated using a 0.35-μm process to verify this technique. Experimental results indicate that the proposed technique provides a significant improvement in the noise immunity of dynamic circuits ($>2.4\times$) with only a modest increase in power dissipation (15%) and no loss in throughput.

Index Terms—CMOS integrated circuits, crosstalk, dynamic circuits, noise, noise-tolerant design.

I. INTRODUCTION

THE RELENTLESS scaling of device and interconnect dimensions has caused noise to become an increasingly important issue in integrated circuit design. Deep-submicron noise is the general term used to designate any phenomenon that causes the voltage at a nonswitching node to deviate from its nominal value [1]. It thus includes [2] power-supply noise caused by circuit switching, crosstalk noise due to capacitive coupling between neighboring interconnects, and fluctuations in device parameters due to process variations [3]. For high-speed dynamic logic circuits, charge-sharing and leakage [4] are additional noise sources. While these noise phenomena have always existed, it is only recently that technology scaling and aggressive design practices have brought them to the forefront.

In this paper, we will restrict our attention to dynamic logic circuits, which are commonly used in high-speed circuits, and are most susceptible to noise. Also, we define noise to be a pulse/glitch that appears at the inputs of dynamic gates and discharges the dynamic node. Figs. 1 and 2 show several possible ways this can occur. The term *input noise* will be used to designate this type of noise.

Crosstalk noise between interconnects is the most common source of input noise. This effect is expected to become increasingly significant with the growing interconnect aspect ratios [5], that lead to a larger fraction of the wire capacitance being due to lateral coupling capacitance. In the next section, we present some analysis and simulation results to show that voltage scaling aggravates the crosstalk noise problem. The increased sensitivity to input noise caused by voltage scaling needs to be addressed by using special noise-tolerant circuit techniques. Section III briefly reviews existing techniques for noise-tolerant dynamic circuit design. In Section IV, a new noise-tolerant circuit technique is described. Section V discusses the design of a pipelined MAC test IC and experimental results showing the improvement in noise immunity and the penalty in terms of power dissipation.

II. IMPACT OF $(V_{dd}, V_{\rm T})$ SCALING ON CROSSTALK NOISE

A very popular low-power strategy is the scaling of the supply voltage [6]–[9]. One can obtain large savings in power using this approach, due to the quadratic dependence of dynamic power dissipation on V_{dd}. However, for this to be practical, another technique that compensates for the increased delay needs to be employed concurrently. One way to achieve this compensation is to use reduced threshold voltages [10]. Using the alpha power law model [11], the following expression for delay τ_d can be obtained:

$$\tau_d \propto \frac{C_L \cdot V_{dd}}{(V_{dd} - V_{\rm T})^\alpha} \tag{1}$$

where C_L is the capacitance that is switched, V_{dd} and $V_{\rm T}$ are the supply and transistor threshold voltages, respectively, and α is the velocity saturation index that assumes a value close to 2 for long-channel transistors. For shorter channel lengths, however, α is close to 1 due to velocity saturation [12]. For simplicity, we will assume that $\alpha = 1$ in the following analysis.

Let the unscaled voltages be denoted by $V_{dd_{\rm U}}$, $V_{\rm T_U}$ and the scaled voltages be denoted by $V_{dd_{\rm S}}$, $V_{\rm T_S}$. From (1), in order to achieve the same delay after voltage scaling, the following equation must be satisfied:

$$\frac{V_{\rm T_U}}{V_{dd_{\rm U}}} = \frac{V_{\rm T_S}}{V_{dd_{\rm S}}} = r. \tag{2}$$

Thus, the ratio $V_{\rm T}/V_{dd}$ should be constant. To determine the impact of this type of voltage scaling on crosstalk noise, let us consider the circuit model for a typical crosstalk scenario shown in Fig. 2, where we have a domino gate whose input is strongly coupled to a neighboring wire, while the voltage at the input node is being held nominally at ground.
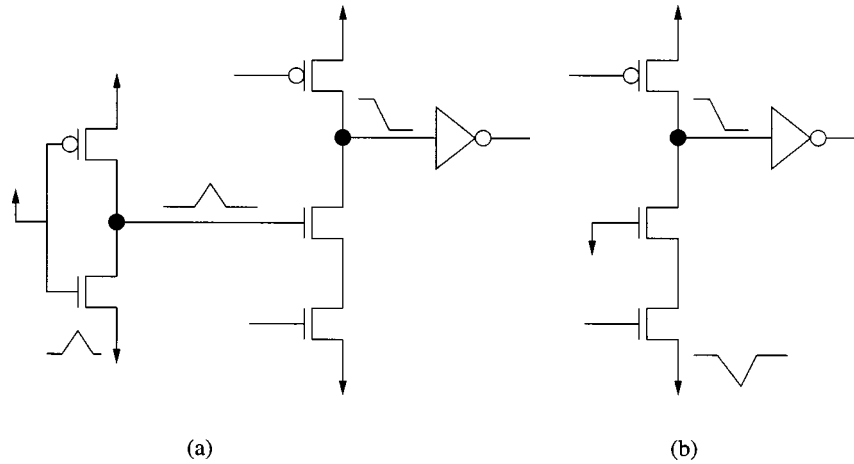
Fig. 1.   Input noise caused by ground bounce. (a) Above 0 V. (b) Below 0 V.

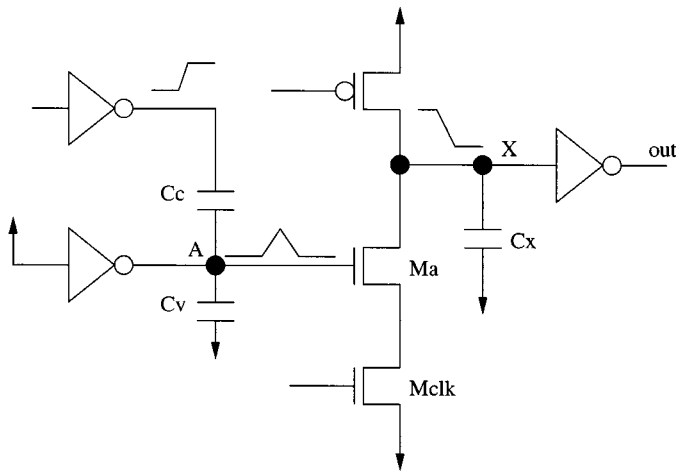Fig. 2.   Circuit model used to obtain the behavior of crosstalk noise with voltage scaling and its effect on dynamic logic circuits.
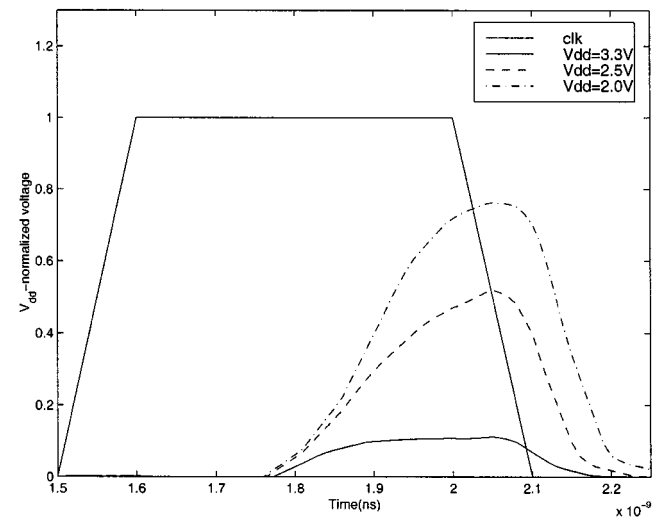

Fig. 3.   HSPICE simulation results showing the V_{dd}-normalized waveforms at the output of a two-input domino AND gate subjected to crosstalk noise, for three (V_{dd}, V_{T}) combinations that achieve the same delay. The model shown in Fig. 2 is used with $C_c = 20$ fF and $C_v = 10$ fF. Transistor parameters for the 0.35-μm process HPCMOS10QA were used in the simulations.

If $V_{\mathrm{N}}(t)$ is the noise pulse at the input node, and C_x is the dynamic node capacitance, we have

$$C_x \cdot \frac{dV_x}{dt} \approx k \cdot (V_{\mathrm{N}}(t) - V_{\mathrm{T}}) \qquad (3)$$

where we have assumed a negligible on-resistance of Mclk, and that the transistor Ma is in saturation. This will result in a slight overestimation of the voltage drop at the dynamic node due to input noise, but simulation results show that (3) correctly predicts the qualitative behavior of input noise under the above low-power strategy. From (3), we find that the voltage degradation of the dynamic node due to input noise is proportional to the average current due to input noise denoted by $I_{\mathrm{n, ave}}$.

$$I_{\mathrm{n, ave}} \propto \int (V_{\mathrm{N}}(t) - V_{\mathrm{T}}) \cdot dt \qquad (4)$$

where the integration is performed over the time interval when $V_{\mathrm{N}}(t) > V_{\mathrm{T}}$ (subthreshold conduction is assumed to be negligible). We will henceforth refer to $I_{\mathrm{n, ave}}$ as the noise current.

In order to determine the dependence of the noise current $I_{\mathrm{n, ave}}$ on V_{dd}, let us consider the simple case of a step waveform

at the aggressor. If the buffer driving the input A is modeled as a resistor R_v to ground, the input noise is given by

$$V_{\mathrm{N}}(t) = k_c \cdot V_{dd} \cdot e^{-t/\tau_c} \qquad (5)$$

where $\tau_c = R_v \cdot (C_c + C_v)$ and $k_c = C_c/(C_c + C_v)$, C_c is the (lumped) coupling capacitance, and C_v is the capacitance to ground at the victim node A.

Substituting (5) in (4), we obtain

$$I_{\mathrm{n, ave}} \propto \tau_c \left(k_c \cdot V_{dd} - \left(1 + \ln \frac{k_c V_{dd}}{V_T}\right) \cdot V_T \right). \qquad (6)$$

Assuming R_v is inversely proportional to $(V_{dd} - V_{\mathrm{T}})$ and employing (2), we have

$$I_{\mathrm{n, ave}} \propto \frac{k_c - r \cdot \left(1 + \ln \dfrac{k_c}{r}\right)}{1 - r}. \qquad (7)$$

All terms in this equation are independent of V_{dd} and V_{T}. Thus, we see that the noise current $I_{\mathrm{n, ave}}$ stays approximately constant
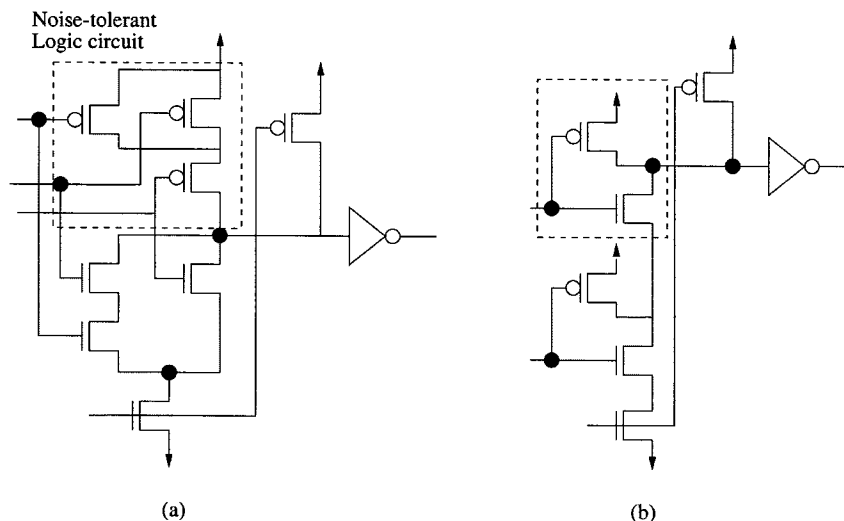
Fig. 4. Techniques to improve the noise immunity of dynamic circuits using (a) a weak and/or incomplete pMOS network for skewed static operation (NTP), and (b) pMOS transistors at gate inputs.

with voltage scaling. Note that although the peak noise value scales with the supply voltage, the input noise pulse width also increases with voltage scaling (due to the larger pulldown resistance shunting C_v). These two effects balance each other to give a constant noise current.

Let I_{crit} be defined as the value of $I_{\mathrm{n,ave}}$ required to bring the voltage of the dynamic node below the inverter threshold $V_{\mathrm{th,inv}}$ and cause false switching. Thus I_{crit}, which is a measure of the noise margin, is proportional to V_{dd} and decreases as V_{dd} is reduced. From (3)

$$I_{\mathrm{crit}} \propto (V_{dd} - V_{\mathrm{th,inv}}) \propto V_{dd}. \qquad (8)$$

Thus the tolerable noise current I_{crit} decreases with voltage scaling while the actual noise current remains constant. Together, these facts imply an increased sensitivity of dynamic circuits to input crosstalk noise at lower voltages. Simulation results corroborate the conclusions drawn from the above analysis using first-order models. Fig. 3 shows the effect of crosstalk noise at the output of the domino gate for three different (V_{dd}, V_{T}) combinations that achieve the same delay. Transistor parameters from the MOSIS 0.35-μm process HPCMOS10QA were used in the simulations. The coupling capacitance is 20 fF, and C_v is about 10 fF. We can conclude that the impact of input crosstalk noise becomes greater at the lower supply voltages. However, operating at these low voltages is desirable from a low-power perspective—hence the need for energy-efficient noise-tolerant circuit techniques.

III. Noise-Tolerant Dynamic Circuit Design—Existing Techniques

The switching threshold of a dynamic logic gate is approximately V_{T}, the transistor threshold voltage. For a 0.35-μm MOSIS process, this is about 0.6 V, and may not be adequate to prevent false switching due to input crosstalk noise. Upsizing the keeper transistor to trade off performance for noise immunity is a commonly used technique in dynamic circuit design.
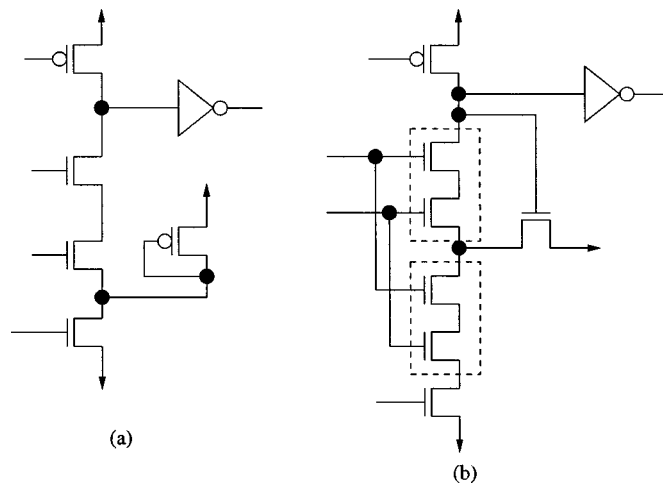

Fig. 5. Existing techniques to improve the noise immunity of dynamic logic circuits using (a) a pMOS pull-up transistor, and (b) a mirror nMOS network.

Several other techniques have also been proposed to increase this threshold [13]–[16].

Fig. 4(a) shows the noise-tolerant precharge (NTP) circuit technique described in [13]. A weak and/or incomplete pMOS pullup logic is used to provide quasistatic operation and avoid floating nodes. While this circuit is faster than static CMOS due to the small sizes of pMOS transistors, it increases the input capacitance and also has nonnegligible short-circuit current. Fig. 4(b) shows the CMOS inverter technique proposed in [14] that uses additional pMOS transistors at the gate inputs to adjust the switching threshold. However, this technique is not suitable for OR/NOR type logic. Fig. 5(a) shows the *pMOS pull-up technique* [15] that increases the switching threshold by an amount depending on the size of the pMOS pull-up device. This technique however suffers from static power dissipation.

Another noise-tolerance technique, which we will refer to as the *mirror technique*, has been proposed recently [17]. A two-input AND gate implemented using this technique is shown in Fig. 5(b). This technique uses the principle of a Schmitt trigger to increase the dynamic switching threshold using a
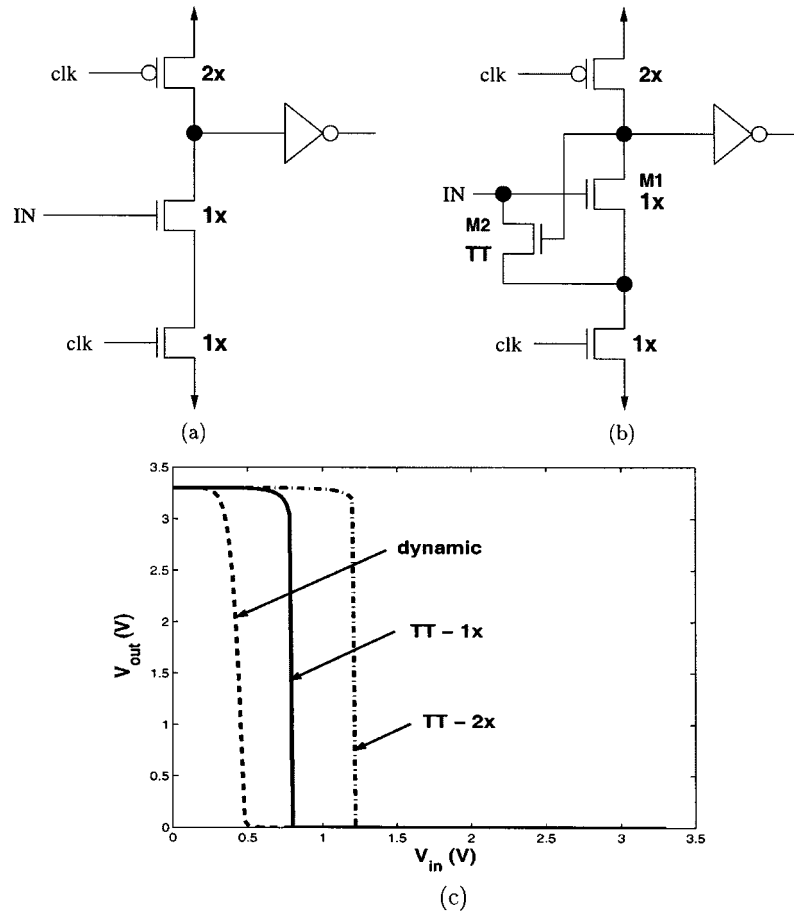
Fig. 6.   A simple buffer implemented using (a) conventional domino, and (b) twin transistors. The dc transfer characteristics are shown in (c) for the conventional circuit and the twin transistor circuit for two different sizes of $M2$ in multiples of $(W/L)_{\min} = (0.6~\mu\mathrm{m}/0.4~\mu\mathrm{m})$. A weak keeper $((W/L) = (0.6~\mu\mathrm{m}/1.2~\mu\mathrm{m})$ used in obtaining these results is not shown in (a), (b).

mirror nMOS network. It was shown in [17] that the mirror technique provides the highest noise immunity per unit energy consumed. Variations of this technique involve simplifications of the upper or lower nMOS networks so that there is just one additional transistor per series path.

In order to compare the performance of various noise-tolerance techniques, we will use a noise-immunity curve as shown in Fig. 15. This curve is the locus of noise amplitude (V_{noise}) and width (T_{noise}) combinations that cause a gate to switch. To encapsulate the information in the plot, we use a noise metric—average noise threshold energy (ANTE)—proposed in [17]. ANTE is defined by

$$\mathrm{ANTE} = E\left(V_{\mathrm{noise}}^{2} \cdot T_{\mathrm{noise}}\right) \qquad (9)$$

where $E()$ denotes the average value.

IV. TWIN-TRANSISTOR TECHNIQUE

The twin-transistor technique is illustrated by the domino buffer shown in Fig. 6(b). The additional crosscoupled transistor $M2$, called the twin-transistor, increases the turn-on voltage of $M1$ by pulling up the voltage of the common-source node. Note that $M2$ is ON at the beginning of evaluation phase since the node X has been precharged to V_{dd}. The increased noise

threshold is seen from the voltage transfer characteristics shown in Fig. 6(c).

Like all noise-tolerant circuit techniques, the twin-transistor technique achieves additional noise immunity at the expense of energy. It has been shown that the twin transistor technique is more energy-efficient than existing noise-tolerant dynamic circuit design techniques [18]. The twin transistors increase node capacitance and hence circuit delay. However, the size of twin transistors can be used to tradeoff delay against the noise threshold. Fig. 7 shows this tradeoff for a two-input AND gate. The delay penalty is seen to be about 60 ps per unit voltage increase in the noise threshold. The delay can however be maintained by increasing the sizes of the transistors in the principal nMOS pulldown path. For example, to maintain the delay of a two-input domino AND gate implemented with minimum size transistors when twin transistors are added, it is sufficient to double the sizes of the three transistors in the nMOS pulldown path.

Twin-transistors also help to mitigate the charge-sharing problem that occurs in dynamic logic circuits. This is fortunate since the use of twin-transistors prevents the use of additional transistors to precharge intermediate nodes [19]. An added benefit of this technique is that the internal nodes are precharged only when the inputs are such that charge-sharing can potentially occur.
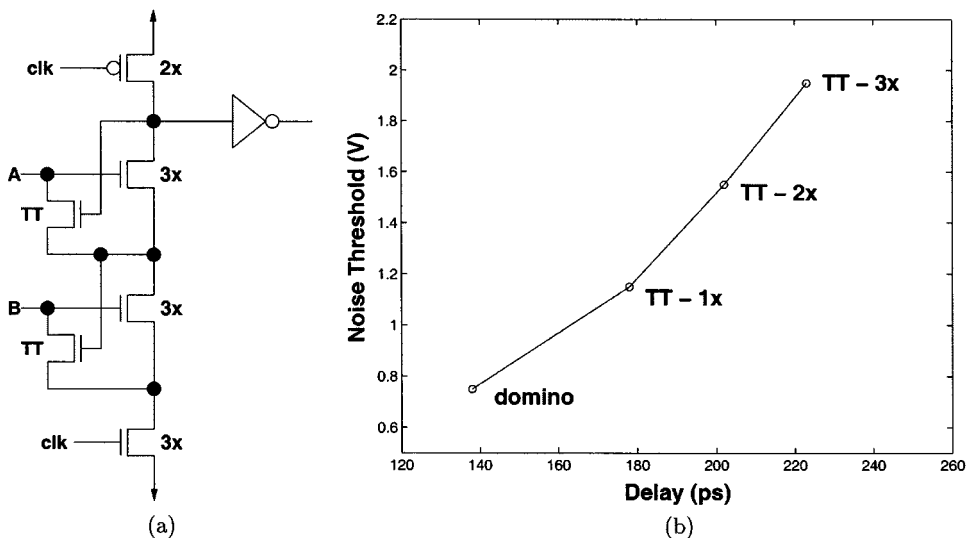
Fig. 7. (a) A two-input AND gate implemented using twin transistors. (b) Simulation results of a two-input AND gate driving an identical gate, showing that the size of the twin transistors can be used to trade off delay against noise immunity.
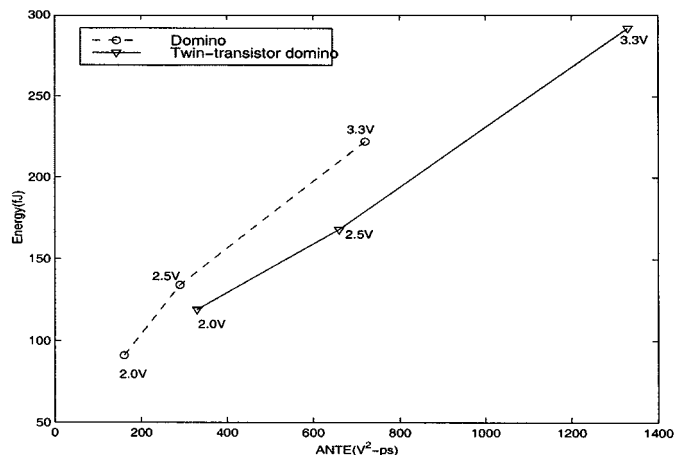

Fig. 8. Comparison of the energy consumption (per clock cycle) and ANTE of a two-input AND gate implemented using conventional domino and twin-transistor domino circuits. V_{dd} assumes values of 3.3, 2.5, and 2.0 V, and in each case V_T is scaled to ensure that the maximum operating frequency is 1.8 GHz. The energy consumption includes energy consumed by the clock and input buffers.

Since the twin transistor technique achieves higher noise immunity than a conventional domino logic circuit, one can operate at a smaller supply voltage to achieve the noise immunity of the conventional circuit at a higher voltage. Of course, the threshold voltage should also be scaled to ensure a constant delay. We used three (V_{dd}, V_T) combinations that achieve the same delay and simulated the conventional domino circuit and the noise-tolerant twin transistor domino circuit at these voltages. The resulting ANTE and energy consumption are plotted in Fig. 8. This plot shows that to achieve a certain noise immunity (quantified by ANTE), it is more energy-efficient to use the twin transistor domino circuit at a lower V_{dd} than the conventional circuit at a higher V_{dd}. For example, to achieve an ANTE of about 700 V^2-ns, one can either operate a simple domino circuit at 3.3 V or the twin transistor domino circuit at 2.5 V (V_T is about 0.4 V). However, Fig. 8 shows that the latter approach uses
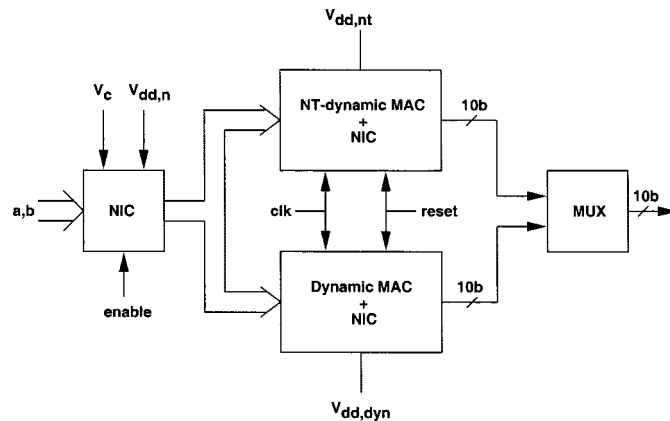

Fig. 9. Simplified block diagram schematic of the testchip.

about 30% less energy. Greater energy savings may be achieved in practice as the target ANTE itself will scale with V_{dd}.

V. TEST CHIP DESIGN AND EXPERIMENTAL RESULTS

A test IC has been designed and fabricated in order to obtain experimentally measured values of the improvement in noise immunity and the increase in power dissipation due to the twin-transistor technique over conventional dynamic logic.

A. MAC

A simplified schematic of the test IC is shown in Fig. 9. Two MACs are built on-chip—one using conventional domino logic (MAC-I), and another using twin-transistors (MAC-II). Both the MACs are pipelined at the bit level and designed to operate at a maximum speed of 500 MHz at 3.3 V supply. The transistors used in the nMOS pulldown path of all dynamic logic gates in MAC-II are twice as large as their counterparts in MAC-I to offset the effect of twin-transistors on delay. The twin-transistors in MAC-II are all of minimum size. Separate supply pins are used for the two MACs to enable measurement of the additional power dissipation caused by the use of twin transistors.
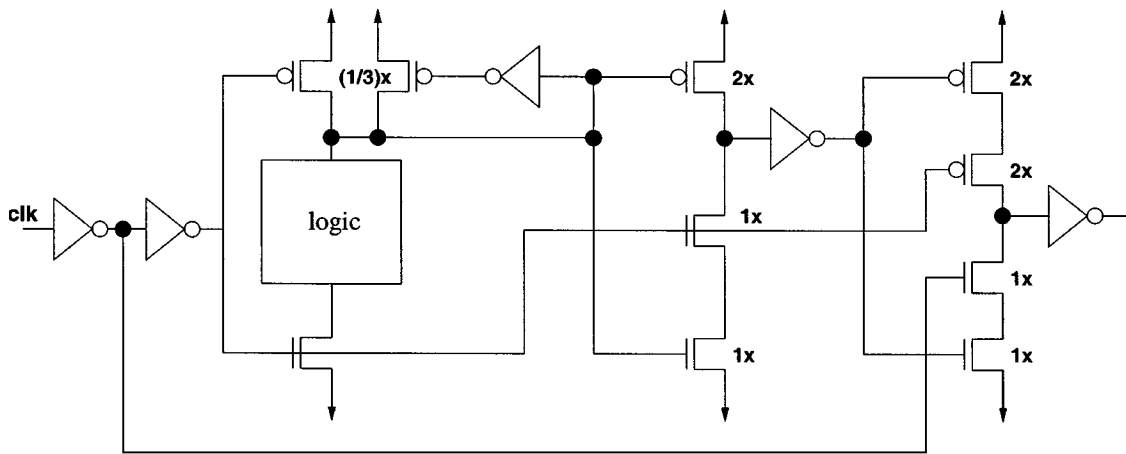
Fig. 10.   Schematic of a general pipelined logic gate used in the MAC. The "logic" block is replaced by the appropriate nMOS network (and twin transistors in the noise-tolerant implementation).
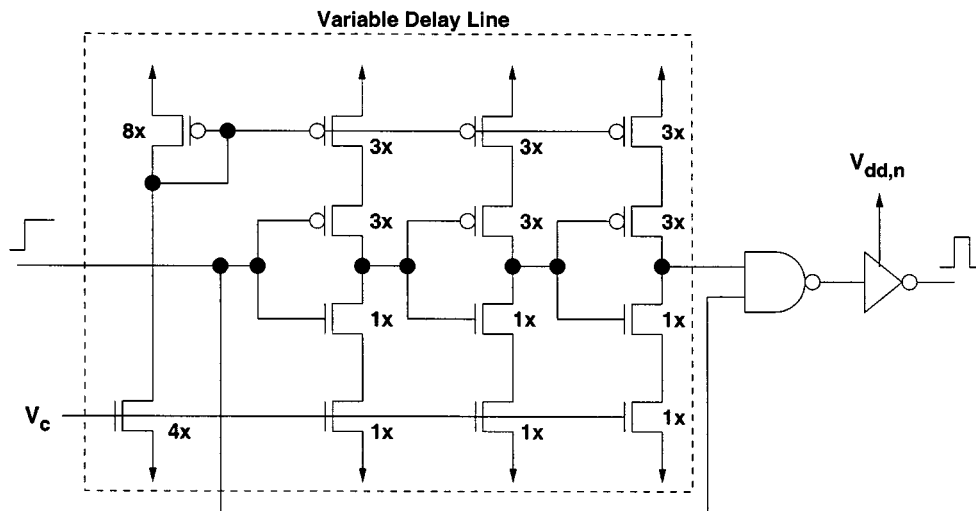

Fig. 11.   Simplified schematic of the NIC. Voltages V_c and $V_{dd,n}$ enable the control of the noise duration and amplitude respectively.

Noise-injection circuits (NICs) are distributed throughout the MACs so that one input of every gate (a full adder, AND gate, or a latch) in the MACs is noisy. Inputs V_c and $V_{dd,n}$ control the amount of noise injected by the NIC when it is enabled. The *reset* input disables the accumulator section of the MAC. Inputs and outputs are skewed to accomodate the bit-level pipelining scheme.

The multiplier is a simple array multiplier consisting of AND gates and half and full adders. It is pipelined so that one bit of the product is available at the end of each clock cycle. The general structure of a pipelined logic gate used on this chip is shown in Fig. 10. The part of the schematic labeled "logic" is replaced with the appropriate nMOS pulldown network (along with twin transistors in the case of MAC-II). Inverters are inserted wherever necessary to avoid the situation of a dynamic node driving a dynamic gate [20].

B. Noise Injection Circuit

The function of the NIC is to inject a noise pulse of desired amplitude and width into a logic gate. NICs are distributed throughout the chip to inject noise at several points in the logic evaluation path. The basic idea used in the design of the NIC is

to produce a glitch at the output of a gate by staggering its inputs in time. The circuit implementation of this idea is illustrated in Fig. 11.

A tunable delay line is used to delay one of the inputs to a dual-input gate. The delay and hence the noise-pulse duration T_n can be controlled through the voltage V_c. The amplitude of the noise V_n can be controlled through the supply voltage of the final inverter $V_{dd,n}$. Fig. 12 shows a typical noise waveform and the definition of noise amplitude and duration, that is used to quantify noise immunity. Fig. 13 shows the range of noise waveforms that can be generated using this technique. It can be seen that the amount of noise injected into a dynamic gate can be varied over a significant range through the control voltages, V_c and $V_{dd,n}$.

C. Experimental Results

The test IC was fabricated in 0.35-μm technology through MOSIS using the process HPGMOS10QA. A photomicrophotograph of the chip is shown in Fig. 14. The die size is 2 mm $\times$ 2 mm and it integrates about 10K transistors.

The noise immunity curve of a logic gate is the set of all combinations of noise amplitudes V_n and durations T_n that
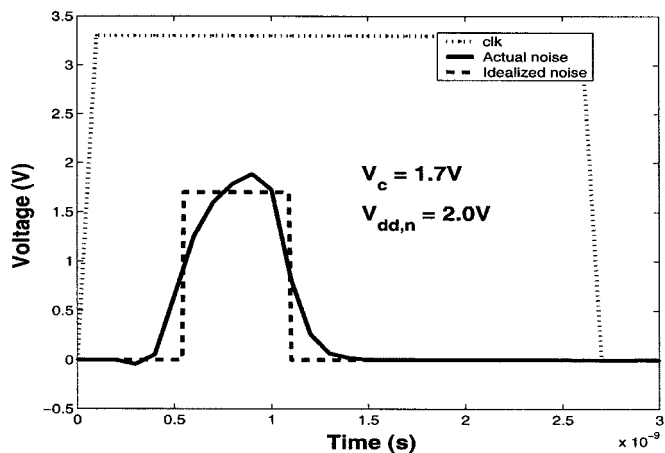
Fig. 12.   HSPICE simulation results showing a typical noise waveform. The idealized noise waveform is constructed so that its duration equals the time for which the noise voltage exceeds 50% of its peak value. The amplitude is chosen so as to preserve the area under the noise waveform.
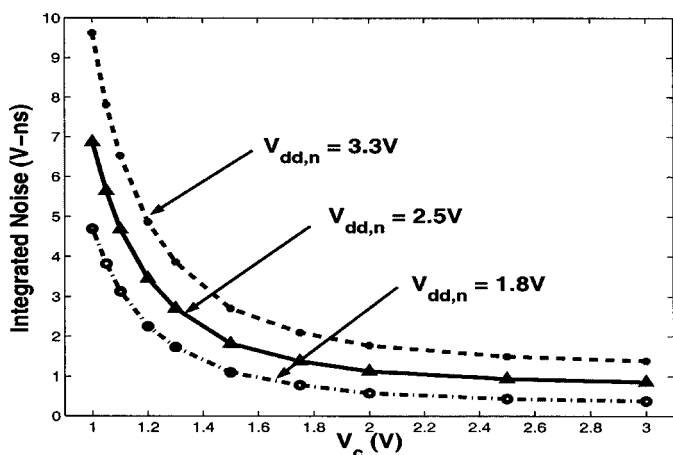

Fig. 13.   Simulation results showing the dependence of the integral of the noise waveform on V_c and $V_{dd,n}$.
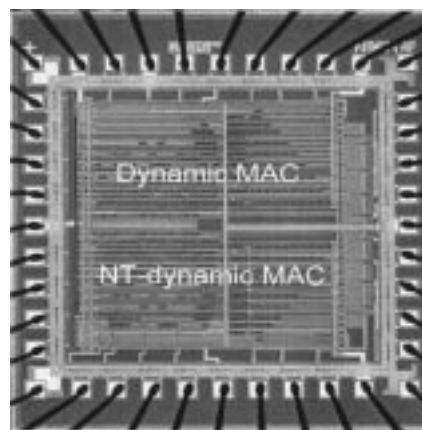

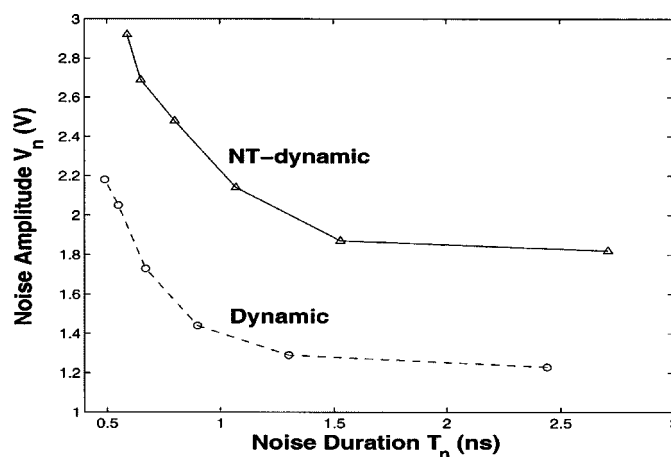
Fig. 14.   Photomicrograph of the test chip.

Fig. 15.   Experimentally measured noise immunity curves of the dynamic and noise-tolerant dynamic multiplier. The curves are the average of the results over several input combinations.

TABLE I
NOISE IMMUNITY (ANTE) RESULTS (MEASURED)

	Conventional	Twin transistor
AND2(V^2-ns)	2.47	6.67
Multiplier(V^2-ns)	2.40	5.65

TABLE II
POWER DISSIPATION AT $V_{dd} = 3.3$ V, 100 MHz

	Conventional	Twin transistor
AND2 (μW)	57	69
Fulladder (μW)	191	260
MAC (mW)	10.3	11.9

cause the gate output to switch. Noise immunity curves were obtained experimentally using the tunable noise injection circuit described in the previous section. Measured values of V_c and $V_{dd,n}$ (Fig. 11) that cause an error in the output of the MAC, are mapped to corresponding noise amplitudes and durations using simulation results such as those shown in Fig. 13. The noise immunity curves for the two multiplier implementations derived using this approach are shown in Fig. 15. It can be seen that the twin-transistor technique increases the noise threshold by about 0.65 V, over that of conventional dynamic logic. Noise immunity can be quantified using (9).

From the noise immunity measurement results shown in Table I, it can be seen that the use of twin-transistors provides an improvement in ANTE that is greater than 2.4× for a two-input AND gate and the multiplier. This improvement is obtained at the cost of additional power dissipation. Information about power dissipation is summarized in Table II. Power dissipation values for the AND gate and full adder were obtained from HSPICE simulations while those for the MAC were measured experimentally. The power penalty of the complete MAC (15%) is smaller than that of the full adder alone.

This is because both the dynamic and noise-tolerant dynamic implementations of the MAC share some common circuitry due to pipelining overhead, specifically latches, clock buffers and delay elements, which mitigate the power penalty due to the twin-transistors. These results show that the twin-transistor technique provides a significant improvement (2.4×) in the noise immunity of dynamic logic circuits, with only a modest increase in power dissipation (15%).

VI. CONCLUSION

We have shown, by analysis using simple models and by simulations, that the sensitivity of dynamic circuits to crosstalk noise increases when the voltage scaling approach to low-power design is employed. A new noise-tolerant dynamic circuit technique has been presented to address this problem. This technique has been used to implement a MAC testchip, and experimental results demonstrate the improved noise immunity provided at nominal increase in power dissipation.

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