Receiver Adaptation and System Characterization of an 8Gbps Source-Synchronous I/O Link using On-die Circuits in 0.13μm CMOS

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Abstract

This paper describes a 0.13μm CMOS, 8Gbps I/O receiver that uses on-die circuits for receiver adaptation and system characterization. On-die adaptive control is used to tune a 4-tap receive-side analog equalizer, cancel receiver offsets, and determine optimal sampling phase. Adaptive equalization improves data rates by 1.3x-2x over 2"-40" FR4 channels. Noise-margin degradation due to statistical variation in adapted coefficients and offsets is less than 3% of the signal swing. On-die circuits are also used to characterize link performance, channel response, and receiver circuits.
Keywords: I/O, Equalization, Offset cancellation, Adaptation, Source-synchronous signaling, FR4, Backplane.

Introduction

As inter-chip signaling rates scale to several Gbps, channel intersymbol interference (ISI) severely limits achievable data rates. Equalization has been widely employed in recent high-speed I/O links to mitigate ISI [1,2,4,5]. Transmit pre-emphasis suffers from the peak transmit power constraint and has to be augmented by receive-side equalization for severe ISI channels. The design of a time-interleaved receive-side equalizer was presented in [1] and is also shown in Fig. 1 for reference. In this paper, we focus on the implementation of the adaptive control for this receiver. We also describe the use of on-die circuits to characterize the I/O channel and receiver circuits.

Receiver Adaptation

Variations in board, IC manufacturing processes and intended application space (e.g. desktop versus server platforms) make an adaptive receiver desirable for I/O links. Typical FR4 channels for I/O vary in length from 2" to 40" resulting in a wide variety of frequency responses as shown in Fig. 2. Previous implementations of adaptive equalization for I/O relied on a reverse channel [2], or were implemented off-chip using software. This implementation uses on-die adaptive control, which in addition to determining the optimal equalizer settings, also cancels receiver offsets, and determines the optimal sampling phase (clock de-skew[3,4]). Fig. 3 shows a schematic of the digital adaptive control and its interface with the analog I/O receiver.

The adaptation of the receiver is based on a training sequence, which is summarized in the simplified flowchart in Fig. 4. During the initial offset trim phase, dominant offsets at the 8 interleaved latch inputs are cancelled by transmitting '0', '1' dc patterns, modulating the offset current DAC (C-DAC) (see Fig. 1) to trip the latch, and averaging the results. In the following alignment phase, the receive bit-stream is optimally delayed to align it with the expected training pattern. This is a two step process involving coarse alignment based on a '0'-to-'1' transition detection and finer alignment using shifting and correlation. The optimal filter coefficients and offsets are then determined during the adaptation phase. Both filter and offset coefficients need to be adapted simultaneously as input offsets are scaled by the filter coefficients before they appear at the latch input. The update equations are variations of the partial zero-forcing (PZF) algorithm[6] and are given by:

$$w_{n+1,i}(j) = \begin{cases} 1.0, & j = cursor\ \ tap \\ w_{n,i}(j) + \mu_w \cdot \mathrm{sgn}\left(e_{n,i} \cdot I_{n,i} \cdot X_{n,i}(j)\right), & else \end{cases}$$

$$V_{n+1,i}(k) = V_{n,i}(k) - \mu_v \cdot \mathrm{sgn}(e_{n,i} \cdot I_{n,i})$$

$$I_{n,i} = \begin{cases} 1, d_n = (2i-1) \\ 0, d_n \neq (2i-1) \end{cases}$$

$$w_\infty(j) = \frac{w_{\infty,0}(j) + w_{\infty,1}(j)}{2} \qquad V_\infty(k) = \frac{V_{\infty,0}(k) + V_{\infty,1}(k)}{2}$$

where w (V) is the vector of filter (offset + reference) coefficients, X is the desired data vector, e_n is the current adaptation error, j=0..3 (k=0..7) is the filter (offset) tap index, n is the update index, $d_n \in \{-1,+1\}$ is the actual transmit binary symbol and i=0,1 represents the adaptation polarity. μ_w and μ_v are the update step sizes for coefficients and offsets respectively. The updates are performed in a block-based fashion by averaging over 32 bits. Use of selective updates through the indicator function $I_{n,i}$ simplifies the adapter implementation as shown in Fig. 5, by eliminating the need for a high-speed analog-digital interface. This selective update followed by averaging also allows both the offset cancellation current and adaptation reference current to be realized using a single C-DAC. Following adaptation, the noise-margin for the current sampling phase is estimated by modulating the offset cancellation C-DACs until bit errors occur and recording the tolerable offset margins. The previous steps are repeated for all possible sampling phases and the optimal sampling phase is then selected.

A schematic block diagram of the synthesized coefficient adaptation control is shown in Fig. 6. Coefficient registers were implemented as up-down counters with excess bits of precision to enable averaging and reduce steady-state coefficient noise. Adaptation parameters like update step size, update frequency, and number of updates were made tunable. Additional states were added to the adapter state machine to enable observation of the adaptation dynamics. A typical example of measured coefficient and offset evolution curves is shown in Fig. 7. The convergence time is less than 25μs. The degradation in noise-margins due to statistical variation in the adapted coefficients and offsets was found to be less than 3% of the transmit swing (measured over 500 iterations). An example of the variation of estimated noise-margin with sampling phase is shown in Fig. 8. The variation of noise-margin with data rate for four different FR4 channels with and without equalization is summarized in Fig. 9. Assuming the minimum required noise-margin is 10% of the transmit signal swing, the 4-tap adaptive equalizer increases

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achievable data rates by 33% for 2" FR4, and 100% (from 2 Gbps to 4 Gbps) for 40" FR4.

System Characterization

Increasing data rates and receiver complexity make the task of I/O test and characterization using external equipment difficult and expensive. We use on-die circuits in the form of C-DACs and low-speed digital logic to enable performance characterization and extraction of channel and circuit parameters. The link performance is characterized by eye diagrams, which are obtained by sweeping the digital input codes to the phase interpolators and the offset cancellation C-DACs [3,4]. On-die PRBS generator and error counters are used to compute the bit error rate. Examples of resulting eye diagrams are shown in Fig. 10.

Besides characterizing overall link performance, on-die circuits can be used to analyze individual components of the I/O link. The offsets and sensitivities of comparators can be measured using the offset cancellation C-DACs and error counters as shown in Fig. 11. By sweeping the C-DAC input code and recording the number of errors for each code, the cumulative distribution function or transfer curve[4] of each of the eight interleaved latches can be derived. The results in Fig. 12 show little within-die variation of latch sensitivities but a significant variation in latch offsets. These offsets differ from those computed by the adaptation logic by less than 2% of the signal swing.

In addition to the comparator, the front-end V-to-I converters (VICs) and current mirrors (CMs) also contribute to the receiver offset (see Fig. 1). These individual offsets can be determined by appropriate choices of transmit data and filter coefficients as shown in Fig. 13. The 1-σ values of comparator, VIC, and CM offsets were found to be 13.9%, 2.3%, and 4.7% of the transmit swing respectively.

Characterization of the I/O channel was performed using equivalent time sampling [4]. The sampled differential pulse response (SDPR) was derived by subtracting the response to an all '0's pattern from the response to a 32b periodic train of lone '1's. The measured unequalized SDPRs for 3.2Gbps transmission over 2" FR4 and 40" FR4 channels are shown in Fig. 14. The measured SDPR after 4-tap receive equalization shows substantially smaller ISI, with less than 4% degradation in the received signal magnitude (cursor value in the SDPR). The simulated SDPR with an ideal 4-tap transmit pre-emphasis filter shows 29% reduction in received signal magnitude due to constraints on the maximum transmit swing. This shows the advantage of using receive-side equalization when equalizing severe ISI channels.

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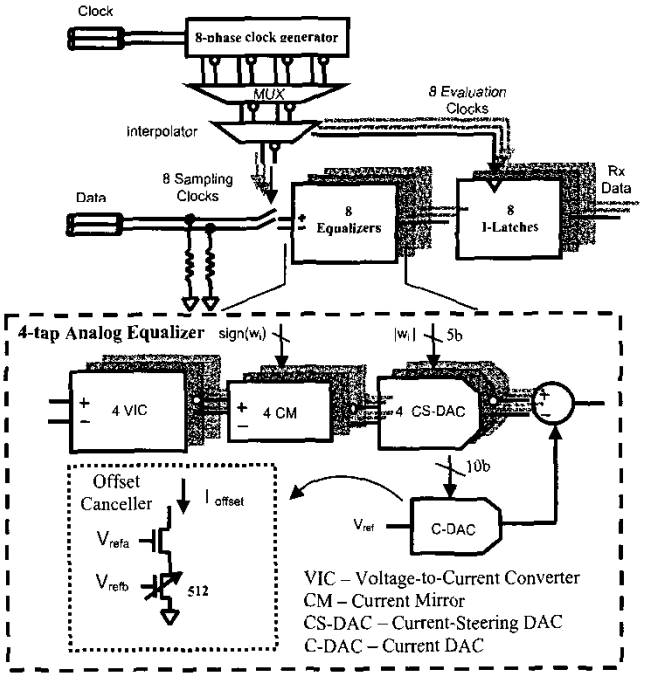


Fig. 1. Schematic of the 8-way time-interleaved receiver.

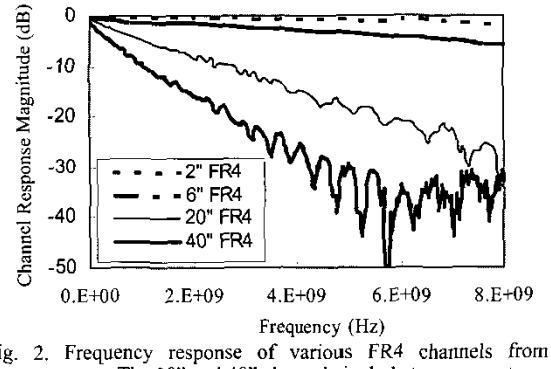


Fig. 2. Frequency response of various FR4 channels from TDR measurements. The 20" and 40" channels include two connectors.

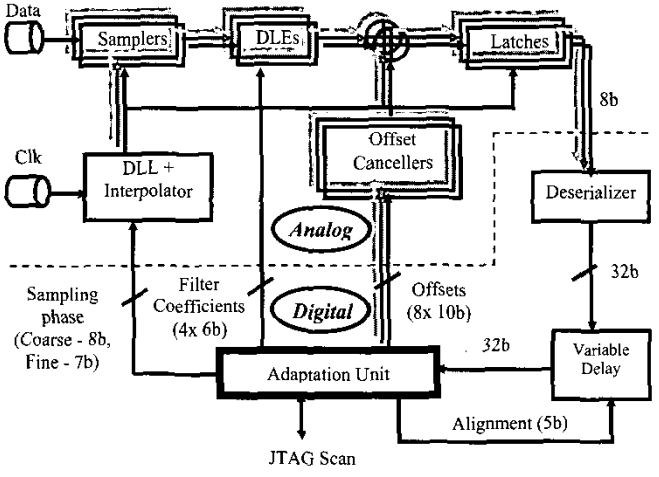


Fig. 3. Schematic showing the interface between digital adaptive control and the analog receiver.

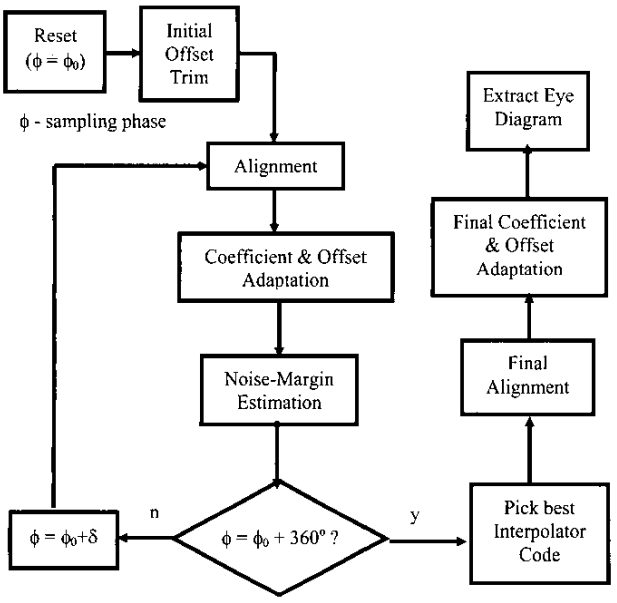


Fig. 4. Flowchart showing the adaptive receiver training sequence.

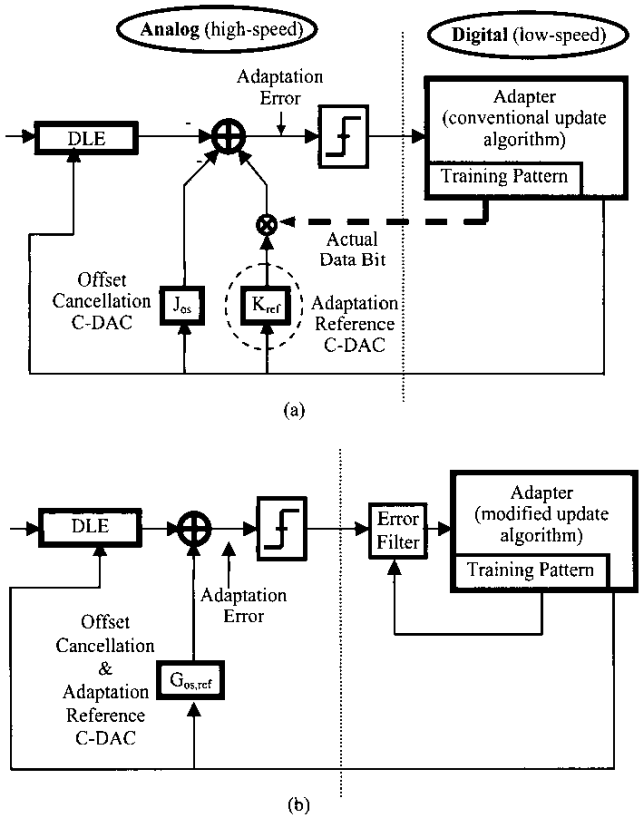


Fig. 5. Comparison of two possible architectures to implement adaptive equalization and offset cancellation – (a) conventional, and (b) modified architecture using selective update algorithm that simplifies hardware implementation.

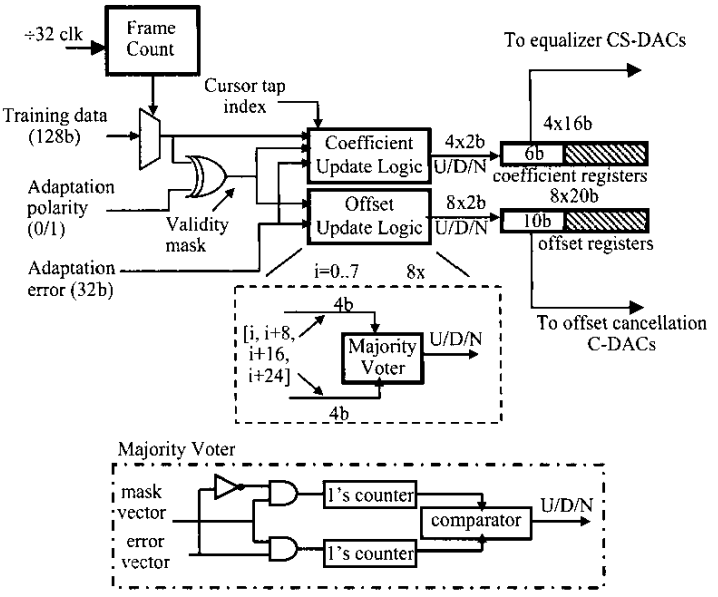


Fig. 6. Block diagram schematic of the adaptation logic (only offset update logic shown).

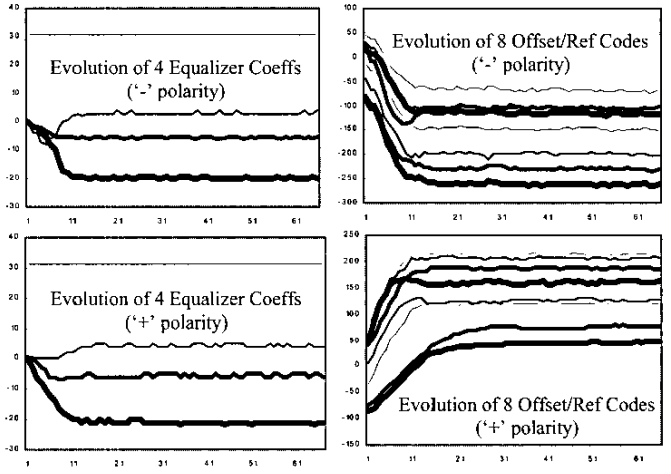


Fig. 7. Measured evolution of filter coefficients and offsets for 4Gbps transmission over 40" FR4. The step sizes for the coefficients and offsets are 0.25 and 0.5 LSBs respectively. Convergence occurs in about 25μs.

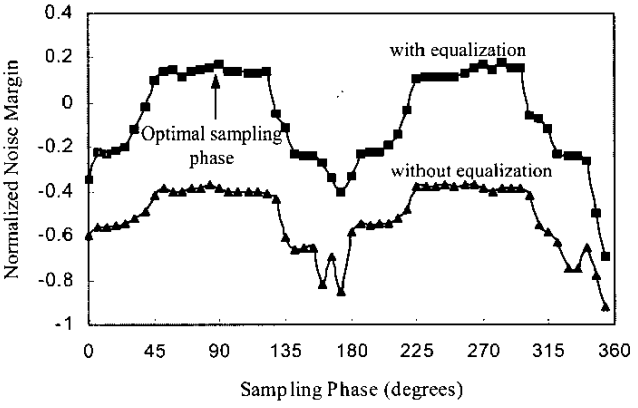


Fig. 8. Measured variation of noise-margin estimate (normalized to a transmit swing of 850mV) with sampling phase for 4Gbps transmission over 40" FR4.

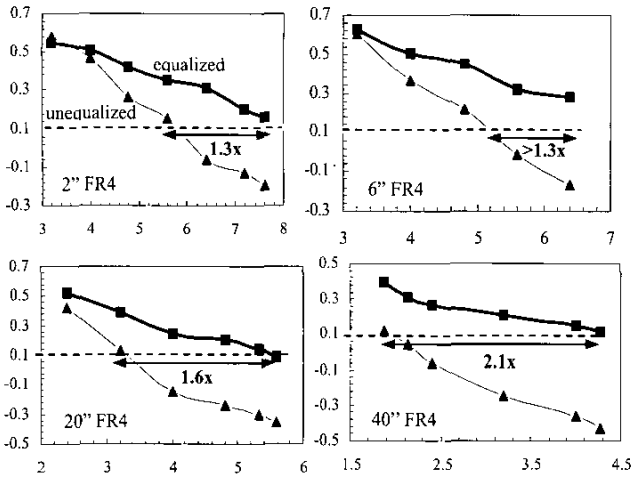


Fig. 9. Measured variation of noise-margin (normalized to a transmit swing of 850mV) with data rate (in Gbps) for 2"-40" FR4 channels. The thicker lines show equalized data and the thinner lines show unequalized data.

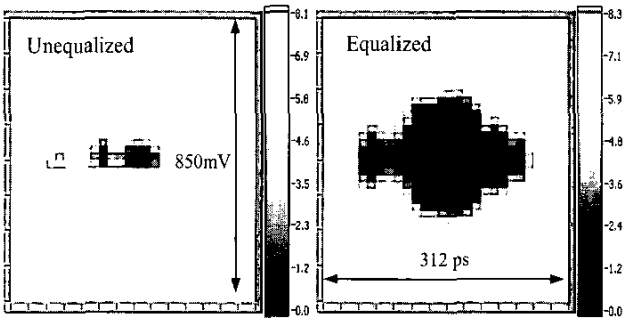


Fig. 10. Eye-diagrams extracted using on-die circuits for 3.2Gbps data over 20" FR4 with and without adaptive equalization. The bars to the right indicate BER on a logarithmic scale.

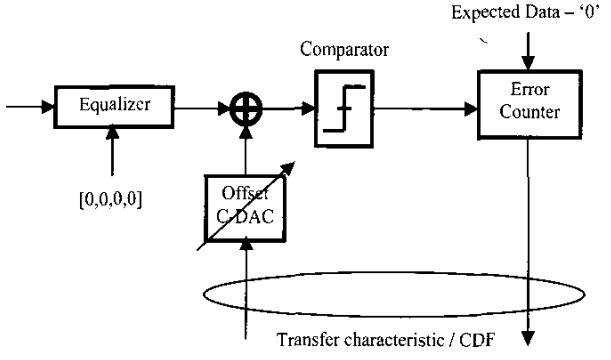


Fig. 11. Characterization method for comparators using on-die circuits. CDF is the cumulative density function or the probability of the latch resolving an input signal to bit value '1'.

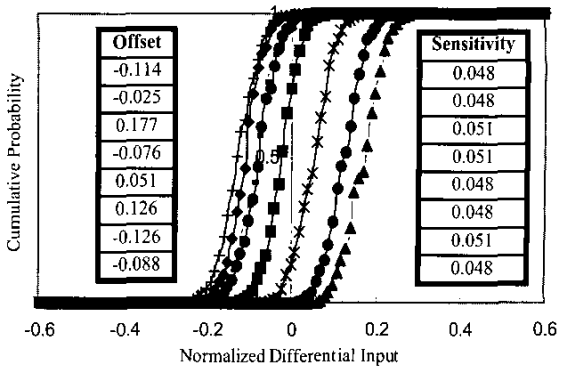
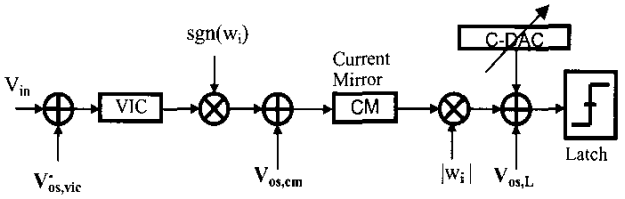


Fig. 12. Characteristic curves for 8 interleaved latches in one receiver measured using on-die circuits. Offsets and sensitivities are normalized to the signal swing of 850mV.



Tx bit	w_i	C-DAC offset
1	0	$V_{a1}=V_{os,L}$
1	-1	$V_{a2}=-V_{sw}-V_{os,vic}+V_{os,cm}+V_{os,L}$
1	+1	$V_{a3}=V_{sw}+V_{os,vic}+V_{os,cm}+V_{os,L}$
0	+1	$V_{a4}=-V_{sw}+V_{os,vic}+V_{os,cm}+V_{os,L}$

$$V_{os,L}=V_{a1}$$

$$V_{os,cm}=\frac{V_{a2}+V_{a3}}{2}-V_{a1}$$

$$V_{os,vic}=\frac{V_{a4}-V_{a2}}{2}$$

Fig. 13. Receiver offset components and decomposition method.

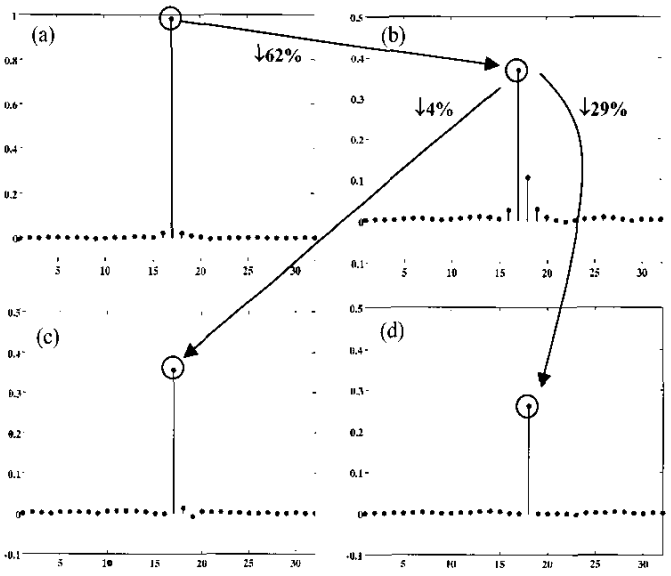


Fig. 14. Measured sampled differential pulse responses for 3.2Gbps data transmission over – (a)2" FR4 (unequalized), (b)40" FR4 (unequalized), (c) 40" FR4 with 4-tap receive equalization, and (d) 40" FR4 with ideal 4-tap transmit pre-emphasis (simulated using the response in (b)).