13.8 An 8Gb/s Source-Synchronous I/O Link with Adaptive Receiver Equalization, Offset Cancellation and Clock Deskew

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An adaptive I/O link is implemented in 0.13µm CMOS to meet the signaling requirements of performance microprocessor platforms. The differential link employs binary signaling, adaptive analog discrete-time linear equalization (DLE) and source-synchronous clocking to enable un-encoded data transmission [1]. The receiver uses an 8-way interleaved equalizer architecture that reduces power dissipation. The DLE is a 4-tap FIR filter that mitigates ISI. In order to accommodate a wide variety of channels and process variations, on-die adaptation logic determines optimal settings for equalization, offset cancellation and per-pin clock deskew. On-die waveform capture and diagnostic capability is also incorporated to enable high-speed test and measurement [1].

The transceiver architecture is shown in Fig. 13.8.1. The driver uses a current-mode, differential amplifier with a cascode transistor to improve the output impedance [1]. The received source-synchronous clock is first amplified before being fed to the delay-locked loop (DLL). The DLL generates four differential clock phases that are buffered and driven across the port. The interpolator combines two adjacent phases and provides a reference clock phase to the sampling clock generator. The clock generator yields eight sampling and evaluation clock phases, four of which are referenced to the rising edge and four to the falling edge. The 8-way interleaved receiver allows one DLE to evaluate while the other DLEs acquire samples and settle to steady-state values. This architecture eliminates the need to rotate filter [2] and offset coefficients, thus reducing power dissipation. The only dynamic elements are the samplers and current latches, also shown in Fig. 13.8.1.

The receiver containing the FIR filter is shown in Fig. 13.8.2. Front-end samplers precede V-to-I converters (VIC) that are implemented as source-coupled differential pairs. The outputs of the VIC are mirrored and fed as inputs to the appropriate FIR filter taps. This mirroring allows one VIC output sample to be shared among four different filter taps. Following the VIC and current mirror, a 5b binary-weighted current steering DAC (I-DAC) is used to implement tap multiplication as shown in Fig. 13.8.2. The sign bit of the 6b filter coefficient is implemented using a pass gate prior to the current mirror. The output currents of the four taps are summed at the input to a differential current latch. A 10b current DAC (C-DAC) also feeds into the comparator to enable offset cancellation and coefficient adaptation. A cascode transistor is added to improve the output resistance and linearity of the C-DAC. While all but one of the eight equalizers share the same 6b filter coefficients, the current latch offsets are independently controlled in order to account for random on-die parameter variations. In order to eliminate the need of additional comparators generally required to implement sign-sign least-mean square (SSLMS) adaptation, tap weights of one equalizer are independently controlled.

On-die adaptation logic is used to determine optimal receiver settings in the presence of channel and circuit variations. Tunable receiver parameters include the equalizer filter coefficients, the comparator offsets and interpolator code settings for clock deskew. The adaptation engine is synthesized and operates at a fraction of the transmit data rate. Coarse offset cancellation is initially performed by transmitting dc pattens of 1s and then 0s. Next the transmitter sends a 32b frame of 1s followed by a repetitive random 128b training pattern. The transition from 0s to the 32b frame of 1s enables initial alignment of the received data with the expected data prior to coefficient adaptation. Variations of partial zero-forcing (PZF) and SSLMS adaptation algorithms that enable simultaneous determination of the filter and offset coefficients is developed and implemented. The weight and offset update equations are given by Fig. 13.8.3, where w (V) is the vector of filter (offset and reference) coefficients, j=0..3 (k=0..7) is the filter (offset) tap index, μ_w (μ_v) is the coefficient (offset) step-size, $e_{n,i}$ is the adaptation error, n is the update index and i=0,1 represents the adaptation polarity. The elements of the state vector X are the desired data vector for PZF or the filter input vector for SSLMS.

Significant speed paths for the adaptation logic are eliminated allowing all components of the adaptation algorithm to be synthesized and operated at lower clock rates, considerably reducing power dissipation. The speed paths are avoided by removing the need for an additional C-DAC to generate a data-dependent reference signal. The adaptation error is determined by performing the adaptation twice, once for each reference polarity, and averaging the results. The range of the offset cancellation C-DAC is expanded to accommodate both the expected offsets and the reference current adaptation requirements. In order to reduce steady-state noise in the converged coefficient values, the internal representation of the filter and offset coefficients in the adapter uses ten excess bits. Test hooks in the adapter enable observation of adaptation dynamics. Figure 13.8.4 shows typical filter weight and offset coefficient evolution curves during adaptation at 4.8Gb/s over 50cm of FR4.

Determination of filter coefficients and offsets is followed by estimation of the noise-margin for the adapted receiver settings. The noise-margin estimation is accomplished during the training phase by skewing the current latch offsets in the positive and negative directions until bit-errors begin to occur and recording the maximum tolerable offset skew. The adaptation and noise-margin estimation steps are repeated for all possible interpolator code settings to obtain an estimated eye boundary. The interpolator code that gives the maximum noise-margin is selected and used for clock deskew, concluding the adaptation process. Port adaptation typically takes tens of milliseconds. The transmitter is now enabled to transmit random data, and the receiver error counter is also enabled. The offsets and interpolator codes are swept around their nominal values to extract an eye diagram as shown in Fig. 13.8.5.

The maximum unidirectional un-encoded data rates with less than 10^{-10} BER are 8Gb/s over 5cm FR4, 8Gb/s over 17cm FR4 and 5.6Gb/s across a 50cm stripline with 2 connectors and a backplane. Over 5cm FR4, 10Gb/s is achievable with multiple 32 bit random patterns . Figure 13.8.6 summarizes the test chip results.

Acknowledgments:
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References:
[1] A. Martin et. al, "An 8Gb/s Differential Simultaneous Bidirectional Link with 4mV-9ps Waveform Capture Diagnostic Capability," *ISSCC Dig. Tech. Papers*, pp. 78-79, Feb. 2003.
[2] T. Lee, B. Razavi, "A 125-MHz CMOS Mixed-Signal Equalizer for Gigabit Ethernet on Copper Wire," *IEEE CICC Dig. Tech. Papers*, pp131-134, May 2001.

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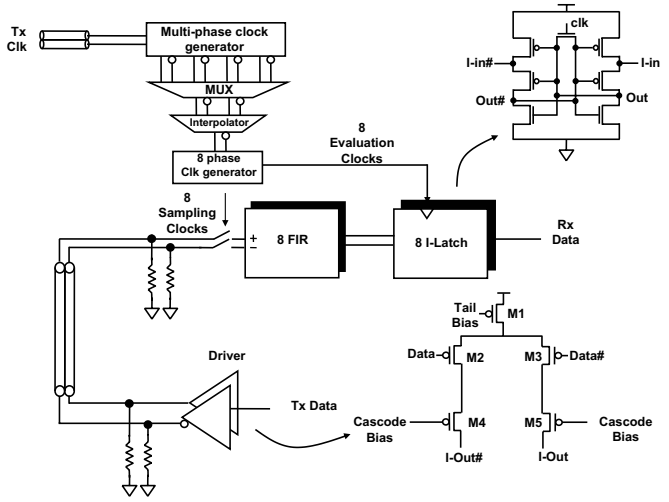

Figure 13.8.1: I/O architecture and circuits.

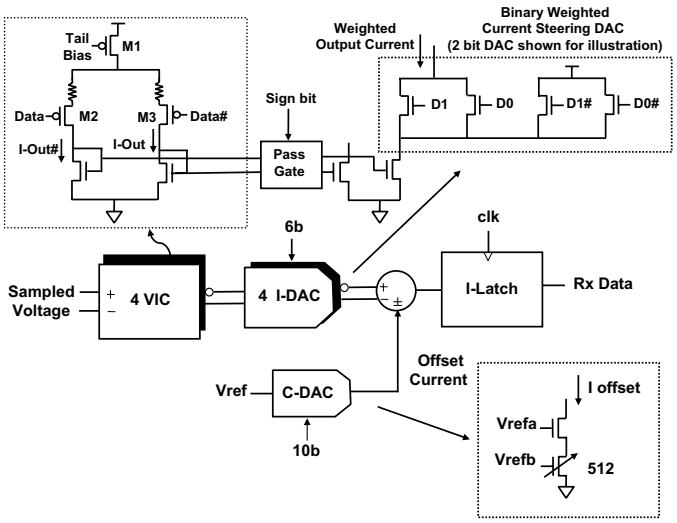

Figure 13.8.2: FIR filter architecture.

$$\boldsymbol{w}_{n+1,i}(j) = \begin{cases} 1.0, & j = cursor\ tap \\ \boldsymbol{w}_{n,i}(j) + \mu_w \cdot \mathrm{sgn}\left(e_{n,i} \cdot \boldsymbol{X}_{n,i}(j)\right), & else \end{cases}$$

$$\boldsymbol{V}_{n+1,i}(k) = \boldsymbol{V}_{n,i}(k) - \mu_v \cdot \mathrm{sgn}(e_{n,i})$$

$$\boldsymbol{w}_{\infty}(j) = \frac{\boldsymbol{w}_{\infty,0}(j) + \boldsymbol{w}_{\infty,1}(j)}{2}$$

$$\boldsymbol{V}_{\infty}(k) = \frac{\boldsymbol{V}_{\infty,0}(k) + \boldsymbol{V}_{\infty,1}(k)}{2}$$

Figure 13.8.3: Adaptation update equations.

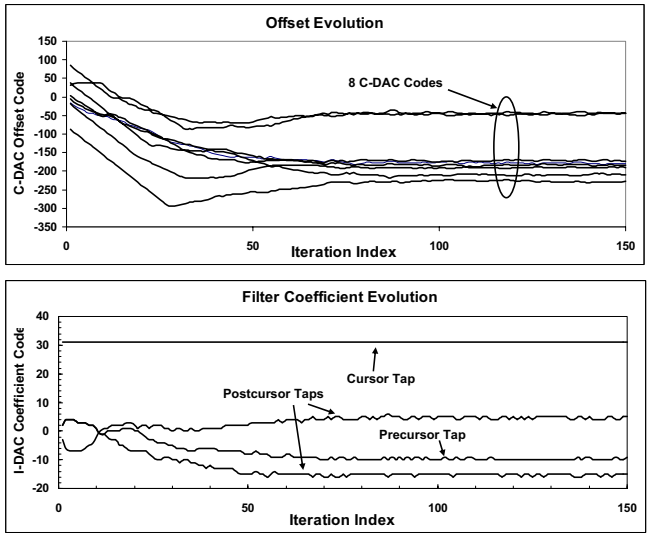

Figure 13.8.4: Evolution of offsets and coefficients during adaptation.

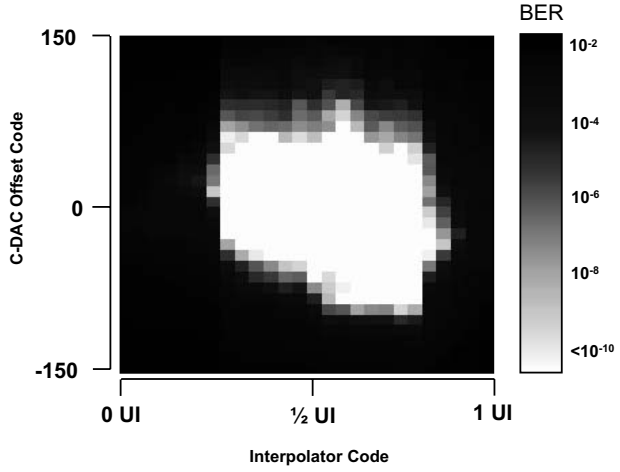

Figure 13.8.5: Sample eye diagram at 7.5Gb/s over 5cm FR4.

Max Data Rate (5 cm FR4)	8 Gb/s
Max Data Rate (17 cm FR4)	8 Gb/s
Max Data Rate (50 cm FR4)	5.6 Gb/s
Estimated Power	280 mW
I/O Cell Area	360μm x 360μm
Supply Voltage	1.7 V
Process Technology	0.13 μm
Package Technology	C4 OLGA
On-die Adaptation Convergence Time	~20 ms

Figure 13.8.6: Test chip summary.

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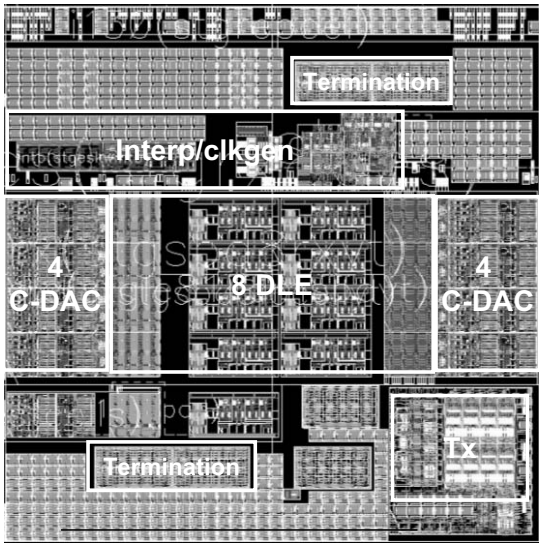

Figure 13.8.7: 360μm x 360μm I/O cell micrograph.

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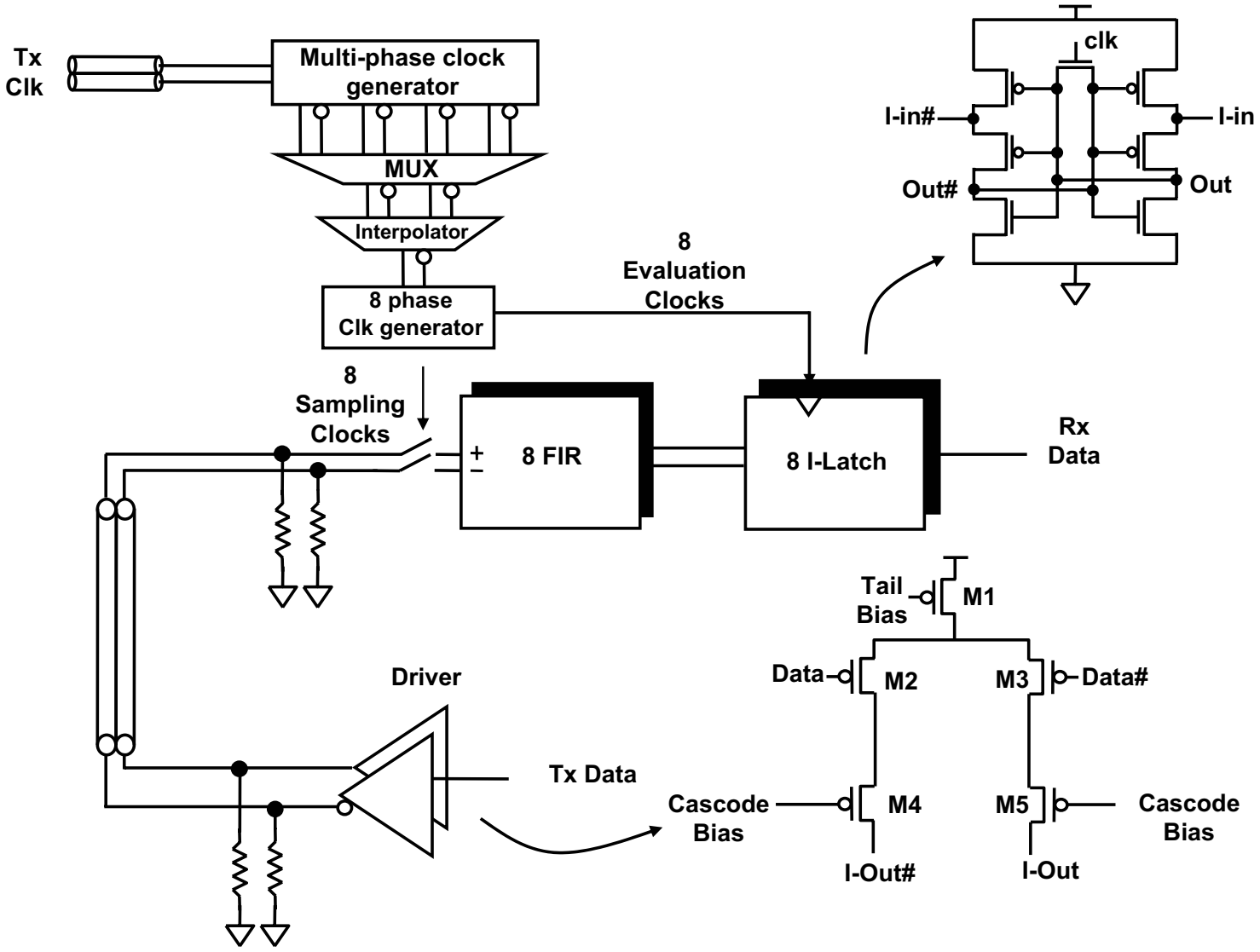

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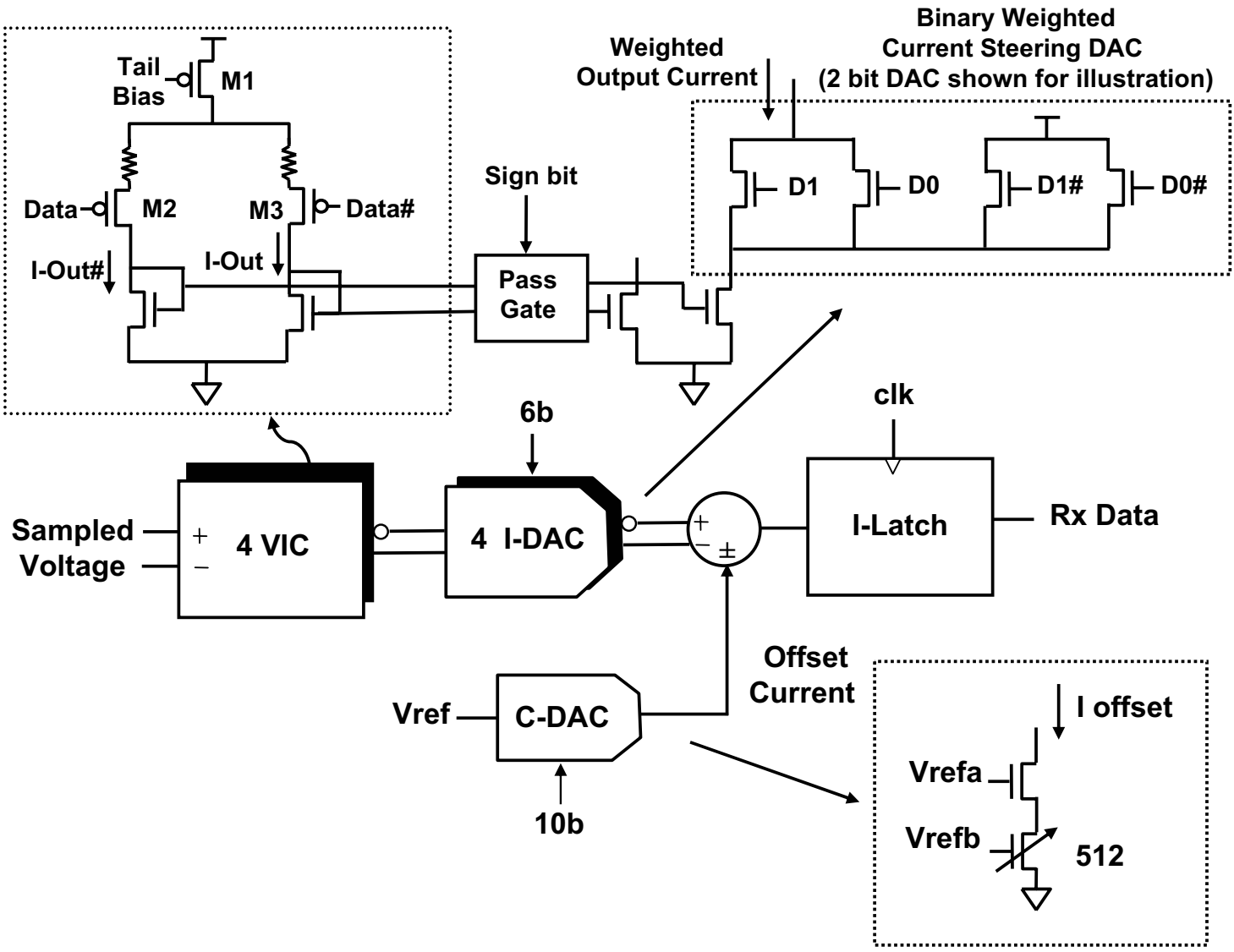

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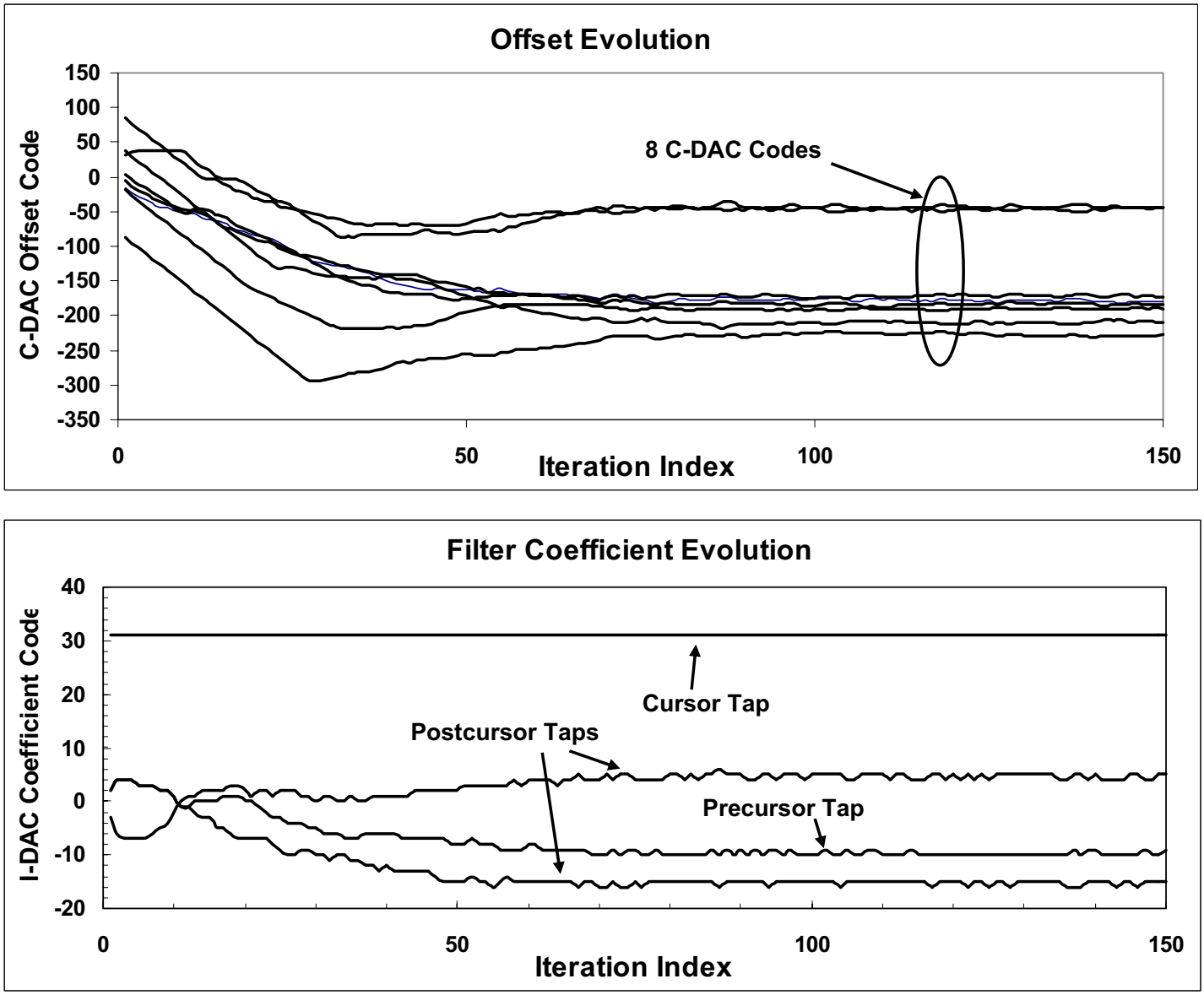

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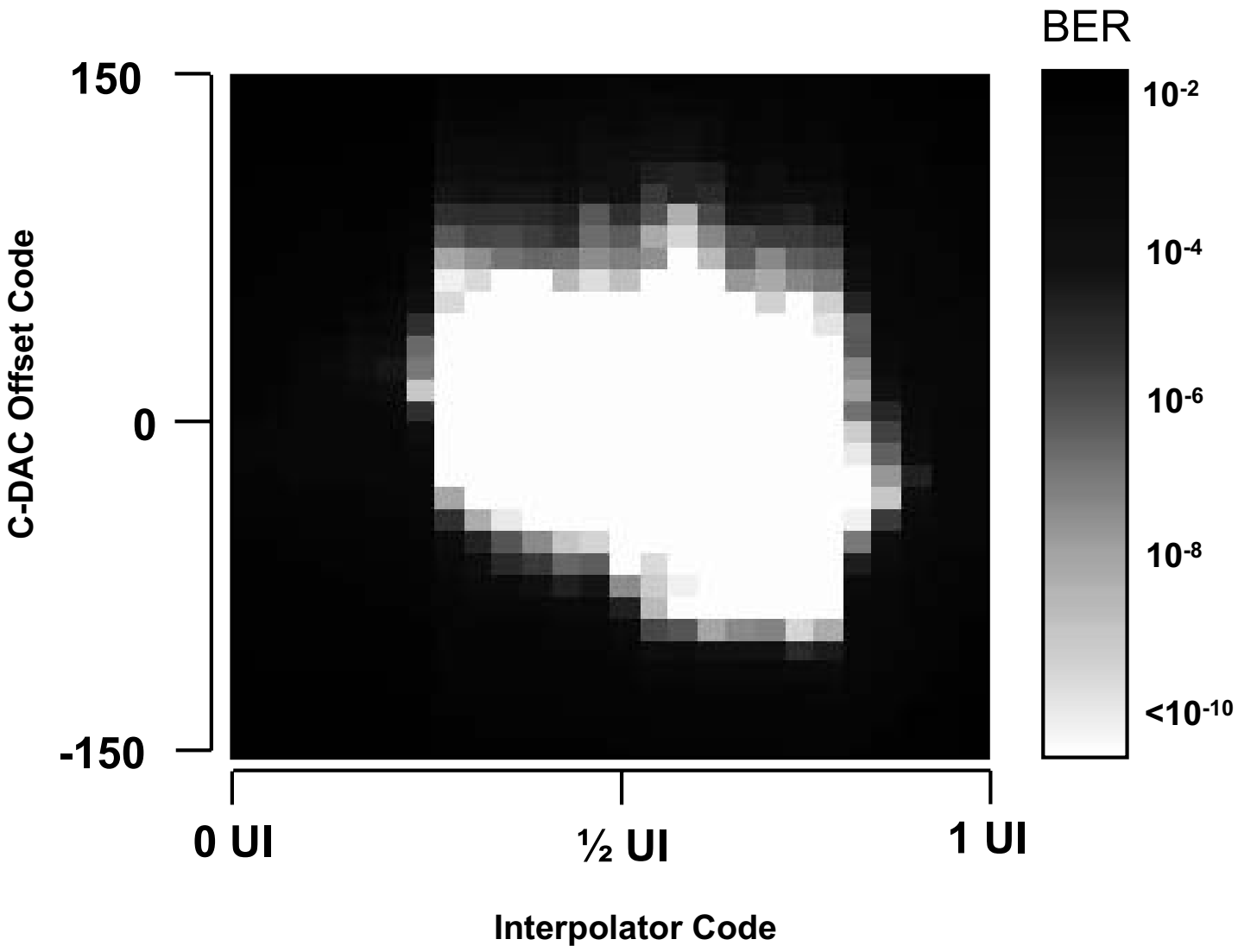

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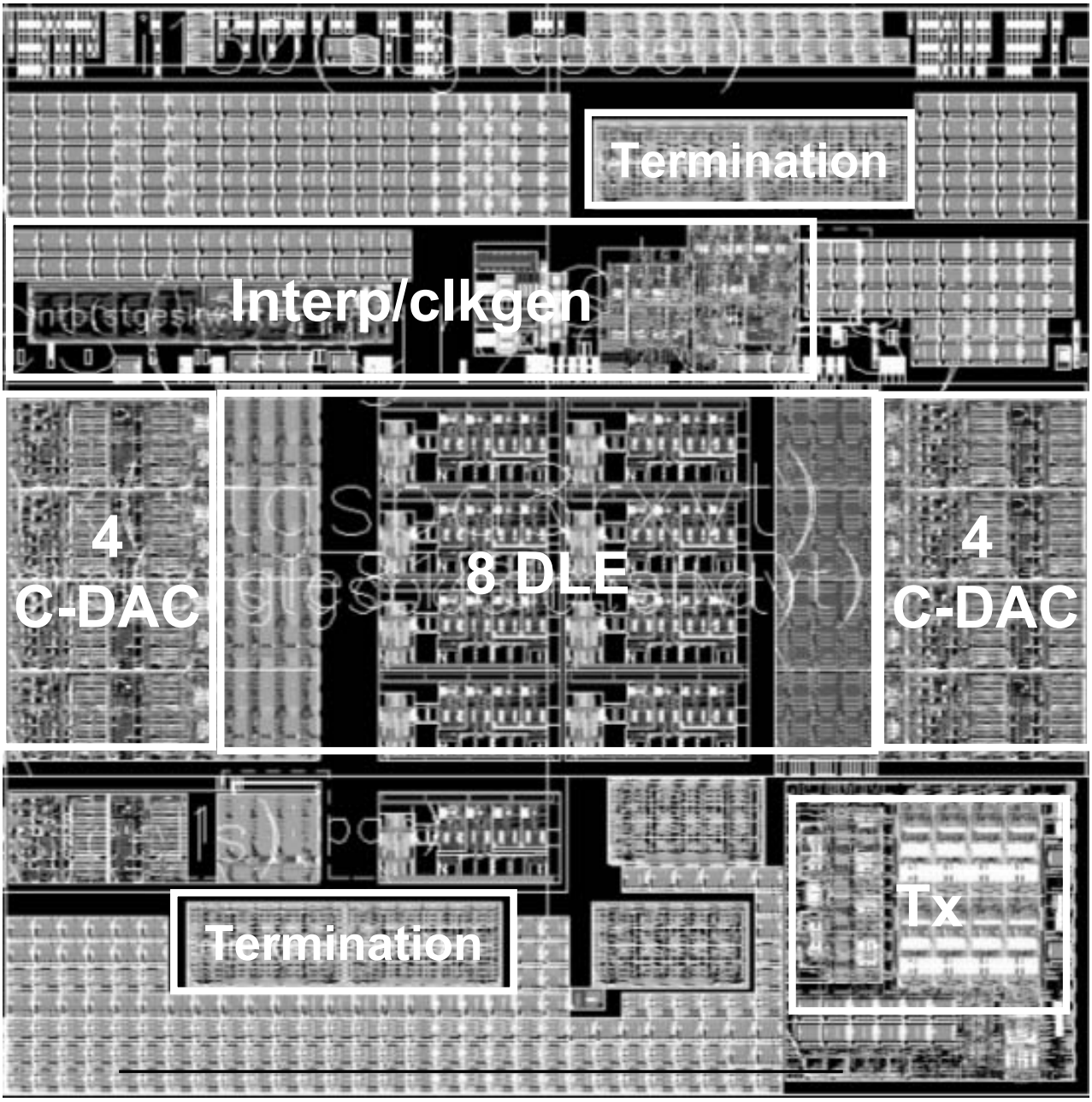

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