Fast Power Transient Management for OC-192 WDM Add/Drop Networks

Hyeon-Min Bae, Jonathan Ashbrook, Naresh Shanbhag, *Fellow, IEEE*, and Andrew Singer, *Senior Member, IEEE*

***Abstract*—This paper describes a fast power transient management functionality incorporated into a 12.5 Gb/s maximum likelihood sequence estimation (MLSE) receiver for optical add/drop multiplexer (OADM)-based WDM networks. The receiver has a VGA with a fast automatic gain control and a high-bandwidth offset cancellation loop. Measured results indicate that the receiver IC tolerates a 10 dB/10 μs optical power transient with 72 consecutive identical digits with no BER impact, and offers a 100X improvement over a standard CDR in tracking an 8 dB sinusoidal power transient at a BER of 10^{-4}.**

***Index Terms*—Clock and data recovery (CDR), electronic dispersion compensation (EDC), maximum likelihood sequence estimation (MLSE), OC-192, variable gain amplifier (VGA).**

I. Introduction

OPTICAL add/drop multiplexers (OADM) are being employed in wave-division multiplexed (WDM) networks to improve bandwidth efficiency by reconfiguring channel capacity on demand. However, abrupt addition/dropping of channels in a WDM network creates variations in combined input power into the erbium doped fiber amplifiers (EDFA). Cross gain saturation, which is caused by amplified spontaneous emission (ASE) in EDFAs, triggers power transients in the surviving channels as shown in Fig. 1, [1]. The speed of a power transient is proportional to the number of cascaded EDFAs [2]. Typical power transients of $+9$ dB/100 μs and -3.5 dB/100 μs are observed in currently deployed OADM-based WDM networks. Performance degradation due to a power transient is caused by the insufficient tracking bandwidth of the AGC and offset loop. Existing solutions to this problem are in the optical domain including dynamic gain equalizers (DGE) [3], [4] and variable optical attenuators (VOA) [5], both of which tend to be expensive. Note that unlike burst-mode CDRs, the power transients in OADM-based WDM networks occur during continuous data transmission. Thus, the techniques employed in designing burst-mode CDRs cannot be employed here.

This paper presents a receiver IC designed to recover data and clock in OC-192 (9.952 Gb/s–12.5 Gb/s) OADM-based SONET WDM metro and long-haul networks. To the best of the authors' knowledge, this is the first reported electrical solution integrated into the receiver IC, to the power transient problem for OC-192 links. An electrical solution is expected to reduce capital expenditures and enable operational simplicity compared to its optical counterparts. The power transient management was added to an existing maximum likelihood sequence estimation (MLSE)-based electronic dispersion compensation (EDC) receiver [6] (see Fig. 2). The MLSE receiver is implemented via an AFE IC in a 0.18 μm, 3.3 V, $f_t = 75$ GHz, SiGe BiCMOS process, and a digital (MLSE equalizer) IC in a 0.13 μm, 1.2 V CMOS process, with both dies packaged in a 23 mm $\times$ 17 mm, 261 pin multi-chip module (MCM). As the MLSE receiver was described in great detail in [6], this paper focuses primarily on the circuit blocks that implement the fast power transient management functionality.

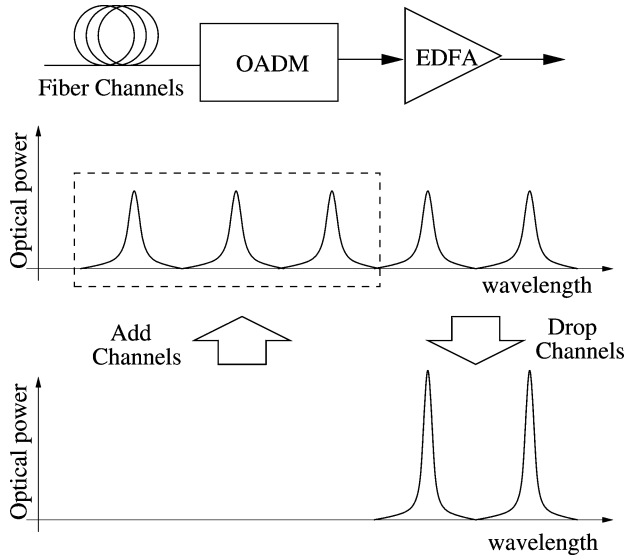

Fig. 1. Power transients in OADM networks.

II. MLSE Receiver Architecture

Fig. 2 shows the architecture of the MLSE receiver. The AFE IC features a power transient-tolerant variable gain amplifier (VGA), a 4-bit 12.5 GS/s analog-to-digital converter (ADC) with an effective number of bits (ENOB) of 3.5 at Nyquist, a dispersion tolerant clock-recovery unit (CRU), and a 1:16 demultiplexer (DEMUX). The digital equalizer IC implements an 8-state MLSE algorithm with a lookback window of 12. The MLSE engine is a parallel, time-reversed, sliding window Viterbi decoder [7]. The decoder utilizes backward recursion to reduce the critical path to a cascade of 8 multiplexers. The MLSE engine is supplied with channel estimates from a low-frequency adaptive channel estimator, which models the nonlinear channel impulse response over three bit-periods.

Manuscript received May 07, 2008; revised June 15, 2008. Current version published December 10, 2008.

H.-M. Bae and J. Ashbrook are with Finisar Corporation, Champaign, IL 61820 USA (e-mail: hyeonmin.bae@finisar.com).

N. Shanbhag and A. Singer are with the Department of Electrical and Computer Engineering, University of Illinois at Urbana-Champaign, Urbana, IL 61801 USA.

Digital Object Identifier 10.1109/JSSC.2008.2006226

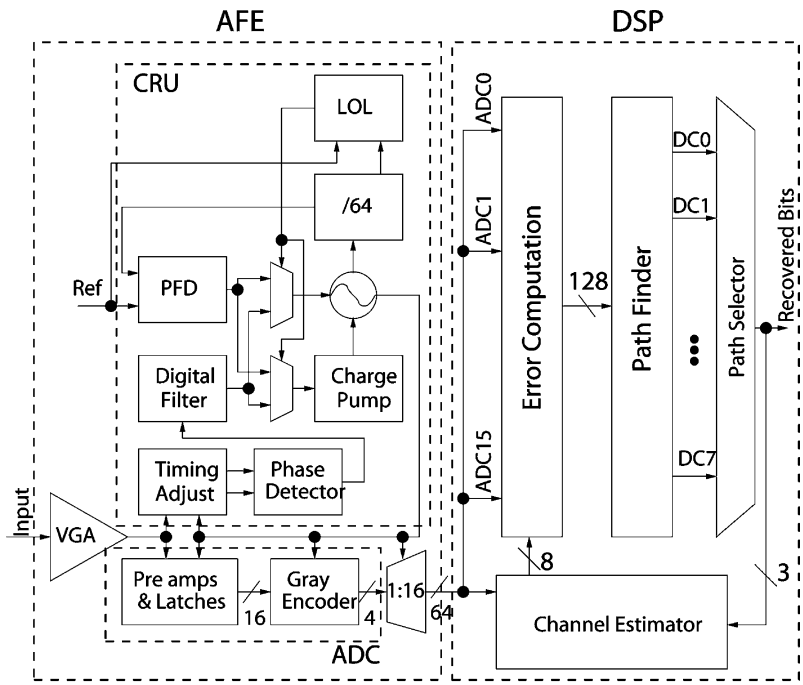

Fig. 2. Top level architecture of MLSE receiver.

The MLSE EDC IC provides a 16-bit output stream compliant with the OFI-SFI4 implementation agreement, thus replacing a conventional CDR-DEMUX.

The power transient management functionality is obtained primarily by adding a fast automatic gain control (AGC), and a high-bandwidth offset cancellation loop (OCL) in the VGA. These will be described in the remainder of the paper.

III. VGA Design

In this section, we begin with the design requirements of the VGA in OADM-based long-haul (LH), and metro area networks (MAN). Then, the architecture and functionality of the proposed VGA is described. Lastly, we describe the key design blocks in the VGA that contribute to the power transient tolerance, including the variable gain offset loop in the OCL, the gain block, the gain controller, and consecutive identical digit (CID)-tolerant peak detector used in the AGC.

A. Design Requirements

Designing a VGA with power transient management for OADM-based networks presents unique challenges as shown in Fig. 3. First, the AGC should track a rapidly changing signal envelope, e.g., 9 dB/100 μs, caused by optical power transients in order to maintain SNR, and linearity, while being insensitive to long strings of CID appearing in the SONET/SDH frame header, which can be as long as 72 ones and zeros alternating in every frame (ITU-T, SDH specification). Second, the OCL in the VGA should suppress transient offsets while being insensitive to 72 CIDs.

The gain block in the VGA and the offset amplifier in the OCL provides a forward gain of A and a feedback gain of G, respectively. The low frequency transfer function $T(s)$ of the VGA is given by

$$T(s) = \frac{\frac{A}{1+AG}\left(1+\frac{s}{p}\right)}{1+\frac{s}{p(1+AG)}}, \tag{1}$$

where p is the single-pole 3 dB cut-off frequency of the offset amplifier. The low frequency pole and zero are located at $p(1+AG)$ and p, respectively.

The offsets of VGA and preceding TIA fluctuate with the optical power transients. Four issues are involved in the design of a power transient tolerant offset loop. First, the bandwidth of the offset amplifier p has to be sufficiently high ($\geq$3.7 KHz) to track the 100 μs offset transient. Second, the offset feedback amplifier should have sufficient gain G, i.e., $(A/(1+AG))$ is sufficiently small to suppress uncompensated offset injected from TIA during the power transient especially in the low gain condition. Third, the VGA should have sufficient dynamic range ($>$40 dB). Fourth, the maximum lower 3 dB cut-off frequency, when the forward gain A is maximum, should be sufficiently low to maintain a constant signal envelope in the presence of long CID. For a 1% droop in the envelope with 72 CID, the low 3 dB cut off frequency should be less than 220 kHz. Insufficient lower 3 dB bandwidth causes pattern dependent offset variation and jitter as well as envelope fluctuation by triggering the fast tracking AGC.

B. VGA Architecture

The VGA block diagram is shown in Fig. 4. The VGA provides a continuous 40 dB tunable gain range, less than 10 mV receiver sensitivity, and greater than 30 dB linearity (third order intermodulation distortion at Nyquist). Three peak detectors, an active ripple canceller, and a gain control unit form the AGC

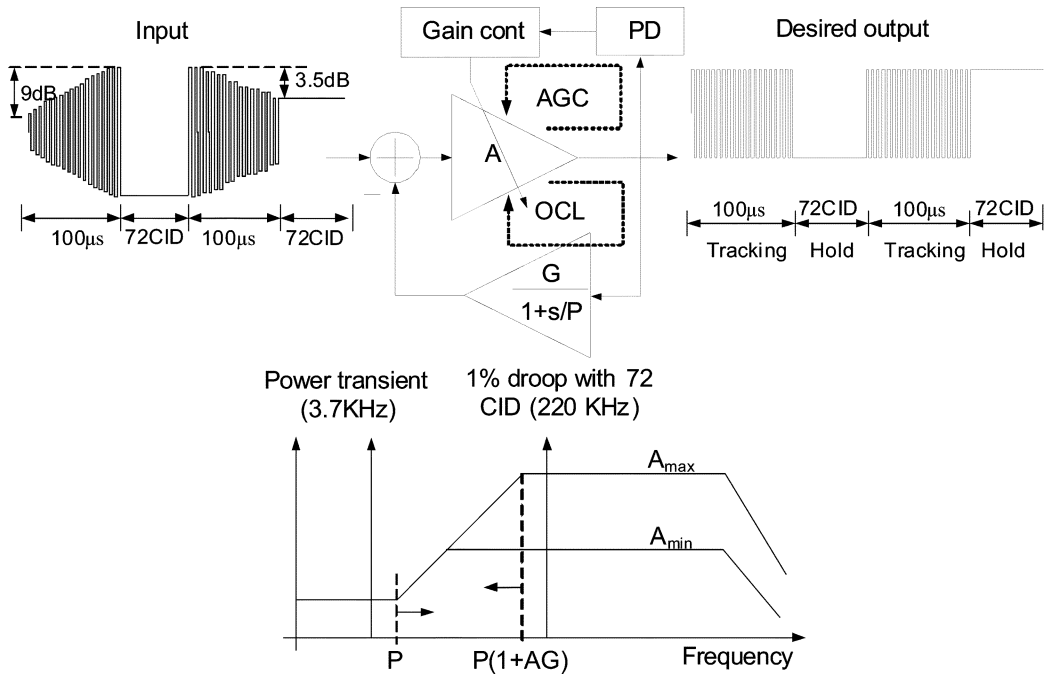

Fig. 3. Desired response of a power transient-tolerant VGA.

loop. The gain control unit maps the peak detector output signal into two separate control signals for the gain block to achieve gain-independent AGC transient response while being insensitive to process, temperature, and supply variations. The gain control unit controls forward and offset gain simultaneously for dynamic gain and bandwidth adjustment. The OCL incorporates a four-point external capacitor ($C_{\rm ext2}$) connection to remove the inductive peaking caused by bonding wires. This scheme suppresses the high frequency offset loop gain, resulting in a flatter forward frequency response. It also helps achieving the desired offset transient response by simplifying the offset loop design. The gain block consists of three cascaded differential amplifier stages. Each stage has an identical gain range of -2 to 13 dB but different voltage headrooms. The first stage has the largest voltage headroom in order to be able to receive a maximum input swing of 2.4 $V_{\rm ppd}$ and attenuate it. Peak detection in the automatic gain loop detects the amplitude of the signal. Pseudo-differential peak detection with active ripple cancellation overcomes bandwidth-ripple trade-off. A reference signal from the ADC to the peak detector sets the target amplitude of the VGA. The output driver includes a common mode feedback (CMFB) loop with offset control. CMFB tracks the common mode voltage information provided by the ADC. The replica bias generator generates replicas of the DC bias points of the gain block and provides them to the gain control block and input termination block in order to achieve process insensitivity.

C. Variable Gain Offset Loop Design

Fig. 5(a) shows the circuit schematic of the first stage of the VGA. Fig. 5(b) depicts the low-frequency response of the VGA without the AC coupling capacitors. With $p = 3.7$ kHz to track offset variations, a moderate $G = 10$, and an expected $A = 0.7 \sim 70$, the maximum lower 3 dB cut-off frequency is around 2 MHz, which is much higher than the upper bound of 220 kHz. In order to solve this problem, the VGA gain A and the offset gain G are simultaneously varied by varying the degeneration resistance $R_{\rm degen} = R_{M_1} \,||\, R_1$ in Fig. 5(a). The VGA gain $A = A_1^3$, where A_1, the single-stage gain, is given by,

$$A_1 = \frac{g_{m1} R_{\rm load}}{1 + \frac{1}{2} g_{m1} R_{\rm degen}}, \tag{2}$$

where g_{m1} is the transconductance of Q_1, and $R_{\rm load} = 0.5R_{M_2} \,||\, R_2$ and $R_{\rm degen}$ are the load and degeneration resistances, respectively. The offset gain G is given by

$$G = A_{\rm oa} \frac{G_1}{A_1} = A_{\rm oa} \frac{g_{m2} R_{\rm degen}}{2}, \tag{3}$$

where $A_{\rm oa}$ is the fixed gain of the offset amplifier in Fig. 4, g_{m2} is the transconductance of Q_2, and G_1 is the gain from the base of Q_2 to the output of the first stage, which is given by

$$G_1 = g_{m2} \left(\frac{R_{\rm degen}}{2} \middle\| \frac{1}{g_{m1}} \right) g_{m1} R_{\rm load}. \tag{4}$$

Varying the degeneration resistance $R_{\rm degen}$ causes G to change in inverse proportion to A, resulting in reduced variations of the lower 3 dB cut-off frequency. If G varies from 10 to 1 when A varies from 0.7 to 70, the variation in low 3 dB cut-off frequency is reduced by an order of magnitude to one decade and the highest cut-off frequency is at 200 kHz as shown in Fig. 5(b). The pole p is set close to 3.7 KHz to place the lower 3 dB frequency below 200 KHz. This is done because the channel estimator in the DSP can track only the residual offset transient, but not the pattern dependency due to an insufficiently small 3 dB frequency. The low feedback gain when the VGA is in the high gain mode does not degrade BER because the transient offset injected from the TIA is small.

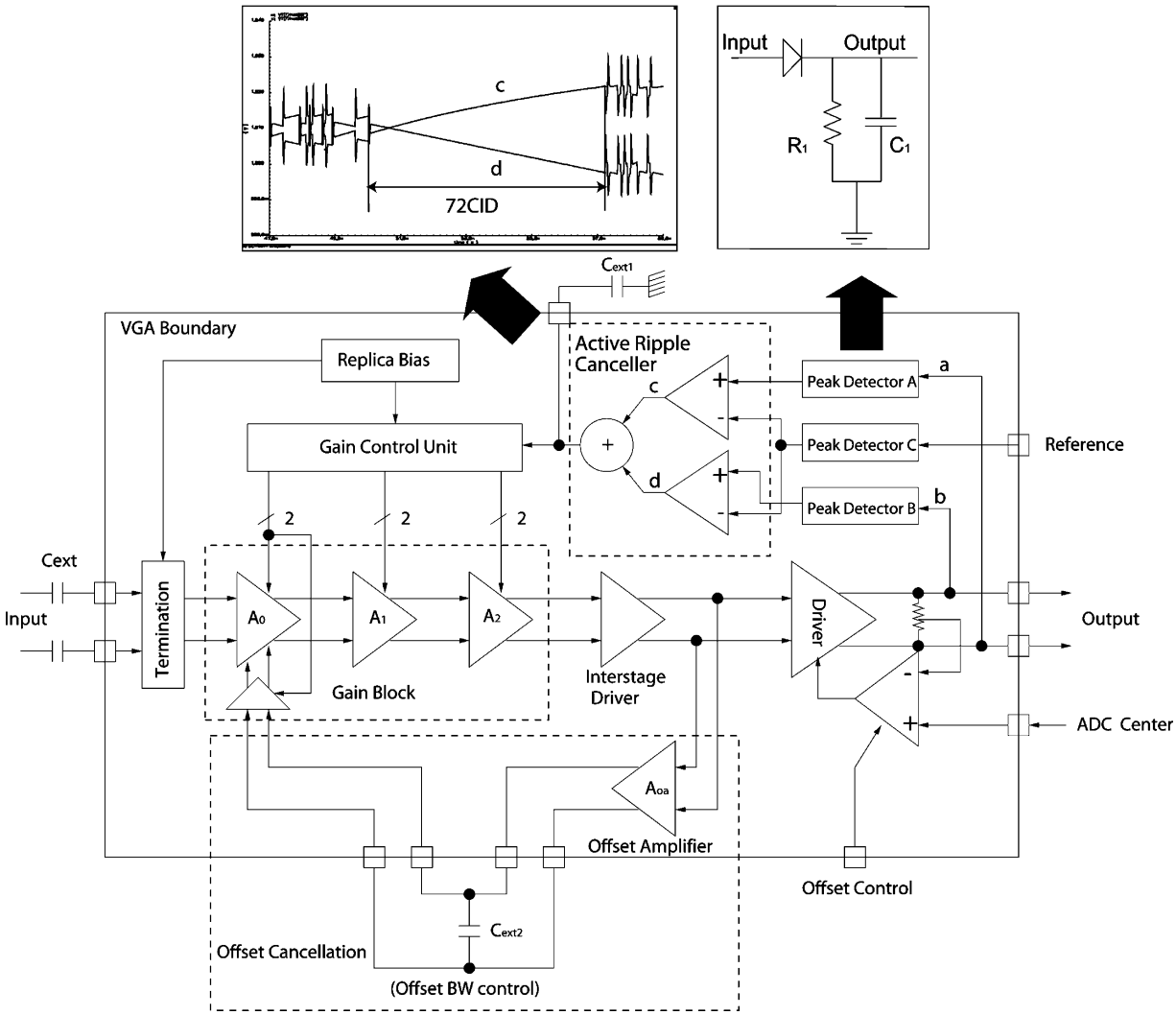

Fig. 4. Block diagram of the power transient-tolerant VGA.

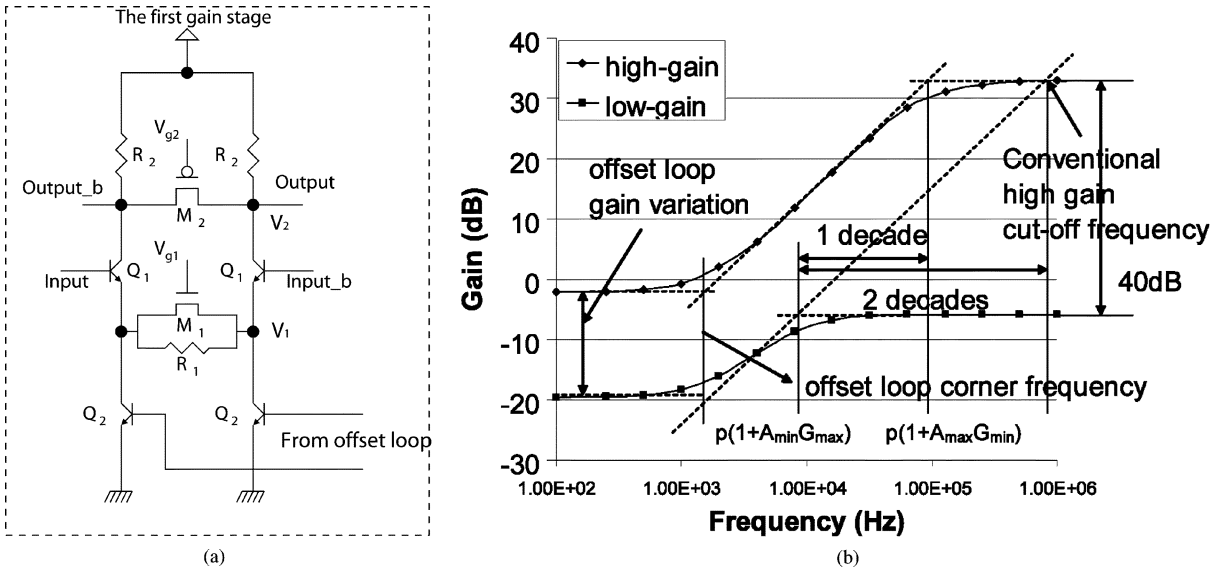

Fig. 5. (a) The circuit diagram of the first stage of VGA and (b) the frequency response of VGA in maximum and minimum gains.

The usage of a peak detector in the offset loop [8] can be a potential solution for this problem as long as the peak detector can discriminate between the power transient and long CID. Individual offset feedback in each stage could mitigate the issue by implementing higher order OCL. However, the number of external pins increases in proportion to the filter order.

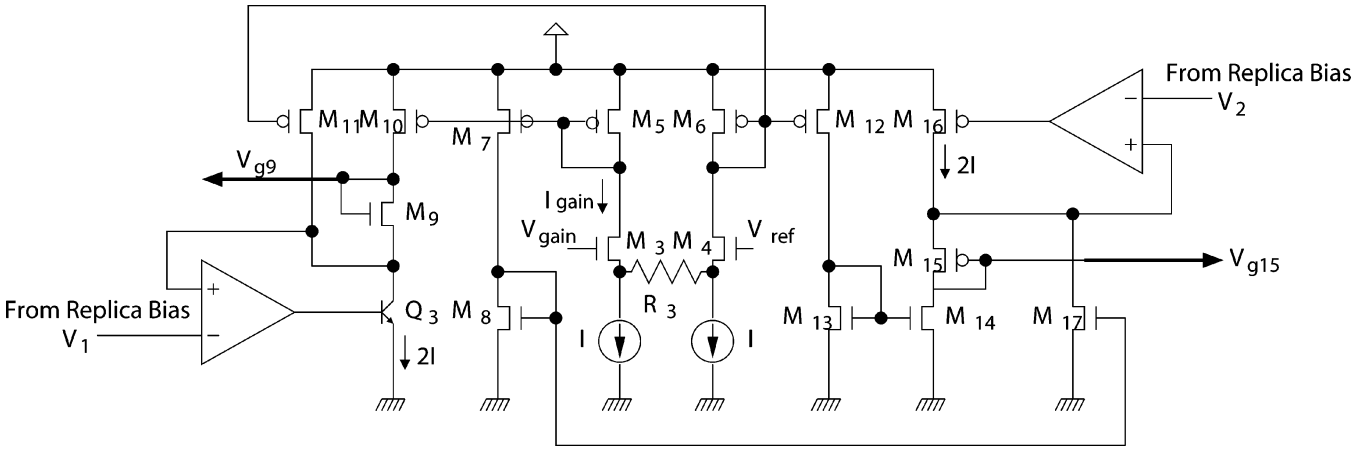

Fig. 6. The simplified circuit schematic of threshold voltage insensitive gain controller.

D. Gain Block and Gain Controller

The gain controller realizes dB-linear gain control with process, temperature, and supply insensitivity. DB-linear gain control provides input power-independent AGC transient response [9]. The gain of the VGA is tuned by controlling the load resistance $R_{\rm load}$ and the degeneration resistance $R_{\rm degen}$ in Fig. 5(a). The performance of the gain block is highly dependent on the process parameters such as the threshold voltage $V_{\rm th}$ and the device transconductance K of M_1 and M_2. The process insensitive gain controller schematic is shown in Fig. 6. The replica bias cell (not shown) generates the DC bias point V_1 and V_2 (see Fig. 5(a)) for the gain controller. The voltage gain of the gain stage A_1 in Fig. 5(a) is given by

$$A_1 \approx \frac{R_{\rm load}}{R_{\rm degen}} = \frac{2R_2}{R_1}\frac{1+2K_1R_1(V_{g1}-V_1-V_{\rm thn})}{1+4K_2R_2(-V_{g2}+V_2-V_{\rm thp})}, \tag{5}$$

where V_{g1} and V_{g2} are the gate voltages of M_1 and M_2, respectively, $V_{\rm thn}$ and $-V_{\rm thp}$ are the threshold voltages of M_1 and M_2, respectively, and K_1 and K_2 are the device transconductances of the triode-region biased transistors M_1 and M_2, respectively, i.e., $I_{\rm ds}=2K(V_{\rm gs}-V_{\rm th})V_{\rm ds}$. The diode-connected NMOS transistor M_9 in Fig. 6 provides a gain control voltage V_{g9} for transistor M_1 (see Fig. 5(a)) equal to

$$V_{g9} = V_1 + V_{\rm thn} + \sqrt{\frac{I_{\rm gain}}{K_9}}, \tag{6}$$

where $I_{\rm gain}$ is the gain control current input which determines the gain, and K_9 is the transconductance of M_9. Similarly, V_{g15} is given by

$$V_{g15} = V_2 - V_{\rm thp} - \sqrt{\frac{(2I-I_{\rm gain})}{K_{15}}}. \tag{7}$$

Substituting (6) and (7) into (5), we obtain

$$A_1 = \frac{2R_2}{R_1}\frac{1+2K_1R_1\sqrt{\frac{I_{\rm gain}}{K_9}}}{1+4K_2R_2\sqrt{\frac{(2I-I_{\rm gain})}{K_{15}}}}, \tag{8}$$

$$= \frac{2R_2}{R_1}\frac{1+2R_1\sqrt{K_1I_{\rm gain}}}{1+4R_2\sqrt{K_2(2I-I_{\rm gain})}}, \tag{9}$$

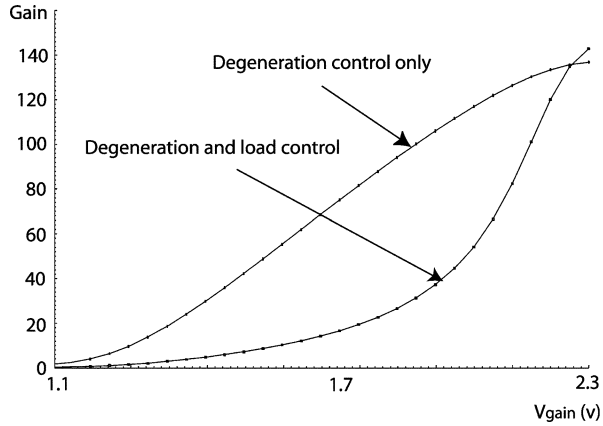

Fig. 7. The gain of VGA with respect to gain control signal.

where $K_1 = K_9$ and $K_2 = K_{15}$. From (9), it is clear that the gain is independent of the threshold voltage and that it is sensitive only to the matching of device transconductance K. The currents in Q_3 and M_{16} in Fig. 6 are fixed at $2I$ in all gain conditions, resulting in a gain-independent phase margin.

For a dB-linear gain control, the voltage gain of the gain stage A should be an exponential function with respect to the gain control signal [9]. Fig. 7 shows the gain of the VGA versus the gain control voltage $(V_{\rm gain})$.

Compared to the degeneration control scheme [6], simultaneous control of degeneration and load resistances exhibits exponential-like gain control characteristics, which is sufficient for achieving the target transient response in the entire gain range. This scheme also enables the VGA to receive a large input signal of 2.4 $V_{\rm ppd}$ and attenuate without source peaking.

E. CID Tolerant Peak Detector Design

The peak detector has to track a 100 μs power transient without causing a BER penalty while being insensitive to long CIDs and dynamic offset variations. The estimated time-constant of the power transient is 43 μs. In order to satisfy these constraints, a conventional peak detector needs to have an RC time constant that is larger than 720 ns in order to suppress the data-dependent ripple to within 1%. At the same time, the RC time constant should be much smaller than 10 μs in

order to track a falling power transient with sufficient damping assuming a closed loop time-constant $\ll 43\ \mu$s. Such a trade-off reduces design margin, resulting in increased process, and temperature sensitivity.

The proposed AGC incorporates three fast peak detectors followed by an active ripple canceller to track dynamic power transients while rejecting the data-dependent peak detector ripple caused by a long string of CIDs. C_1 and R_1 (see Fig. 4) are chosen to balance the charge-up and discharge response in the presence of 72 CIDs. The nominal common-mode voltage V_Q at capacitor C_1 with a pseudo-random bit sequence is

$$V_Q = \frac{1}{2} I_s e^{\frac{V_{\text{in,peak}} - V_Q}{V_T}} R_1 = \frac{I_Q R_1}{2}, \tag{10}$$

where I_s is reverse saturation current, $V_{\text{in,peak}}$ is the peak voltage of the input signal, and $V_T = 26$ mV. The charge-up response V_r with 72 CIDs is dominated by diode I-V characteristics, R_1 and C_1, given by

$$C_1 \frac{dV_r}{dt} + \frac{V_r}{R_1} = I_s e^{\frac{V_{\text{in,peak}} - V_r}{V_T}}, V_r(t=0) = V_Q. \tag{11}$$

Substituting $V_r = V_Q + v_r$ in (11), we get

$$C_1 \frac{dv_r}{dt} + \frac{V_Q + v_r}{R_1} \approx I_Q \left(1 - \frac{v_r}{V_T}\right), \tag{12}$$

where $V_r < V_T$.

Solving (12) and employing (10), we get

$$v_r = V_T \frac{I_Q R_1 - V_Q}{V_T + I_Q R_1} \left(1 - e^{-\left(\frac{V_T + I_Q R_1}{R_1 C_1 V_T}\right) t}\right), \tag{13}$$

$$= \frac{V_Q V_T}{V_T + I_Q R_1} \left(1 - e^{-\left(\frac{V_T + I_Q R_1}{R_1 C_1 V_T}\right) t}\right). \tag{14}$$

Similarly, the discharge response v_f is given by

$$v_f = V_Q \left(e^{-\frac{t}{R_1 C_1}} - 1\right). \tag{15}$$

The Taylor series expansion of (14) and (15) around $t = 0$ is

$$v_r = \frac{V_Q V_T}{V_T + I_Q R_1} \left(\frac{V_T + I_Q R_1}{R_1 C_1 V_T} t - \frac{1}{2} \left(\frac{V_T + I_Q R_1}{R_1 C_1 V_T}\right)^2 t^2 \ldots\right) \tag{16}$$

and

$$v_f = -\frac{V_Q}{R_1 C_1} t + \frac{V_Q}{2 R_1^2 C_1^2} t^2 \ldots, \tag{17}$$

respectively. From (16) and (17), note that the first order terms of v_r and v_f have the identical magnitude but opposite signs in the nominal condition given in (10). The magnitude difference in the second order terms is $(V_Q^2)/(R_1^2 C_1^2 V_T)$, which can be made small with a large $R_1 C_1$. Thus, the single-ended outputs of the peak detectors A and B (see Fig. 4) together form a pseudo-differential signal as long as R_1 and C_1 are sufficiently large to suppress the voltage ripples in the order of V_T. These single-ended outputs when added together generate a common-mode component representing the power transient while canceling out the differential-mode component representing the data-dependent ripples caused by CIDs. An empirical condition for 1% output ripple with active ripple cancellation is given by

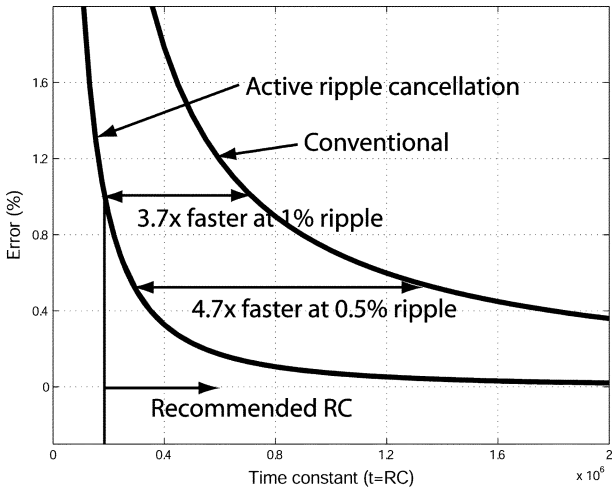

Fig. 8. RC time constant and data ripple.

$$R_1 C_1 > \frac{\Delta t}{3 V_T} V_Q, \tag{18}$$

where Δt is the length of the CID, which is 7.2 ns. Fig. 8 shows the trade-off between $R_1 C_1$ time-constant and the data ripple in conventional and proposed designs. Compared to conventional rectifier-based peak detector designs, the proposed peak detector scheme significantly improves the tracking speed while maintaining the same level of data-dependent ripple. The external capacitance C_{ext1} in Fig. 4 sets the AGC loop bandwidth.

IV. Measured Results

The measurement setup for the MLSE receiver is shown in Fig. 9. A HP8672A clock generator feeds a 9.953–12.5 GHz clock to an Advantest D3186 pattern generator. A commercial 300-pin MZM NRZ transponder with 5 dBm output power is used as a transmitter. Low gain EDFAs are inserted to control OSNR and nonlinearities. OSNR and received power are controlled with two attenuators and an EDFA used as an amplified spontaneous emission noise source. The power transient is created by using a Mach-Zehnder modulator (JDSU X5) driven by a random signal generator to emulate the power transient measured in the field. A PRBS of $2^{31}-1$ sequence and SDH frame data are used for testing of the MLSE EDC receiver. A commercial PIN-TIA with a 3 dB bandwidth of 8 GHz and input sensitivity of -20 dBm at BER of 1×10^{-12} is used for all measurements.

The measured AGC and VGA response to a 10 dB/10 μs power transients is shown in Fig. 10, where the maximum and minimum input powers are -4 dBm and -14 dBm, respectively. The VGA output is monitored through a test buffer integrated in the AFE IC, which has -8 dB gain, >30 dB SFDR, and >8 GHz 3 dB bandwidth. The tracking response of the AGC is captured by monitoring the voltage at the external loop capacitor C_{ext1}. Note that 10%–90% tracking is completed in 8 μs. The envelope of the VGA output remains constant

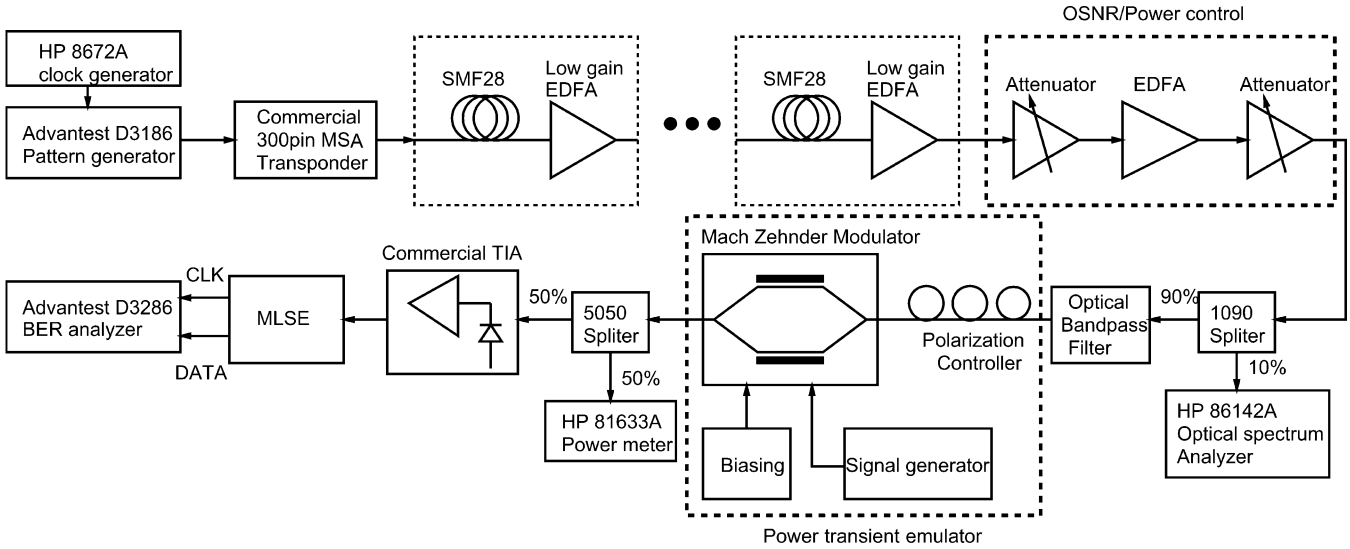

Fig. 9. Power transient measurement setup for the MLSE receiver.

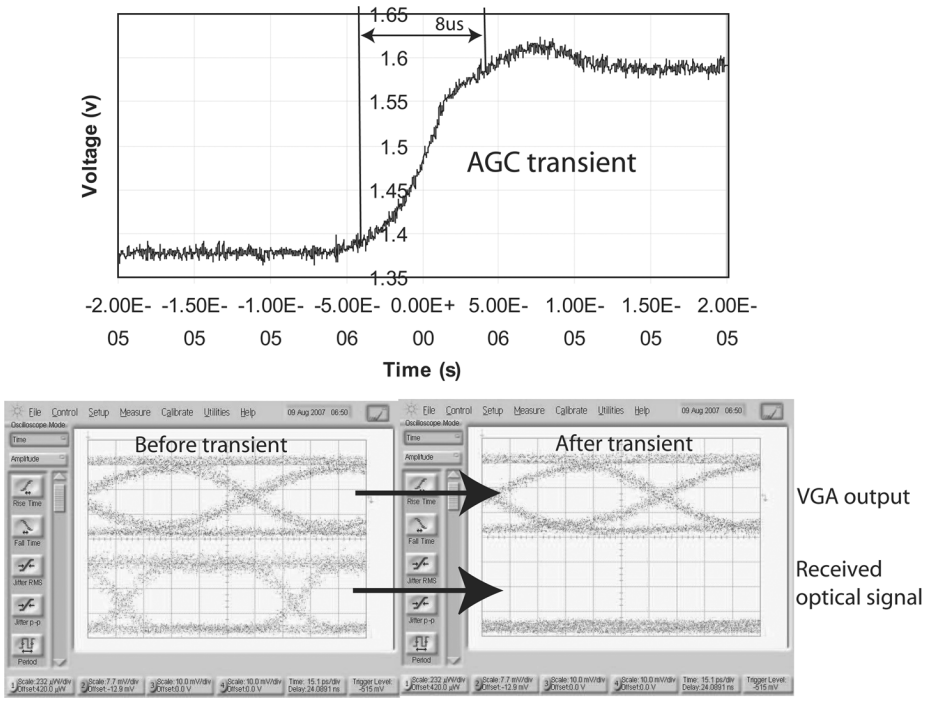

Fig. 10. Measured AGC response in the presence of power transients.

except for a 15 ps shift in the zero crossings due to group delay variation. A group delay variation of 15 ps in a 10 μs window is well within the SONET mask [10]. No variations in BER were observed when operating at a BER of 1×10^{-6} with a $2^{31}-1$ PRBS, which is also well within the operating BER regime of forward error correction (FEC) based links.

Fig. 11 shows the BER plots for a commercially available CDR (Intel 16713XC) and the MLSE receiver in presence of an 8 dB (-14 dBm to -6 dBm) sinusoidal power transient at various frequencies. The optical SNR is adjusted to achieve 2×10^{-7} in the absence of power transients. Two orders-of-magnitude improvement in performance is observed at a typical pre-FEC BER of 10^{-4}.

BER with increasing distance in the presence of 10 dB/100 μs power transient is shown in Fig. 12. OSNR was adjusted to achieve the BER of 10^{-4} at back-to-back. OSNR was adjusted at each point to maintain a constant BER. Algorithm step size μ in the channel estimator has been adjusted to track residual power transient. Back-to-back penalty associated with the algorithm step size was negligible at the BER of 10^{-4}. The MLSE receiver showed 0.4 dB ONSR penalty at 100 km with respect to the power transient. The commercial CDR could not be tested

TABLE I
SUMMARY OF MLSE RECEIVER

Technology	AFE: $0.18\,\mu$m, SiGe BiCMOS (f_T=75 GHz), DE: $0.13\,\mu$m CMOS
Supply voltage	AFE: $3.3\,\text{V}\pm0.3\,\text{V}$, DE: $1.2\,\text{V}/2.5\,\text{V}$(I/O)
Data rate	$9.953\,\text{Gb/s}$ to $12.5\,\text{Gb/s}$
Power	ADC: $1\,\text{W}$, VGA: $0.3\,\text{W}$, PLL: $0.5\,\text{W}$ DEMUX (4 times more complexity than conventional DEMUX): $1\,\text{W}$ LVDS between AFE and DE: $0.7\,\text{W}$ DE : $1\,\text{W}$ Total : $4.5\,\text{W}$
Chip area	AFE: $25\,\text{mm}^2$, DE: $25\,\text{mm}^2$
Number of transistors	AFE: 34,100 = 24,900(FET) + 9200 (BJT), DE: 937,000 (FET)
ADC ENOB (@ $12.5\,\text{GS/s}$)	>3.4 (4-bit mode) with $5\,\text{GHz}$ data >2.8 (3-bit mode) with $5\,\text{GHz}$ data
Output	620 to $781\,\text{Mb/s}$ LVDS
Jitter tolerance	Meets SONET spec in presence of dispersion
Jitter generation	$< 0.5\,\text{ps}_{\text{rms}}$, back-to-back
RX sensitivity	$< 5\,\text{mV}_{\text{pp}}$ differential
CID tolerance	1300 @ 1E-2 BER, $125\,\text{km}$ SMF-28
Packaging	$23\,\text{mm} \times 17\,\text{mm}$, 261ball FBGA (MCM)

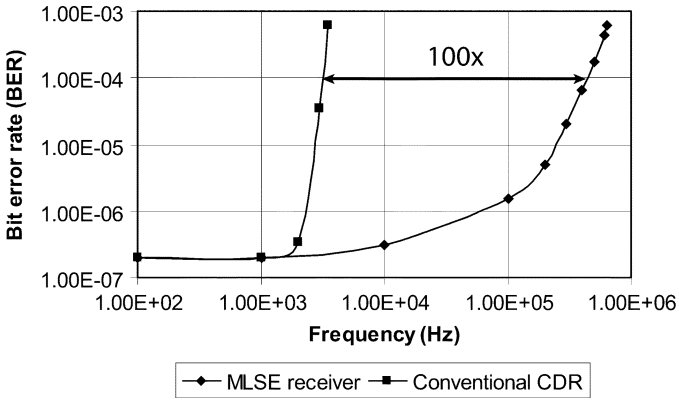

Fig. 11. Measured BER with sinusoidal power transients.

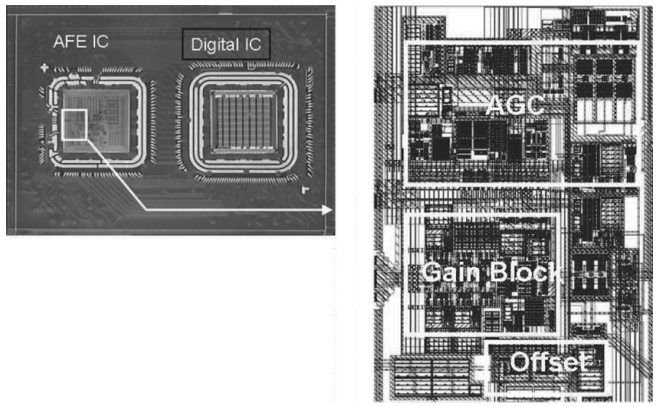

Fig. 13. Microphotograph of MLSE MCM and the layout capture of VGA.

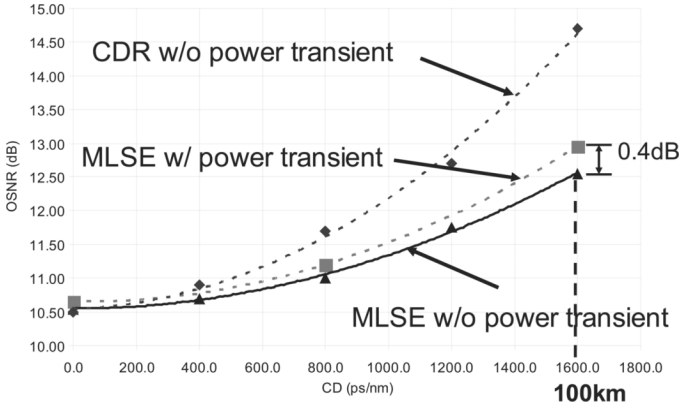

Fig. 12. Measured BER with increasing distance under 10 dB/100 μs power transient.

with the power transient because of its operational instability at the testing conditions.

Fig. 13 shows the photomicrograph of the MLSE MCM with the wire-bonded AFE and DSP ICs, and a detailed layout view of the power transient-tolerant VGAs.

Table I summarizes the features of the two-die solution.

V. CONCLUSION

This paper has described the design of the first fully-integrated OADM power transient-tolerant electronic receiver based on maximum likelihood sequence estimation (MLSE). It can replace expensive optical domain solutions such as DGE and VOA. It demonstrated $100\times$ improvement over a conventional CDR at the BER of 10^{-4} in back-to-back under sinusoidal power transient. The OSNR penalty with 10 dB/100 μs power transient was 0.4 dB up to 100 km at typical pre-FEC BER.

The design of a signal processing-enhanced optical communication receiver for OADM-based WDM metro area networks presents unique challenges spanning algorithmic issues, mixed-signal analog front-end design, and VLSI architectures for implementing the digital signal processing back-end. A cost-effective solution, i.e., a solution that meets the system performance specifications within the power budget, requires joint optimization and innovations of the signal processing algorithms, VLSI architectures and analog and digital integrated circuits.

REFERENCES

[1] M. Karasek, M. Menif, and L. Rusch, "Output power excursion in a cascade of EDFAs fed by multichannel burst-mode packet traffic: Experimentation and modeling," *J. Lightw. Technol.*, vol. 19, pp. 933–940, Jul. 2001.

[2] Y. Sun, A. Srivastava, J. Zyskind, J. Sulhoff, C. Wolf, and R. Tkach, "Fast power transients in WDM optical networks with cascaded EDFAs," *Electron. Lett.*, vol. 33, pp. 313–314, Jul. 1997.

[3] C. Doerr, L. Stulz, R. Pafchek, L. Gomez, M. Cappuzzo, A. Paunescu, E. Laskowski, L. Buhl, H. Kim, and S. Chandrasekhar, "An automatic 40-wavelength channelized equalizer," *IEEE Photon. Technol. Lett.*, vol. 12, pp. 1195–1197, Sep. 2000.

[4] K. Maru, T. Chiba, K. Tanaka, S. Himi, and H. Uetsuka, "Dynamic gain equalizer using hybrid integrated silica-based planar lightwave circuits with $LiNbO_3$ phase shifter array," *J. Lightw. Technol.*, vol. 24, pp. 495–503, Jan. 2006.

[5] T. Lim, C. Ji, C. Oh, H. Kwon, Y. Yee, and J. Bu, "Electrostatic MEMS variable optical attenuator with rotating folded micromirror," *IEEE J. Sel. Topics Quantum Electron.*, vol. 10, pp. 558–562, May 2004.

[6] H. Bae, J. Ashbrook, J. Park, A. Singer, N. Shanbhag, and S. Chopra, "An MLSE receiver for electronic dispersion compensation of OC-192 fiber links," *IEEE J. Solid-State Circuits*, vol. 41, no. 11, pp. 2541–2554, Nov. 2006.

[7] R. Hegde, A. Singer, and J. Janovetz, "Method and apparatus for delayed recursion decoder," U.S. Patent 7,206,363, Apr. 2007.

[8] E. A. Crain and M. H. Perrott, "A 3.125 Gb/s limit amplifier in CMOS with 42 dB gain and 1 μs offset compensation," *IEEE J. Solid-State Circuits*, vol. 41, no. 2, pp. 443–451, Feb. 2006.

[9] W. K. Victor and M. H. Brockman, "The application of linear servo theory to the design of AGC loops," in *Proc. IRE*, 1960, pp. 234–238.

[10] "Synchronous optical network (SONET) transport systems: Common generic criteria," Telcordia Technologies, no. 3, GR-253-CORE, Sep. 2000.

Hyeon-Min Bae received the B.S. degree in electrical engineering from Seoul National University, Seoul, Korea, in 1998 and the M.S. and Ph.D. degrees in electrical and computer engineering from the University of Illinois at Urbana-Champaign in 2001 and 2004, respectively.

From 2001 to 2007, he lead the analog and mixed-signal design aspects of OC-192 EDC-based CDRs at Intersymbol Communications, Inc., Champaign, IL. Since 2007, he has been with Finisar Corporation after its acquisition of Intersymbol Communications Inc. He is also a Visiting Lecturer with the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory at the University of Illinois at Urbana-Champaign, where he is teaching and engaged in research projects related to high-speed clock-data recovery systems on a part-time basis.

Dr. Bae received the Silver Medal in Samsumg Humantech Thesis Prize in 1998 and the 2006 IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award.

Jonathan Ashbrook received the B.S. and M.S. degrees in electrical engineering from the University of Illinois at Urbana-Champaign in 1998 and 2000.

From 2000 to 2002, he worked at IBM in Essex Junction, VT, designing high performance semi-custom ASICs. In 2002 he joined venture-funded Intersymbol Communications in Champaign, IL. Until 2007 he lead the development of custom DSP chips for EDC-based OC-192 chipsets. During this time, he was awarded the 2006 IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award. In 2007 Intersymbol Communications was acquired by Finisar Corporation where he continues to lead the digital development for optical networking chipsets for OC-192 applications and beyond. He currently holds two patents in the area of high performance memory design.

Naresh R. Shanbhag (F'06) received the Ph.D. degree from the University of Minnesota in 1993 in electrical engineering.

From 1993 to 1995, he worked at AT&T Bell Laboratories at Murray Hill, NJ, where he was the lead chip architect for AT&T's 51.84 Mb/s transceiver chips over twisted-pair wiring for Asynchronous Transfer Mode (ATM)-LAN and very high-speed digital subscriber line (VDSL) chip-sets. Since August 1995, he has been with the Department of Electrical and Computer Engineering and the Coordinated Science Laboratory, University of Illinois at Urbana-Champaign, where he is presently a Professor. His research interests are in the design of integrated circuits and systems for broadband communications including low-power/high-performance VLSI architectures for error-control coding, equalization, as well as digital integrated circuit design. In 2000, he cofounded and served as the chief technology officer of Intersymbol Communications, Inc., a venture-funded fabless semiconductor start-up that provided mixed-signal ICs for electronic dispersion compensation of OC-192 optical links. In 2007, Intersymbol Communications, Inc., was acquired by Finisar Corporation, Inc., where he is presently serving as a Senior Scientist on a part-time basis. He has numerous publications in this area and holds four US patents. He is also a coauthor of the research monograph *Pipelined Adaptive Digital Filters* (Kluwer Academic, 1994).

Dr. Shanbhag became an IEEE Fellow in 2006, received the 2006 IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award, the 2001 IEEE TRANSACTIONS ON VLSI CIRCUITS Best Paper Award, the 1999 IEEE Leon K. Kirchmayer Best Paper Award, the 1999 Xerox Faculty Award, the Distinguished Lecturership from the IEEE Circuits and Systems Society in 1997, the National Science Foundation CAREER Award in 1996, and the 1994 Darlington Best Paper Award from the IEEE Circuits and Systems Society. He served as an Associate Editor for the IEEE TRANSACTIONS ON CIRCUITS AND SYSTEMS: PART II (1997–1999) and the IEEE TRANSACTIONS ON VLSI CIRCUITS (1999–2002). He is currently serving on the technical program committees of major international conferences including the IEEE International Solid-State Circuits Conference (ISSCC), the International Conference on Computer-Aided Design (ICCAD), the International Symposium on Low-Power Design (ISLPED), and the International Conference on Acoustics, Speech and Signal Processing (ICASSP).

Andrew C. Singer (SM'05) received the S.B., S.M., and Ph.D. degrees, all in electrical engineering and computer science, from the Massachusetts Institute of Technology in 1990, 1992, and 1996, respectively.

Since 1998, he has been on the faculty of the Department of Electrical and Computer Engineering (ECE) at the University of Illinois at Urbana-Champaign, where he is currently an Associate Professor in the ECE department, a Research Associate Professor in the Coordinated Science Laboratory, and a Willett Faculty Scholar. In 2005, he was appointed as the Director of the Technology Entrepreneur Center (TEC) in the College of Engineering and has started several successful initiatives in the Center since. In 2000, he cofounded and served as the chief executive officer of Intersymbol Communications, Inc., a venture-funded fabless semiconductor start-up that provides mixed-signal ICs for electronic dispersion compensation of OC-192 optical links. In 2007, Intersymbol Communications, Inc., was acquired by Finisar Corporation, Inc., where he is presently serving as a Senior Scientist on a part-time basis. During the academic year 1996, he was a Postdoctoral Research Affiliate in the Research Laboratory of Electronics at MIT. From 1996 to 1998, he was a Research Scientist at Sanders, A Lockheed Martin Company in Manchester, New Hampshire, where he designed algorithms, architectures and systems for a variety of DOD applications. His research spans statistical signal processing and communication systems and machine learning.

Dr. Singer was a Hughes Aircraft Masters Fellow, and was the recipient of the Harold L. Hazen Memorial Award for excellence in teaching in 1991. He received the National Science Foundation CAREER Award in 2000, the Xerox Faculty Research Award in 2001, was named a Willett Faculty Scholar in 2002, and received the IEEE JOURNAL OF SOLID-STATE CIRCUITS Best Paper Award in 2006. He serves as an Associate Editor for the IEEE TRANSACTIONS ON SIGNAL PROCESSING and is a member of the MIT Educational Council, Eta Kappa Nu and Tau Beta Pi.