11.8 A 10Gb/s MLSE-based Electronic-Dispersion-Compensation IC with Fast Power-Transient Management for WDM Add/Drop Networks

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Optical add/drop multiplexers (OADM) are being used in WDM networks to improve bandwidth efficiency by reconfiguring channel capacity on-demand. However, abrupt addition/dropping of channels creates cross-gain saturation in erbium-doped fiber amplifiers triggering fast power transients in the surviving channels (see Fig. 11.8.1). Typical power transients of +9dB/100µs and -3.5dB/100µs are observed in currently deployed OADM-based WDM networks. Existing solutions to this problem are in the optical domain such as dynamic gain equalizer (DGE) and variable optical attenuator (VOA).

In this paper, a receiver IC is designed to recover data and clock in OC-192 (9.952Gb/s-12.5Gb/s) OADM-based SONET WDM metro and long-haul networks. This is an electrical solution integrated into the receiver IC to address the power-transient problem for OC-192 links. An electrical solution reduces the cost and simplifies the operation. As power-transient management is added to an existing MLSE-based electronic dispersion compensation (EDC) receiver [1] (see Fig. 11.8.2), in this paper, the focus is primarily on the blocks related to the power-transient management functionality. The MLSE receiver is implemented via an AFE IC in a 0.18µm 3.3V f_t=75GHz SiGe BiCMOS process, and a digital (MLSE equalizer) IC in a 0.13µm 1.2V CMOS process, with both dies packaged in a 23×17mm² 261-pin multi-chip module (MCM).

Figure 11.8.2 shows the architecture of the MLSE receiver. The AFE IC features a VGA, a 4b ADC, a dispersion-tolerant clock-recovery unit (CRU), and a DEMUX. The bulk of power-transient management functionality is in the AFE IC via the VGA incorporating a fast automatic gain control (AGC) and a high-bandwidth offset-cancellation loop (OCL). The digital IC compensates for any residual variations.

Designing a VGA with power-transient management for OADM-based networks presents unique challenges. First, the AGC should track a rapidly changing signal envelope, e.g., 10dB/100µs, caused by optical power transients while being insensitive to the data ripple at the peak-detector output caused by long strings of consecutive identical digits (CID). Second, the AGC loop causes the VGA output offset to change in the presence of a power transient. The preceding TIA output offset will also vary with a power transient. Thus, the 3dB bandwidth and the OCL feedback gain should be high enough to suppress these variations. However, high-gain and bandwidth of the OCL shifts the lower 3dB cut-off frequency of the VGA to higher frequencies resulting in a decaying envelope with low-frequency signal patterns. The estimated time-constant of the power transient is 43µs assuming a single-pole response (equivalent 3 dB bandwidth is 3.7kHz). The transient response of the AGC and the OCL determines the ability of the receiver to manage power transients.

The VGA block diagram (Fig. 11.8.3) shows that the gain block and the offset amplifier form a low-frequency feedback loop. The AGC incorporates 3 fast peak detectors followed by an active ripple canceller to track dynamic power transients while being insensitive to the data-dependent peak detector ripple caused by a long string of CID. The capacitance C_1 in the peak detector (Fig. 11.8.3) is made small to enhance tracking performance. Resistor R_1 is chosen to make node X have similar charge-up and discharge transients in the presence of 72 CID (SONET specification). Capacitance C_1 and the voltage at node X determine the charge-up transient, and C_1, and the input resistance of Q_1 determines the discharge transient. The single-ended outputs of peak detectors A and B together form a pseudo-differential signal, that when added together generates a common-mode component representing the power transient while canceling out the differential-mode component representing the data-dependent ripples caused by CID. The external capacitance C_{ext1} sets the AGC loop bandwidth.

The gain block in the VGA and the offset amplifier in the OCL provide a forward gain of A and a feedback gain of G, respectively. Thus, the lower 3dB cut-off frequency of the VGA output is given by $p(1+GA)$, where p is the single-pole 3dB frequency of the offset amplifier. Figure 11.8.4 depicts the low-frequency response of the VGA without the AC-coupling capacitors. With p=3kHz to track offset variations, a moderate G=10, and an expected A=0.7 to 70, the highest lower 3dB cut-off frequency is around 2MHz, which is much higher than the upper bound of 220 kHz needed to suppress variations in the output signal envelope to within 1% in the presence of 72 CID. In order to solve this problem, the VGA gain A and the offset gain G are simultaneously varied by varying the load and the degeneration resistance in Fig. 11.8.4. The variation in degeneration resistance causes G to change in inverse proportion to A, resulting in reduced variations of the lower 3dB cut-off frequency. The variable load resistance linearizes the AGC loop gain to achieve the desired transient AGC loop response over the entire dynamic range. With G varying from 10 to 1 when A varies from 0.7 to 70, the variation in low 3dB cut-off frequency is reduced by an order of magnitude to one decade and the highest cut-off frequency is at 200kHz as shown in Fig. 11.8.4. The offset feedback loop incorporates a 4-point external capacitor connection (C_{ext2}) to remove the inductive peaking caused by bonding wires. This scheme suppresses the high-frequency offset loop gain, resulting in a flatter forward frequency response. It also helps achieving desired offset transient response by simplifying the offset loop design.

The measured AGC and VGA response to 10dB/10µs power transients are shown in Fig. 11.8.5, where the minimum and maximum input powers are -4dBm and -14dBm, respectively. A JDSU ERM568 PIN-TIA and a 2^{31}-1 PRBS is used. The VGA output is monitored through a test buffer integrated in the AFE IC. The tracking response of the AGC is captured by monitoring the voltage at the external loop capacitor C_{ext1}. Note: 10%-to-90% tracking is completed in 8µs. The envelope of the VGA output remains constant except for a 15ps shift in the zero crossings due to group-delay variation. A group-delay variation of 15ps in a 10µs window is well within the SONET mask [2]. No variations in BER are observed when operating at a BER of 1×10^{-6} with a 2^{31}-1 PRBS, which is also well within the G.709 FEC operating regime. Figure 11.8.6 shows the BER plots for an Intel 16713XC CDR and the MLSE receiver in presence of an 8dB (-14dBm ~ -6dBm) sinusoidal power transient at various frequencies. The optical SNR is adjusted to achieve 2×10^{-7} in the absence of power transients. Two orders-of-magnitude improvement in performance is observed at a typical pre-FEC BER of 10^{-4}. Other performance metrics of the MLSE receiver such as jitter tolerance and dispersion compensation are similar to those reported in [1] and hence are not shown. Figure 11.8.7 shows the micrograph of the MCM.

References:

[1] H. Bae, J.B. Ashbrook, J. Park et al., "An MLSE Receiver for Electronic-Dispersion Compensation of OC-192 Links," *IEEE J. of Solid-State Circuits*, vol. 41, no. 11, pp. 2541-2554, Nov. 2006.

[2] Synchronous Optical Network (SONET), GR-253-CORE, Issue 3, 2000.

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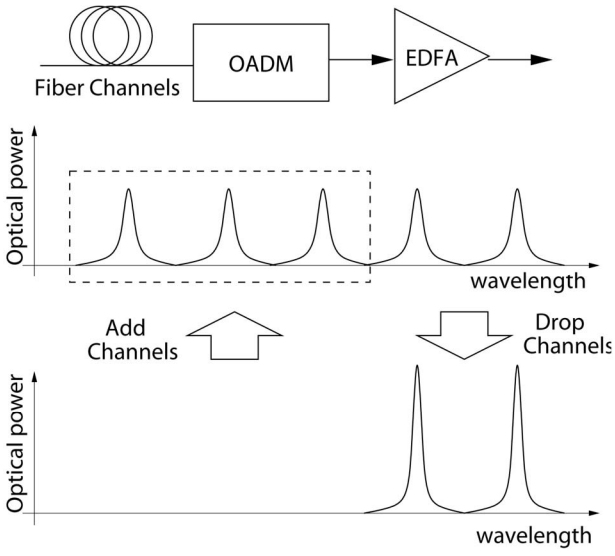

Figure 11.8.1: Optical power transients in an OADM-based WDM network.

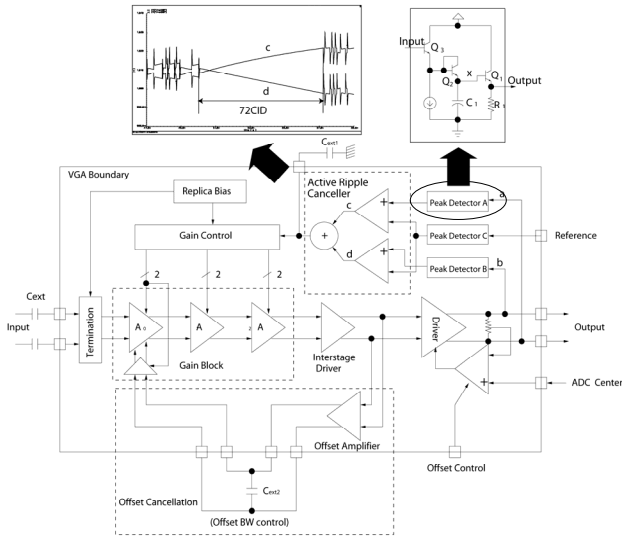

Figure 11.8.3: Block diagram of the VGA with an AGC and offset-cancellation loop.

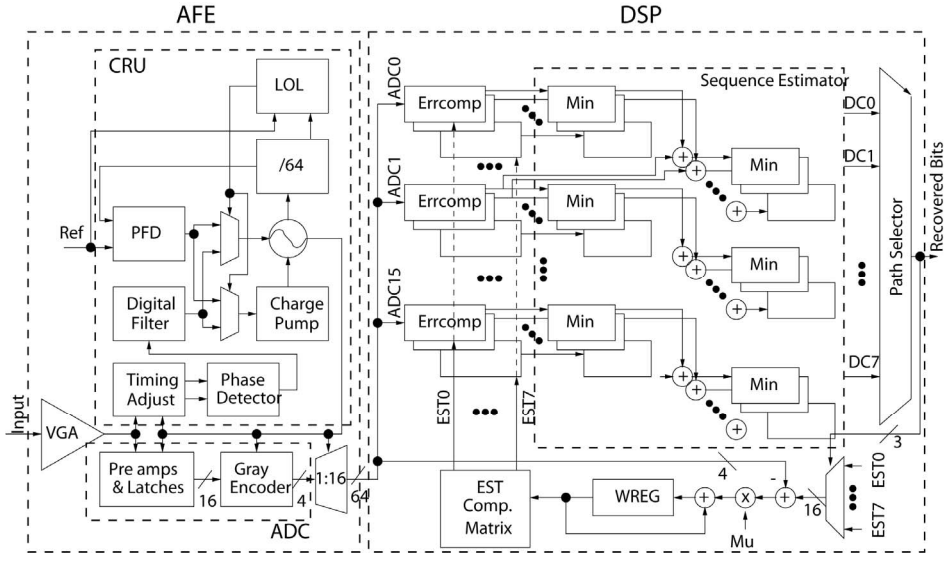

Figure 11.8.2: The architecture of the MLSE receiver.

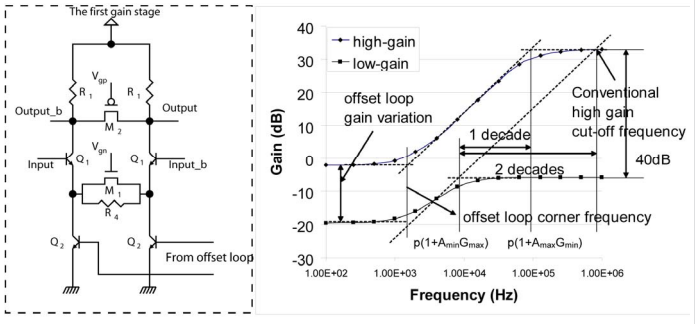

Figure 11.8.4: First stage of the gain block and the low-frequency response of the VGA.

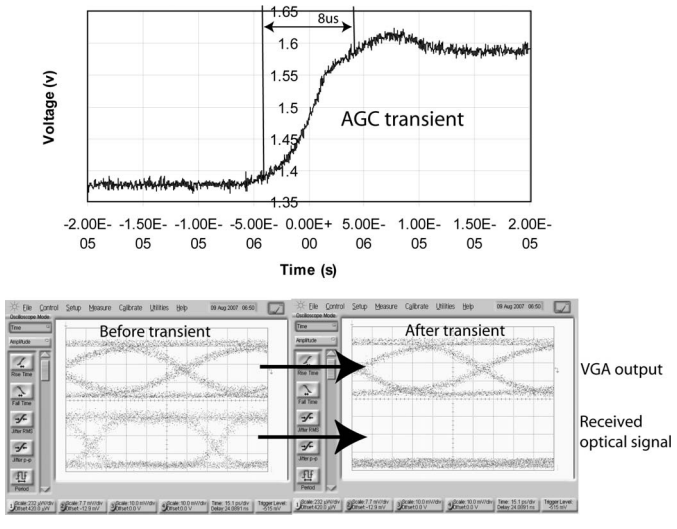

Figure 11.8.5: Measured AGC and VGA responses with ±10dB/10µs optical power transients.

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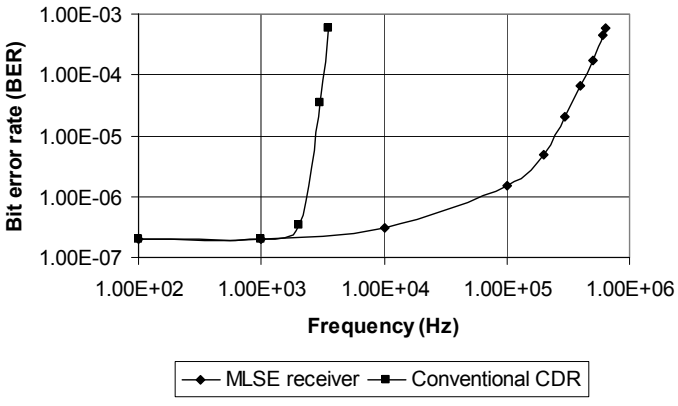

Figure 11.8.6: Measured BER with sinusoidal power transients.

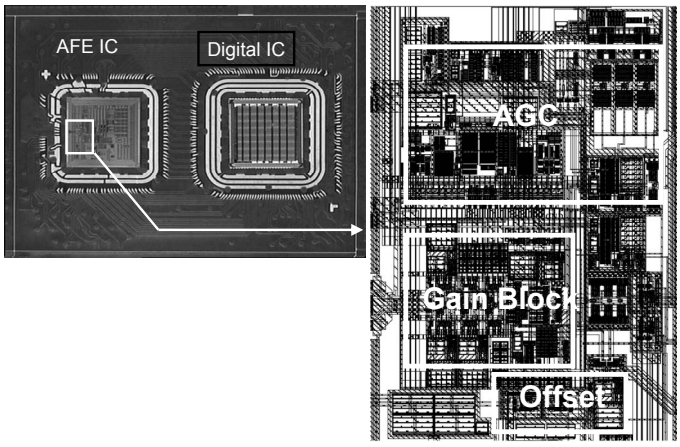

Figure 11.8.7: Micrographs of the AFE and digital (MLSE) dies in an MCM.

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