A 0.13μm 6GHz 256x32b Leakage-tolerant Register File

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Abstract

This paper describes a 256x32b 4-read, 4-write ported register file for 6GHz operation in 1.2V, 0.13μm technology. The local bitline uses a pseudo-static leakage tolerant scheme to achieve 8% faster read performance and 36% higher DC noise robustness (with 6x active leakage reduction) compared to dual-Vt scheme optimized for high-performance.

Introduction

Multi-ported register files are performance-critical processor components with single-cycle read/write latency and throughput requirement. Large number of read-select entries per port forces wide-OR dynamic local bitline structures. Increasing Ioff with process scaling degrades dynamic circuit active leakage and noise tolerance, requiring alternate robust schemes to sustain high performance demand. A 256x32b register file in 1.2V, 0.13μm dual-Vt CMOS technology with copper interconnect [1] is described for 6GHz operation. Single-ended read-select and bit-line signaling is used throughout to reduce wiring congestion, enabling 4-read, 4-write port capability in a dense layout occupying 356μmx89μm (Fig. 8). A pseudo-static local bitline (LBL) scheme that enables 16 cells/bitline with all low-Vt transistors is proposed for improved leakage and noise tolerance.

RF organization

Fig. 1 shows organization of the 4-read, 4-write ported 256-wordx32-bits/word register file. 8-bit read/write address per port is decoded in previous cycle and fed as read/write select signals into the 256x32b array. Each LBL (1 per port) supports single-ended read on 16 cells with two-way merge via static NAND. Fig. 2 shows the register file bitcell, with symmetric loading of 2 read ports on each side of storage cell for optimal cell stability [2]. Matched pass transistors on each side of the storage cell enable single-ended write. Fig. 3(a)-(b) shows the local and global bitline (GBL) scheme. Data from storage cell is read by two access transistors per word (M1 and M2), forming a dynamic 16-way OR. The 8-way GBL multiplexes the NAND outputs to deliver a 32b word per read-port. Fig. 3(c) shows the read/write 2Φ domino timing plan with fully time-borrowable Φ2 boundary.

LBL and GBL dynamic OR's are susceptible to noise due to high active leakage during evaluate when precharged domino node should stay high. LBL is particularly more sensitive than GBL due to smaller domino node stored charge (0.1x compared to GBL) and a wider dynamic OR structure (16-way for LBL vs. 8-way for GBL). Low-Vt on the domino pulldown NMOS transistors (M1 and M2) for LBL does not meet minimum noise margin floor whereas low-Vt on GBL achieves sufficient noise immunity. The contending dual-Vt LBL scheme optimized for high-performance uses high-Vt on the read-select transistors (M1) and low-Vt on the bit-cell data transistors (M2). Low-Vt is used for all other transistors. Worst-case domino node active leakage is reduced by 10x (Fig. 4). However, read performance penalty is 12%.

Fig. 5 shows the proposed pseudo-static leakage tolerant LBL circuit with read-select and bit-cell data inputs swapped. Static PMOS sustainers Px precharge the stack nodes Vs to Vcc every cycle. A static 2-input NOR pre-conditions the data input to Gnd, achieving Vgs = -Vcc reverse-bias on M1. This reduces active leakage by 58x even with using low-Vt transistors on M1 and M2 (6x better than dual-Vt). Performance penalty compared to dual-Vt due to higher input capacitance and slow static NOR pullup is offset by (i) low-Vt usage throughout read-path and (ii) 50% downsized keeper transistor Pk that reduces contention during evaluate. Complete read-path operates at 165ps, 8% faster than dual-Vt and only 4% slower than all low-Vt best-speed solution (Table 1). Simulations include layout-extracted parasitics (Fig. 8), with maximum LBL and GBL lengths of 115μm and 1092μm respectively.

DC Noise Robustness

To compare noise tolerance of proposed LBL scheme with conventional low-Vt and dual-Vt schemes, worst-case leakage and input DC noise conditions are setup for each. DC robustness is evaluated as unity-gain noise margin at output of LBL-merge NAND gate normalized to Vcc. LBL domino node DC droop with worst-case leakage and no input noise is 5x (25x) lower for proposed scheme than dual-Vt (low-Vt) scheme (Fig. 6). With worst-case leakage and input DC noise, proposed scheme has 36% (197%) higher robustness than dual-Vt (low-Vt) scheme (Table 2). Fig. 7 shows DC robustness-performance trade-off with LBL keeper upsizing. Increased keeper contention degrades speed but improves robustness. The proposed leakage-tolerant scheme sustains robustness and speed advantage over dual-Vt scheme with keeper upsizing.

Conclusion

A 1.2V, 0.13μm 256x32b register file operating at 6GHz offers 8% higher performance than dual-Vt LBL scheme with 36% DC noise robustness improvement.

Acknowledgement

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References

[1] S.Tyagi et al, 2000 IEDM Tech. Digest, pp. 567-570.
[2] M.Golden et al, 1999 VLSI Circuits Symp. Digest, pp. 105-108.

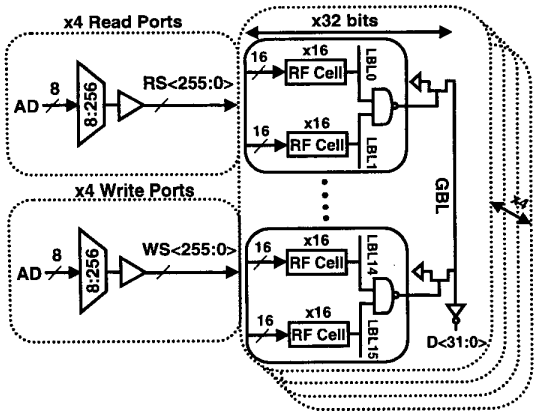

Fig. 1. Register file organization.

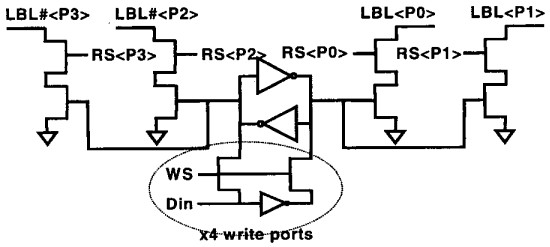

Fig. 2. Symmetric register file bitcell.

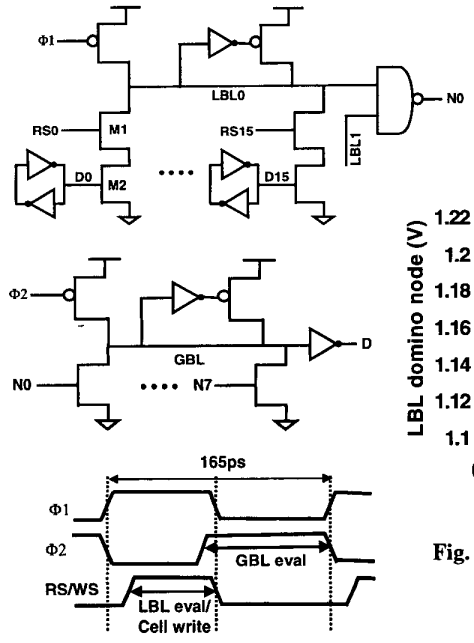

Fig. 3 (a) LBL scheme, (b) GBL scheme, (c) Clocking.

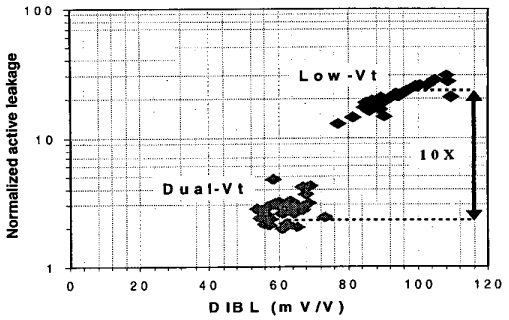

Fig. 4. 1.2V, 0.13μm leakage measurement.

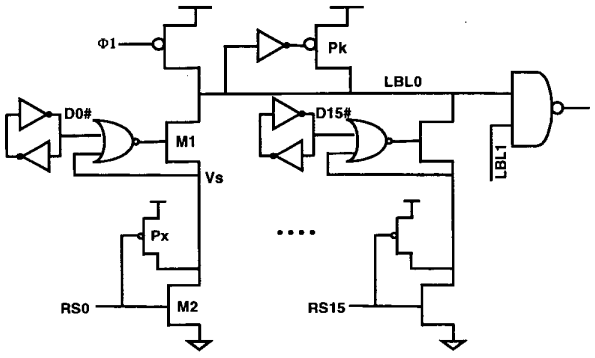

Fig. 5. Proposed LBL scheme.

LBL Scheme	Read Delay
Low-Vt	158ps
Dual-Vt	178ps
This work	165ps

LBL Scheme	DC robustness
Low-Vt	0.072
Dual-Vt	0.157
This work	0.214

Table 1 & 2. Read delay, DC robustness simulations (1.2V, 110C).

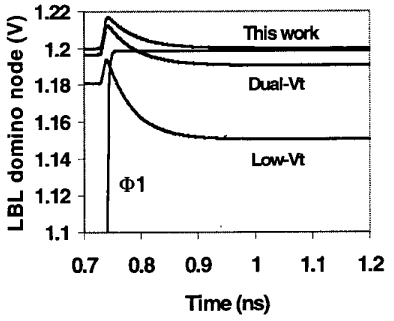

Fig. 6. LBL domino node DC droop.

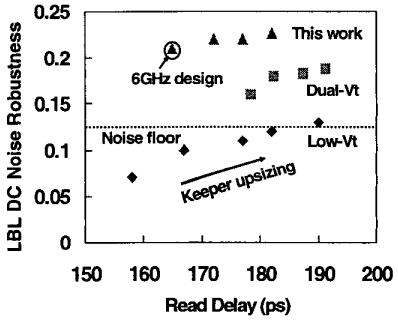

Fig. 7. Robustness-Delay trade-off.

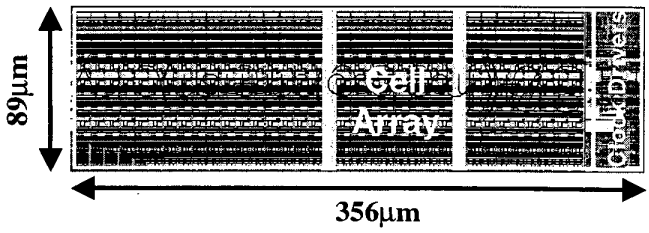

Fig. 8. Register file layout.