Low-power CDMA Multiuser Receiver Architectures

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Abstract — Presented in this paper are low-power, reconfigurable adaptive CDMA multiuser receiver architectures developed via *dynamic algorithmic transforms* (DAT). The architectures achieve low-power operation via run-time reconfiguration of receiver complexity to match the requirements of a time-varying multiuser channel. Simulation results with $0.25\mu m$, $2.3V$ CMOS technology parameters indicate that the proposed architectures have high resistance to the near-far problem, and can achieve up to 60.4% in power savings compared to architectures without DAT depending on the interference situation.

1 Introduction

The standards for third generation (3G) wireless systems such as UMTS and IMT–2000 specify variable data-rates (up to 384 kbps for wide area coverage and upto 2 Mbps for local area coverage) at chip rates of 0.9216/3.6864/ 14.7456 Mcps, high spectral efficiency and high flexibility [1] for providing multimedia services. The challenge is in providing these high data-rates and services in the presence of multiple access/user interference (MAI) and the so called near-far problem (transmitters near the receiver overwhelm the desired user who can be far away).

Code division multiple-access (CDMA) scheme is part of most standards proposals. Current CDMA-based wireless systems employ the *single-user receiver* (decorrelator) due to its extremely low hardware complexity. However, the performance of the single-user receiver deteriorates significantly in the presence of MAI. Previous work has demonstrated that *multiuser detection* (MUD) schemes can vastly improve the performance of CDMA receivers. However, the optimal multiuser detector [2] is complex and in practice impossible to implement for any reasonable number of users. This is also true for most of the suboptimal multiuser detection schemes due to the matrix inversions involved.

Not much work has been done in the past on implementations of multiuser detectors [3]. Further, none exploit the fact that the detector complexity is a function of the number of users present and the various modes of operations specified in the standards. In addition, standards usually specify the

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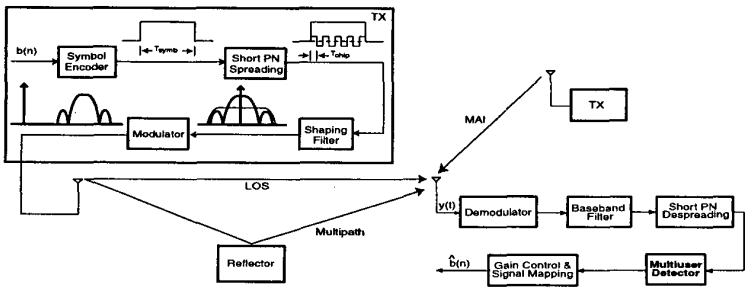


Figure 1: A third generation wireless system block diagram.

worst case scenario and thus most transceivers are overdesigned for the nominal and worst cases. The time-varying nature of the channel, flexibility demanded by 3G wireless standards and the mobility requirements make reconfigurable architectures an attractive approach for low-power solutions. Most approaches to reconfigurable DSP [4] seek to maintain the flexibility of fully programmable solutions with a corresponding power and throughput penalty (an exception being the approach in [4] which explicitly targets low-power). In contrast, our approach to reconfigurable DSP is to exploit the energy and throughput efficiencies inherent in an ASIC solution and add in just the right amount of application-dependent flexibility. The resulting solution, termed *application specific reconfigurable IC* (ASRIC), is extremely well-suited for the low-power mobile multimedia communication systems that the 3G standards are expected to stimulate. Recently, we have proposed *dynamic algorithm transforms* (DAT) [5], a design methodology for such low-power ASRICs.

In this paper, we develop low-power, reconfigurable multiuser receiver architectures via dynamic algorithm transforms (DAT) [5, 6]. These architectures require relatively low hardware complexity and can achieve high throughput while preserving the performance improvement inherent in multiuser detection.

2 Algorithms and Architectures for MUD

In this section, we provide the necessary background of an adaptive CDMA MUD algorithm and propose two architectures.

2.1 Adaptive MUD Algorithm

Fig. 1 shows the block diagram of a typical 3G wireless system receiver [1]. The symbols to be transmitted are first mapped to an antipodal format (i.e., either 1 or -1). Each symbol $b(n)$ is then multiplied by an N-chip spreading sequence (or signature). This operation effectively spreads the bandwidth of the signal because the chip period T_{chip} is N times smaller than the symbol

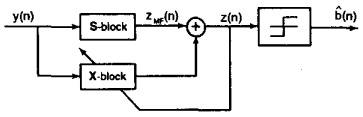


Figure 2: Block diagram of the adaptive MUD algorithm.

period T_{symb}. Chips are then modulated and sent into the channel. As all CDMA users share the same bandwidth, the received signal $y(n)$ is a linear combination of signals from different users (MAI) and reflected signals (multipath). Therefore, MUD can be employed at the receiver to recover the transmitted symbol $b(n)$ from $y(n)$.

One particular adaptive MUD algorithm is described in [7]. Consider the following canonical representation for the linear detector of a particular user:

$$\mathbf{c}(n) = \mathbf{s} + \mathbf{w}(n), \tag{1}$$

where $\mathbf{c}(n) = [c_0(n), c_1(n), \ldots, c_{N-1}(n)]^T$ is the detector coefficient vector, $\mathbf{s} = [s_0, s_1, \ldots, s_{N-1}]^T$ is the normalized spreading sequence vector of the desired user, and $\mathbf{w}(n) = [w_0(n), w_1(n), \ldots, w_{N-1}(n)]^T$ is a vector orthogonal to $\mathbf{s}$, i.e., $\mathbf{s}^T\mathbf{w}(n) = 0$. Two metrics of interests for the receiver are the mean-squared-error (MSE) and the mean-output-energy (MOE), which are defined below:

$$MSE = E[(N\,b(n) - \mathbf{y}(n)^T\mathbf{c}(n))^2], \tag{2}$$

and

$$MOE = E[z^2(n)] = E[(\mathbf{y}(n)^T\mathbf{c}(n))^2], \tag{3}$$

where $z(n)$ is the detector output.

It has been shown that [7] the MSE and MOE can be expressed in the canonical form (1) and that the corresponding $\mathbf{w}(n)$ vectors are identical. Specifically,

$$MSE(\mathbf{w}) = MOE(\mathbf{w}) - N^2, \tag{4}$$

where N is the spreading gain of the desired signal. This leads to a simple adaptive algorithm that determines the optimal value of $\mathbf{w}(n)$ that minimizes the MOE. From (3), we obtain the gradient of the MOE as

$$\nabla_{MOE}(\mathbf{w}) = 2\mathbf{y}(n)(\mathbf{s} + \mathbf{w}(n))\mathbf{y}(n), \tag{5}$$

whose component orthogonal to $\mathbf{s}$ is

$$2\mathbf{y}(n)^T(\mathbf{s} + \mathbf{w}(n))(\mathbf{y}(n) - (\mathbf{y}(n)^T\mathbf{s})\mathbf{s}) = 2z(n)(\mathbf{y}(n) - z_{MF}(n)\mathbf{s}). \tag{6}$$

Substituting (6) as an estimate of the gradient with respect to $\mathbf{w}$ in the steepest descent algorithm, we can obtain the following equations that describe the adaptive MUD algorithm [7]:

$$\begin{aligned} z_{MF}(n) &= \mathbf{y}(n)^T\mathbf{s}, & (7)\\ z(n) &= \mathbf{y}(n)^T(\mathbf{s}+\mathbf{w}(n)), & (8)\\ \mathbf{w}(n+1) &= \mathbf{w}(n)-\mu z(n)(\mathbf{y}(n)-z_{MF}(n)\mathbf{s}), & (9) \end{aligned}$$

where n is the symbol index, $z_{MF}(n)$ is the output of the signature filter, $z(n)$ is the input to the data slicer, and μ is the adaptation step size. In summary, the adaptive MUD algorithm in (7)–(9) can be implemented with a fixed signature filter **S**–block and an adaptive filter **W**–block as shown in Fig. 2. The complexity of the **S**–block is fixed and much smaller ($\approx 20\%$) compared to that of the **W**–block. Further the complexity of the **W**–block depends upon the channel conditions. Hence, a configurable approach that detects the channel condition and adjusts the complexity of the **W**–block would result in substantial energy savings.

2.2 Architectures

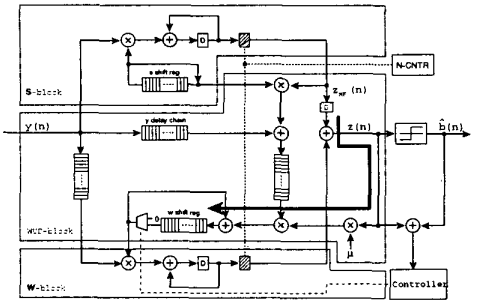
In this section, we introduce two architectures for the MUD-based algorithm. Fig. 3(a) shows a cutset-retimed [8] chip-serial structure that achieves low hardware complexity. (The multiplexers and the controllers are introduced to make the architecture reconfigurable as discussed in Section 3.) In this architecture, chips are processed sequentially as they are received. Since the signature sequence s_i is antipodal, the two multipliers in the **S**–block can be implemented as a two-input multiplexer that selects between the input and the 2's complement of the original input. The step size multiplier can be implemented with a shifter, assuming that μ is a power of 2.

The retimed chip-serial architecture has a critical path delay of,

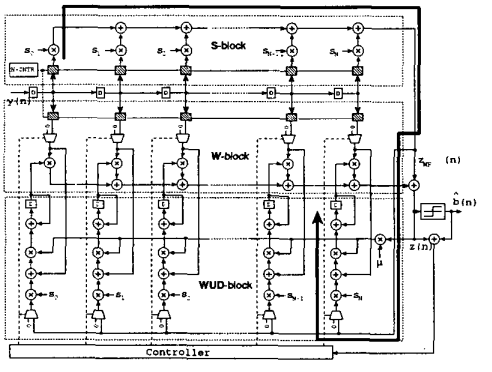
$$T_{chip\_serial} = 2T_a + 2T_m, \quad (10)$$

where T_a is a 7-bit two-operand adder delay, and T_m is a 7×7-bit two-operand multiplier delay. Using a 0.25 μm, 2.3 V CMOS technology standard cell library [9], one can synthesize a 32–bit carry-save adder (CSA) with about $27.5ns$ delay and a 32–bit Baugh-Wooley multiplier with about $51.8ns$ delay. From (10), the maximum chip rate achieved by the retimed chip-serial architecture in Fig. 3(b) is approximately 6.31 Mcps. This is sufficient for the basic rates of 0.9216 Mcps and 3.6864 Mcps described in CDMA–2000 specifications [1], but not for high-bandwidth mode which requires a chip rate of 14.7456 Mcps. The throughput of the chip-serial architecture can be improved further via high throughput techniques such as relaxed look-ahead [10] pipelining and parallel processing.

Note that the critical path in Fig. 3(a) is activated only when the last chip of each symbol is processed. At all other times, the sampling rate is



(a)



(b)

Figure 3: Reconfigurable architectures:(a) chip-serial and (b) chip-parallel architectures.

limited by the multiply-accumulate delay in the adaptive filter in the **W**–block. This is clearly not ideal since the occasionally activated critical path delay determines the overall throughput. We now present a chip-parallel architecture (Fig. 3(b)) that resolves this problem by processing all N chips of a symbol in parallel. The critical path in the chip-parallel architecture indicated in Fig. 3(b) consists of computations in all three blocks. Note that the adder chains can be replaced with a binary adder tree structure. In that case, the critical path delay for the chip-parallel architecture becomes

$$T_{chip\_parallel} = (\log_2 N + 2)T_a + T_m + T_{2's\_comp} \leq T_{symb}, \qquad (11)$$

where T_a is the adder delay, T_m is the multiplier delay, T_{mux} is the delay of two-input multiplexer, and $T_{2's\_comp}$ is the delay of 2's complement logic. As

the detector processes N chips at a time, the filter can take up to T_{symb} to update the **W**–block coefficients. That is,

$$\frac{1}{N}T_{chip\_parallel} \leq T_{chip}, \tag{12}$$

assuming that a spreading sequence of length N is used. This architecture can also be pipelined via the relaxed look-ahead technique [10] to obtain further speed-ups.

In summary, the chip-serial architecture has very low hardware complexity and is ideal when area is a major concern as in an FPGA implementation. The chip-parallel architecture trades area for higher throughput.

3 Reconfigurable MUD-based CDMA Architectures

In CDMA systems, critical system parameters, such as the number of active users and their distances from the receiver, are variable. The reconfigurable architecture in Fig. 3 can exploit this variability to save energy by powering down certain taps. Among the three blocks of the adaptive CDMA MUD receiver, the **W** and **WUD**–blocks are the most power-hungry elements and dissipate about 80% of the overall power. Hence the reason for introducing multiplexers into the **W** and **WUD**–blocks in Fig. 3(b). In this section, we employ DAT to derive energy optimal values for the control signals in Fig. 3(b). We also use an energy model for the multipliers that allows us to quantitatively evaluate the energy savings.

3.1 Reconfiguration Control Algorithm via DAT

It was shown in [6] that the tap metric necessary for deriving the energy-optimum configuration of a filter is $\frac{|w_k|^2}{\varepsilon_m(w_k)}$, where w_k is the k^{th} filter coefficient and $\varepsilon_m(w_k)$ is the energy consumed by a multiplier that has w_k as one of its operand. If a tap has a smaller metric, then it implies that the tap contributes less to the output but consumes more energy. Such taps should be the first to be disabled. Thus, the reconfiguration for the adaptive filter **W**–block can be summarized as follows.

Step 1: Activate all taps in the **W**–block and start the adaptation.
Step 2: Monitor $MSE = E[z(n) - sgn(z(n))]^2$.
Step 3: If $MSE < MSE_{min}$ then go to *Step* 4,
if $MSE > MSE_{max}$ then go to *Step* 1,
else keep current coefficients and go to *Step* 2.
Step 4: Disable the tap with the smallest non-zero tap metric: $\frac{|w_k|^2}{\varepsilon_m(w_k)}$.
Step 5: Go to *Step* 2.

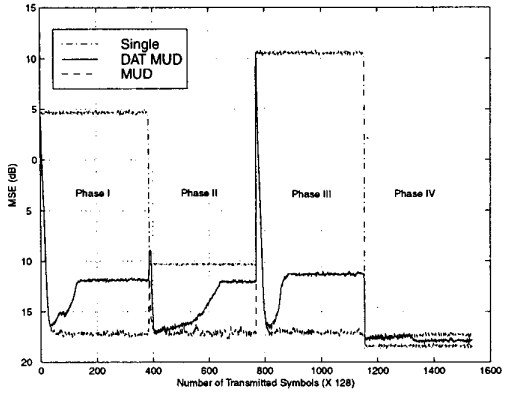


Figure 4: MSE for various detectors.

Note that we keep the MSE within the range $[MSE_{min}, MSE_{max}]$. This avoids the situation where oscillatory reconfigurations may occur due to small variations in the MSE around a threshold.

We employ the multiplier energy model proposed in [6]:

$$\varepsilon_m(w_k) = \varepsilon_{max} \frac{\eta N_1(w_k) + (1-\eta) N_2(w_k)}{B_w}, \tag{13}$$

where ε_{max} is the maximum power dissipation of the multiplier (when all bits of the multiplicand are 1s), B_w is the total number of bits of w_k, and η is a weight factor between 0 and 1, N_1 is the number of non-zero bits in coefficient w_k, and $N_2 \equiv B_w - B_{0,lsb}$, where B_w is the number of coefficient bits and $B_{0,lsb}$ is the number of '0' bits in the least-significant-bit (LSB) positions. It was found in [6] that this model with $\eta = 0.9$ is accurate with less than 9% estimation error using the gate-level simulation tool MED [11].

4 Simulation Results

In this section, we present the simulation results for the three types of CDMA receivers: the single-user detector, the adaptive MUD detector and the reconfigurable adaptive MUD detector. First, we describe the simulation setup.

4.1 Setup

A synchronous DS-CDMA system is employed in the simulation. Without loss of generality, all simulations are conducted using a baseband equivalent additive Gaussian noise channel with MAI. A signal-to-noise ratio (SNR) of 20 dB is used as in [7]. All user signatures are randomly chosen from

Phase	Single	MUD	DAT MUD
I	$-4.7dB$	$17.2dB$	$11.9dB$
II	$10.3dB$	$17.1dB$	$12.1dB$
III	$-10.5dB$	$17.0dB$	$11.3dB$
IV	$18.4dB$	$17.3dB$	$17.9dB$

Table 1: Stabilized SIR achieved by the three receivers.

truncated PN sequences of length 128, and a rectangular chip waveform is employed at a rate of 14.7456 Mcps. All simulations employ 7-bit precision multiply-accumulate, except the **WUD**–block which employs 20 bits.

The entire transmitted data sequence contains 196,608 symbols in binary phase-shift keying (BPSK) format. The simulations consist of four phases. In Phase I (symbol 1 to 49,152) there are 7 interferers whose signal amplitudes are 18 dB larger than that of the desired user at the receiver. Phase II (symbol 49,153 to 98,304) has 3 interferers present. Each interferencer's relative signal amplitude is 6 dB stronger. Phase III (symbol 98,305 to 147,456) simulates a severe near-far situation where all of the 8 interferers' relative signal amplitudes are 26 dB. The last phase (symbol 147,457 to 196,608) has only the desired users in the channel.

According to the IMT–2000 standard, the BER for data transmission should be less than 10^{-6}. This translates to a combined SNR and SIR at around 11 dB for BPSK. In this simulation, the SNR and the SIR combined are targeted better than 12 dB.

4.2 Results

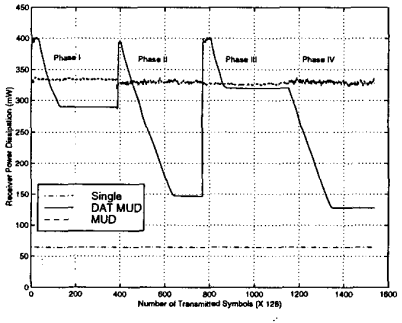


Figure 5: Power dissipation.

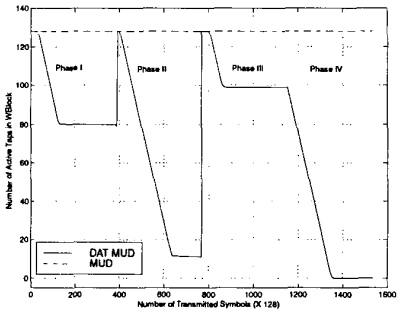


Figure 6: Active taps in the **W**–block.

The results of interest include the MSE and filter power dissipation. We include the power dissipation of the reconfigurable controller and the signature filter **S**–block in the energy analysis. As a rough estimate, we assume the power dissipations of the **S**–block and the controller are identical. In this

		MUD only	DAT MUD	Power Savings
Phase I	Power (mW)	326.5	289.7	11.3%
	Active Taps	128.0	80.1	—
Phase II	Power (mW)	318.8	146.6	54.0%
	Active Taps	128.0	11.4	—
Phase III	Power (mW)	323.0	319.5	1.1%
	Active Taps	128.0	98.8	—
Phase IV	Power (mW)	323.1	128.0	60.4%
	Active Taps	128.0	0.0	—

Table 2: Power dissipation of reconfigurable architecture.

simulation, there are 128, 1-bit multipliers in the **S**–block which amounts to approximately 20% of the total receiver power.

Fig. 4 and Table 1 show the MSE of the three CDMA receivers. The tolerance for the proposed receiver is set as between -12 dB and -15 dB across the entire simulation. In all four phases, the MUD-based adaptive receiver achieves an MSE of -17 dB once it converges. This figure is very close to the noise floor if the quantization error is taken into account. The output MSE of the DAT MUD receiver is maintained at around -12 dB. Finally, the MSE of the conventional decorrelator is very sensitive to the interference, changing from -17 dB to 10 dB.

Fig. 5 and Table 2 summarize the power dissipation of the **W**–block. The y-axis in Fig. 5 is the power dissipation of the receiver. In Phase I, the DAT MUD receiver converges after 17,280 symbols, and the average power savings in this phase is 7.12%. In Phase II, the DAT MUD receiver takes much longer time to converge because more taps can be disabled. The final energy savings is 54%. In Phase III, most of the taps need to be active to achieve the MSE requirement. However, the extra power dissipation due to the control circuit remains and results in only marginal power savings. It is worth mentioning that Phase IV is a nearly ideal situation. The DAT MUD receiver detects the low MAI condition and reconfigures itself into the single-user decorrelator. The adaptive MUD receiver, however, keeps all its taps active as in Phase III and dissipates much unnecessary power.

5 Conclusion

3G wireless standards provide an exciting backdrop and context for the design of reconfigurable receiver architectures due to their emphasis on flexibility (in terms of services), the need for sophisticated digital video and signal processing, and communications algorithms and low-power operation. In this paper, we applied dynamic algorithm transforms (DAT) for the design of a low-power, reconfigurable CDMA multiuser ASRIC architecture. Multipath is another key impairment in wireless channels and reconfigurable

architectures for multipath mitigating algorithms such as RAKE can also be developed.

6 Acknowledgement

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