# Low-Power Digital Filtering via Soft DSP *

Rajamohana Hegde and Naresh R. Shanbhag
ECE Department/Coordinated Science Laboratory
University of Illinois, Urbana, IL 61801.
**email**:[rhegde, shanbhag]@uivlsi.csl.uiuc.edu

## Abstract

In this paper, we propose low-power filtering algorithm developed via the *soft DSP* framework. Soft DSP refers to scaling the supply voltage of a DSP implementation beyond the voltage required to match its critical path delay to the throughput. This deliberate introduction of input-dependent errors leads to degradation in the algorithmic performance, which is then compensated for via algorithmic error-control schemes. The proposed error-control schemes, based on forward/backward linear prediction, provides improved performance over the ones proposed in the past by exploiting correlation in both leading and trailing samples with a latency penalty. It is shown that a) the proposed scheme provides $60-80\%$ reduction in energy dissipation over that achieved via conventional voltage scaling and b) for the same algorithmic performance, the overhead involved in the proposed algorithm is more than $50\%$ smaller than existing schemes for medium bandwidth filters.

## 1 Introduction

Energy-efficient VLSI circuit design for DSP applications is of great interest given the proliferation of mobile computing devices. For a given technology, reduction in energy dissipation has also been made possible due to energy-efficient design techniques at all possible levels of design hierarchy. Schemes at the lower levels of the design process [1] are usually application independent. At the algorithmic and architectural levels, features that are specific to a class of applications are exploited to develop application specific energy reduction techniques [2, 3]. Voltage scaling [3] is an effective means of achieving reduction in energy dissipation as a reduction in supply voltage $V_{dd}$ by a factor $K$, reduces the dominant capacitive component of energy dissipation by a factor $K^2$ [3]. However, the extent of voltage scaling [3] is limited by the critical path delay of the architecture and the throughput requirements of the application. If the supply is scaled beyond this limit (denoted as $V_{dd-crit}$), input dependent intermittent errors (soft errors) appear at the output.

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Recently, we have shown [4] that $V_{dd}$ can be scaled beyond $V_{dd-crit}$ for multimedia communication systems. It was shown that the errors introduced due to sub-critical voltage operation lead to degradation in algorithmic performance. The notion of algorithmic noise-tolerance (ANT) was proposed to restore the performance degradation due to sub-$V_{dd-crit}$ operation. The use of ANT in this context leads to substantial energy savings at no loss of throughput and was referred to as *soft DSP*. A backward prediction based error-control algorithm that exploits the correlation in the trailing samples was proposed for *frequency selective filters* to restore performance degradation due to soft errors. It was shown that up to $80\%$ energy savings are possible for narrowband filters. It was also shown that the proposed scheme is effective in restoring performance degradation due to random errors induced by deep submicron (DSM) noise [5].

In this paper, we propose an error-control algorithm that is based on forward-backward linear prediction and hence exploits correlation in both leading and trailing samples at the expense of increased latency.

The rest of this paper is organized as follows. In section 2, The notions of algorithmic noise-tolerance, soft DSP, and noise-tolerant DSP [4] are reviewed. In section 3, a low complexity forward/backward prediction-based algorithm is developed to detect the errors in the filter output. The effectiveness of the proposed filtering algorithm in a typical filtering scenario is evaluated in section 4. Finally, in section 5, conclusions and scope for future work on this topic are presented.

## 2 Algorithmic Noise-Tolerance (ANT)

The notion of algorithmic noise-tolerance, proposed in [4], refers to algorithmic error-control to restore performance degradation due to errors in the system output. As the algorithmic performance of DSP/communication systems is specified in terms of average metrics such as bit-error-rate ($BER$) and signal-to-noise ratio ($SNR$), errors in system output lead to degradation in $BER$ or $SNR$. If the error frequency is high enough, it can lead to substantial degradation in $BER$ or $SNR$ making them fall below the minimum desired level. In [4], two scenarios that can lead to degradation in $BER/SNR$ in a DSP system are considered. For both, we employ ANT to restore the performance degradation. In the first scenario, referred to as *soft DSP*, errors are deliberately introduced by scaling supply voltage without sacrificing throughput to achieve energy savings. In the second scenario, errors are due to spurious voltage deviations introduced at the circuit level due to DSM noise.

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### 2.1 Soft DSP

A typical DSP system is designed in such a way that the critical path delay [6] $T_{cp}$ (defined as the *worst case delay over all possible input patterns*), should be less than or equal to the sample period $T_s$, i.e., $T_{cp} \leq T_s$. Hence, given $T_s$, the DSP system is designed such that, at the rated supply voltage $V_{dd}$, the *delay condition*, $T_{cp} \leq T_s$, is satisfied. Note that violating the delay condition by reducing $V_{dd}$ beyond $V_{dd-crit}$ [4], i.e., setting

$$V_{dd} = K_v V_{dd-crit}, \tag{1}$$

where $0 < K_v < 1$, leads to erroneous output when the critical paths are excited. In [4], it was proposed to operate the DSP architecture at voltages lower than $V_{dd-crit}$ in order to achieve higher energy savings. Such operation leads to errors in the system output when the critical paths and other longer paths are excited, which are corrected using ANT techniques. This approach is referred to as *soft DSP* and typically gives upto 80% additional energy savings after current voltage scaling approaches have been applied.

### 2.2 DSM Noise

Errors in system output can also result from the phenomenon of DSM noise that is inherent in current and future technologies. DSM noise refers to unwanted voltage deviations due to DSM phenomenon such as *ground bounce*, *charge sharing*, *charge leakage* etc. [5]. When the voltage deviations at the circuit level are substantial in magnitude and duration, they lead to logical errors which can also be corrected via ANT techniques [4].

### 2.3 Impact of errors on algorithmic performance

In the absence of errors, the performance of a DSP transfer function $H(z)$ is measured in terms of the output $SNR$ given by

$$SNR = 10\log(\sigma_s^2/\sigma_w^2), \tag{2}$$

where $\sigma_s^2$ is the signal power and $\sigma_w^2$ is the signal noise power. In presence of errors (due to soft DSP or DSM noise), we have,

$$SNR = 10\log(\sigma_s/(\sigma_{w+c}^2)), \tag{3}$$

where $\sigma_{w+c}^2$ is the total noise power. In this scenario, ANT is to achieve a value of $\sigma_{w+c}^2$ that is as close to $\sigma_w^2$ as possible.

It should be noted that the proposed approach differs significantly from algorithm based fault tolerance (ABFT) [7, 8, 9]. In ABFT for DSP systems, the objective is to maintain or restore performance in the event of a permanent fault in the hardware. In these cases, the general approach is to detect the change in system state due to the fault and the carry out fault recovery. In our case, the 'faults' are intermittant and hence warrant immediate detection and correction. Though, the fault detection/correction techniques in [7, 9] can handle intermittant errors, they do not exploit the statistical properties of the output and involve a larger overhead.

## 3 Noise-Tolerant Filtering Algorithm

In this section, we present an algorithmic error-control scheme for digital-filtering in order to reduce the impact of errors on the algorithmic performance. The proposed algorithm is based on forward-backward linear prediction (FBP) [10].

The filter output, when the filter is error-free, is denoted by $y(n)$ and is given by,

$$y(n) = \sum_{k=0}^{N-1} h(k)x(n-k), \tag{4}$$

where $h(k)$ denotes the filter impulse response, $x(n)$ is the filter input and $N$ is the number of taps in the filter. The difference in consecutive samples of the filter output is given by,

$$y_d(n) = y(n) - y(n-1). \tag{5}$$

Let $\hat{y}(n)$ denote the filter output when the filter is operating under reduced voltage, with

$$\hat{y}(n) = y(n) + y_{err}(n), \tag{6}$$

where $y_{err}(n)$ denotes the error in the filter output due to soft errors. Note that $y_{err}(n)$ is non-zero only when the input pattern is such that longer paths in the filter implementation are excited. Let $y_p(n)$ denote the output of an $2N_p$-tap predictor when the filter is noiseless, i.e.,

$$y_p(n) = \sum_{k=-N_p, k\neq 0}^{N_p} h_p(k)y(n-k), \tag{7}$$

where $h_p(k)$ denotes the *optimum predictor coefficients* [10] that minimize the mean squared value (MSE) $< e_p^2(n) >$ of the prediction error $e_p(n)$, given by,

$$e_p(n) = y(n) - y_p(n). \tag{8}$$

The minimum mean square error (MMSE) depends on the autocorrelation function of $y(n)$ and the order of the predictor. Let $\hat{y}(n)$, $\hat{y_p}(n)$, and $\hat{e_p}(n)$ denote the filter output, the predictor output, and the prediction error, respectively, in presence of soft errors. From (6) and (8), we get

$$\hat{e_p}(n) = y_{err}(n) + e_p(n). \tag{9}$$

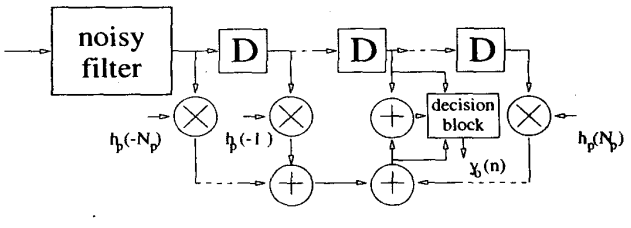


Figure 1: The forward/backward prediction-based ANT scheme for LPF.

Assuming that no more errors occur in the next $N_p$ output samples, we can show that,

$$\hat{e_p}(n+m) = -h_p(m)y_{err}(n) + e_p(n+m), \qquad (10)$$

for $m = -N_p, \cdots, -1, 1, \cdots, N_p$. Equations (9) and (10) can now be expressed in vector form as

$$\hat{\mathbf{e}}_p(n) = y_{err}(n)\mathbf{h} + \mathbf{e}_p(n) \qquad (11)$$

where $\hat{\mathbf{e}}_p(n) = [\hat{e_p}(n)\ \ \hat{e_p}(n+1)\ \ \cdots\ \ \hat{e_p}(n+N_p)]^T$,
$\mathbf{h} = [1\ \ -h_p(1)\ \ -h_p(2)\ \ \cdots\ \ -h_p(N_p)]^T$,
and $\mathbf{e}_p(n) = [e_p(n)\ \ e_p(n+1)\ \ \cdots\ \ e_p(n+N_p)]^T$. It can be shown that if $|\mathbf{h}^T\mathbf{e}_p(n)| \leq E_{th}$, where $E_{th}$ is positive, then

$$|\mathbf{h}^T\hat{\mathbf{e}}_p(n)| \ \geq\ |y_{err}(n)|\|\mathbf{h}\|^2 - E_{th}. \qquad (12)$$

It can be seen from (12) that if $|y_{err}(n)| > \frac{2E_{th}}{\|\mathbf{h}\|^2}$, then $|\mathbf{h}^T\hat{\mathbf{e}}_p(n)| > E_{th}$ and hence the error is detected.

### 3.1 Error-Control Algorithm

The following algorithm derived from (12) is employed for error control:

- Let $\sigma^2_{e_p}$ be the variance of the prediction error with noiseless digital filter.
- Error detection:
  If $|\mathbf{h}^T\hat{\mathbf{e}}_p(n)| > \sigma_{e_p}$, then an error is declared.
- Error correction:
  If an error is declared, then
  $$y_o(n) = y_p(n),$$
  else
  $$y_o(n) = \hat{y}(n).$$

Hence, if an error is detected, the predictor output based on the past correct samples is declared as the system output. The effectiveness of the error detection and correction scheme described above depends on the following assumptions:

1. The magnitude of $y_{err}(n)$ is relatively large. Errors with higher magnitudes lead to a higher value of $|\mathbf{h}^T\hat{\mathbf{e}}_p(n)|$ and the error is easily detected.
2. The probability that $\hat{y}(n) \neq y(n)$ is small enough such that the frequency of the errors in the filter output is less that $1/2N_p$. The performance of the above scheme deteriorates when multiple errors occur at the filter output in the span of $2N_p$ samples.

The errors due to soft DSP occur in the MSBs and hence are of large magnitude. This validates assumption 1. Assumption 2, limits the factor by which voltage can be reduced and suggests the type of arithmetic unit architecture that can be employed (delay imbalanced architectures are better).

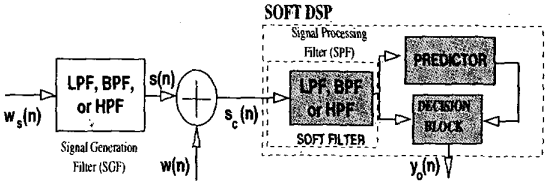


Figure 2: Simulation setup to evaluate the proposed scheme.

## 4 Experimental Results

The setup used to measure the performance of the proposed scheme in which the filtering algorithm is employed (shown in Figure 2) is similar to the one employed in [4]. A lowpass, bandpass or a highpass filter (LPF, BPF or HPF), denoted as the signal generation filter (SGF), is used to generate a bandlimited signal $s(n)$ which is then corrupted by wideband noise $w(n)$. The $SNR$ of $s_c(n)$ is given by

$$SNR_{in} = 10\log_{10}\left(\frac{\sigma_s^2}{\sigma_w^2}\right), \qquad (13)$$

where $\sigma_s^2$ is the variance of $s(n)$ and $\sigma_w^2$ is the variance of $w(n)$. As $s(n)$ is bandlimited, the $SNR$ can be improved by passing $s_c(n)$ though a frequency selective filter with bandwidth $\omega_b$. This filter is denoted as the signal processing filter (SPF) in Figure 2. The $SNR$ at the filter output, denoted by $SNR_o$, is given by,

$$SNR_o = 10\log_{10}\left(\frac{\sigma_s^2}{\sigma_n^2}\right), \qquad (14)$$

where $\sigma_n^2$ is the power of $w(n)$ in the same band as $s(n)$. We employ the proposed soft DSP implementation of the filtering algorithm to perform frequency selective filtering on $s_c(n)$ as shown in Figure 2. Note that this setup simulates several practical scenarios for signal processing where the task is to extract a bandlimited signal embedded in wideband noise.

### 4.1 Performance Measures

The $SNR$ at the output of the filter in presence of errors is given by,

$$\hat{SNR}_o = 10\log_{10}\left(\frac{\sigma_s^2}{\sigma_n^2 + \sigma_c^2}\right), \qquad (15)$$

where $\sigma_s^2$ is the variance of the signal component (due to $s(n)$), $\sigma_n^2$ is the variance of the noise component (due to $w(n)$), and $\sigma_c^2$ is the variance of error in the output due soft computations or DSM noise (i.e., $< y_{err}(n)^2 >$). In order to estimate the energy savings obtained via voltage reduction as proposed, the energy dissipation values are obtained by using MED [11], a gate level energy estimator. The reduction in energy dissipation is characterized by *energy savings* ($ES$), defined as

$$ES = \frac{E_{original} - E_{proposed}}{E_{original}} \times 100\%, \qquad (16)$$

where $E_{original}$ is the energy dissipation with conventional voltage scaling (i.e., with $V_{dd} = V_{dd-crit}$), and $E_{proposed}$ is the energy dissipation with the proposed scheme.

### 4.2 Energy-Performance Characteristics

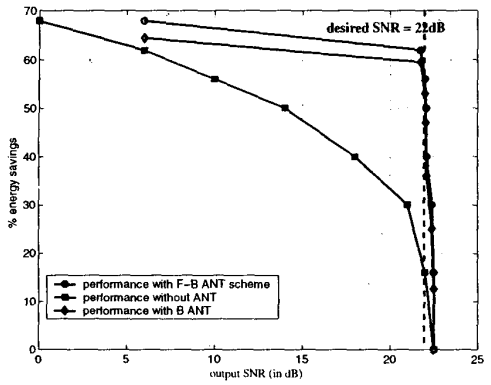


Figure 3: Performance vs. Energy Savings with filter bandwidth $\omega_b = 0.5\pi$ for the forward-backward prediction based ANT scheme with $N_p = 1$ ($SNR_{in} = 18.5dB$).

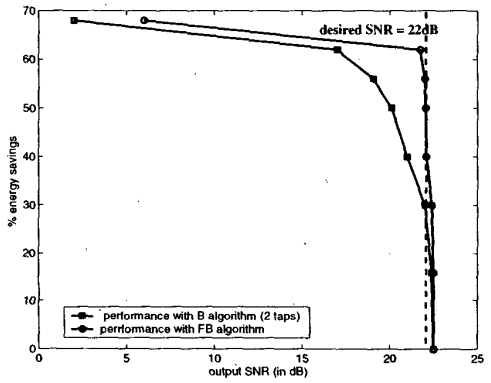


Figure 4: Performance vs. Energy Savings with filter bandwidth $\omega_b = 0.5\pi$ for the forward-backward prediction based ANT scheme with $N_p = 1$ ($SNR_{in} = 18.5dB$).

The plot of $SNR_o$ vs. energy savings of the proposed scheme is shown in Figure 3. In the absence of noise-tolerance, note that there is a rapid degradation in performance with reduction in energy dissipation. As the errors occur in the MSBs, the degradation in performance is quite steep. The performance degradation is however arrested by the proposed noise-tolerant algorithm over a significant range. Note that about 64% reduction in energy dissipation is possible via the proposed FBP algorithm with $N_p = 1$, i.e., the error control overhead is 2-taps. Similar performance is obtained for the backward prediction (BP) algorithm [4] with an overhead of 4-taps for error control. Thus the FBP scheme offers the same performance with 50% smaller overhead.

The performance of the FBP algorithm with that of the BP algorithm for the same error control overhead is shown in Figure 4. Note that the BP algorithm provides only upto 30% reduction in energy dissipation without significant degradation in performance as compared to the FBP algorithm that provides upto 60% reduction in energy dissipation with less than $0.5dB$ loss in performance.

## 5 Conclusions & Future Work

In this paper, we have proposed a generalized error-control algorithm to achieve significant reduction in energy dissipation with a marginal trade-off in performance via soft DSP. It was shown that the proposed algorithm provides the same performance with 50% lesser error-control overhead as compared to the existing scheme. Future work on this topic will involve measuring the effectiveness of the proposed algorithm for wireless applications and an integrated circuit implementation of a soft DSP system.

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