Reliable Low-Power Design in the Presence of Deep Submicron Noise

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ABSTRACT

Scaling of feature sizes in semiconductor technology has been responsible for increasingly higher computational capacity of silicon. This has been the driver for the revolution in communications and computing. However, questions regarding the limits of scaling (and hence Moore's Law) have arisen in recent years due to the emergence of deep submicron noise. The tutorial describes noise in deep submicron CMOS and their impact on digital as well as analog circuits. In particular, noise-tolerance is proposed as an effective means for achieving energy and performance efficiency in the presence of DSM noise.

1. INTRODUCTION

Since, late eighties, enormous advances have been made in developing tools and techniques that enable the design of energy-efficient ICs. These include techniques at various levels of the design abstraction. Relentless scaling of feature sizes in semiconductor technology [14] following Moore's Law has rendered the ability to significantly improve performance and lower power of integrated circuits at an affordable cost. This has been the driver for the revolution in the computing and communication infrastructure. However, with feature sizes being reduced towards $0.1 - 0.05\mu m$ generations, questions have arisen regarding the ability to achieve favorable cost vs. performance/power trade-offs in future CMOS technologies. The emergence of deep submicron (DSM) noise [28] in the form of cross-talk, leakage, supply noise, as well as process variations is making it increasingly hard to achieve the desired level of noise-immunity while maintaining the historic improvement trends in performance and energy-efficiency.

Indeed, the scenario facing the semiconductor industry and present design approaches are reminiscent of the communication design techniques of the pre-Shannon era that ended with the publication of [27] in 1948. Repetitive transmission with large signal powers was a common means of achieving reliable communication of information. A key impact of [27], relevant to the discussion here, was to enable modern day communication systems to achieve a high degree of reliability with signal levels that are comparable to noise in many cases thereby achieving the dual goals of reliability and energy-efficiency. Interestingly, Winograd in 1963 provided the following motivation for his work in [32]: "As computers become larger, faster, and more complex, it seems unlikely, despite recent developments in microelectronics, that component reliability will become sufficiently good to permit the immediate synthesis of complex computing organs from components that for all practical purposes may be considered infallible."

Winograd's prediction was much ahead of its time. Semiconductor process technology, the design tools, techniques and methodologies have made integrated circuits a reliable medium for implementation of information processors until now. DSM noise along with increasing complexity of systems-on-a-chip (SOC) solutions, and increasingly stringent requirements on speed and power have made the design of *reliable and efficient (in terms of energy and/or performance) SOC* a problem of great significance: one that has a direct bearing on the future of Moore's Law. Solving this problem requires a new design paradigm that addresses the reliability of the system as opposed to that of the component (devices, and circuits) even though the cause (DSM noise) of unreliable system behavior is in the component. Such a paradigm will be inherently multidisciplinary as it may bring in information-theory for computing bounds on energy-efficiency and reliability, error-control coding and communication theory for designing efficient computing systems that approach these bounds, a blurring of the boundaries between analog and digital circuit design techniques, and CAD tools and techniques that are noise aware. The low-power design community, due to its diverse constituents, is well-positioned to address the problem of *reliable low-power design*. The fault-tolerant and low-power design communities have independently addressed the reliability and the energy-efficiency issues, respectively. However, joint optimization of these two metrics is essential to ensure that benefits of large scale integration can be continually reaped.

In addition to discussing trends in DSM noise sources, and their influence on high-performance and low-power design

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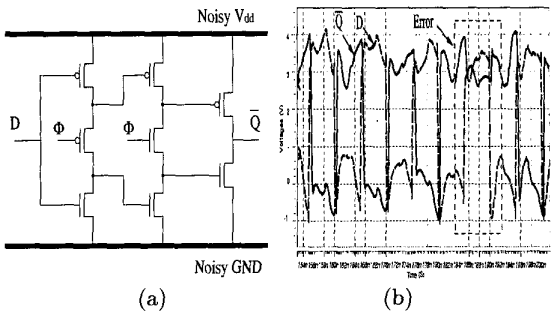

Figure 1: Impact of power supply bounce on a dynamic D-latch: (a) transistor schematic, and (b) input and output waveform.

techniques, this tutorial paper will present concrete approaches for computing bounds on energy-efficiency in the presence of DSM noise, and new circuit as well as algorithmic techniques for exploring the energy-efficiency vs. reliability curve. Key concepts will be emphasized through theoretical as well as measured results obtained in the VLSI Information Processing Systems (ViPS) Research Group at University of Illinois at Urbana-Champaign, the Circuits Research Laboratory (CRL) at Intel Corp., Portland, Oregon and Bell Laboratories at Lucent Technologies, Murray Hill, New Jersey.

The paper is organized as follows. In section 2, we describe DSM noise sources and their trends with scaling, noise metrics and their measurement. In section 3, we desribe an information-theoretic framework for computing achievable bounds on energy-efficiency in the presence of DSM noise. A key conclusion of this section will be that noise-tolerance is necessary to approach the energy-efficiency bounds. Circuit as well as algorithmic techniques for noise-tolerance will be illustrated in section 4. The role of noise in analog circuits will be discussed in section 5.

2. NOISE IN DEEP SUBMICRON CMOS

2.1 DSM Noise Mechanisms

Noise in DSM circuits is defined as any disturbance that drives node voltages and/or currents away from a nominal value causing permanent as well as intermittent logic failure. Increased delay as well as accidental discharge/charge of dynamic nodes are common mechanisms for such failures. Figure 1 illustrates one such error. When $D = V_{dd}$, if an inductive kick raises the supply node above $V_{dd} + |V_{tp}|$ then the topmost PMOS at the input in Fig. 1(a) will turn on resulting in a logic error as shown in Fig. 1(b).

Noise sources that have substantial impact on the performance of digital circuits include ground bounce, IR drop, crosstalk, charge sharing, process variations, charge leakage, alpha particles, electro-magnetic radiation, etc., [17, 28]. These problems worsen as technology scales further and hence are referred to as deep submicron (DSM) noise.

For example, a key feature of the scaling trend is the increase in I_{off} (by 3X) with every successive technology generation. Fig. 2 shows the impact of this trend on the dynamic node of a fully loaded (fanout = 9) 8-wide NOR domino circuit with

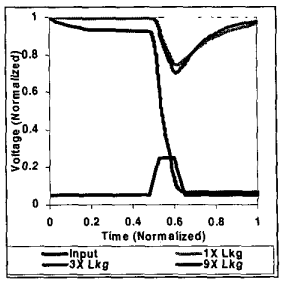

Figure 2: Noise scaling trend at the dynamic node of a domino circuit.

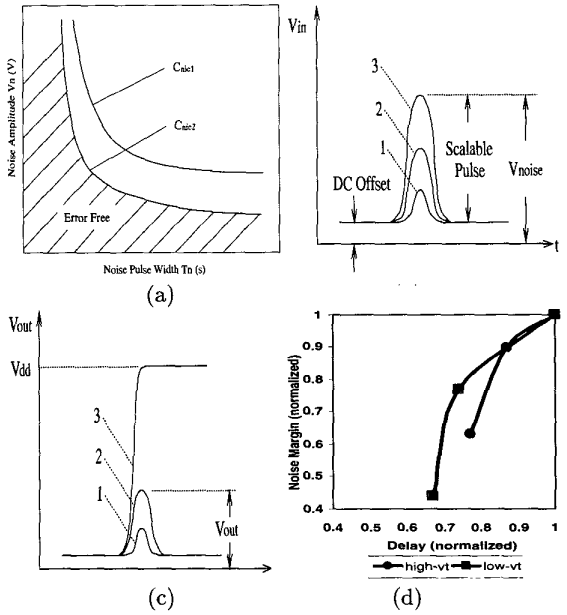

Figure 3: Dynamic noise-immunity metrics: (a) noise-immunity curves (NICs), (b), input and (c) output waveforms employed in defining unity noise gain (UNG) and (d) the "noise wall" in the delay vs. UNG plot.

a PMOS keeper. The data shows that this circuit technique is unsustainable when the leakage is set at 9X (e.g $0.1\mu m$) of the base technology (e.g $0.18\mu m$).

2.2 Noise-Immunity Metrics

A commonly employed definition of noise-immunity [15] are the static noise margins $NM_L = V_{IL} - V_{OL}$ and $NM_H = V_{OH} - V_{IH}$, where V_{OL}, and V_{OH} are the minimum and maximum output voltage levels, respectively, and V_{IL} and V_{IH} are the low and high input voltage levels at which the DC voltage transfer curve of a gate has a gain of -1. Static noise margins are conservative noise-immunity metrics because they do not account for the fact that digital gates are inherently low-pass in nature and thus can filter out noise pulses with amplitude V_n that are greater than NM_L or NM_H provided the noise pulse width T_n is sufficiently narrow, i.e., the noise pulse has predominantly high frequency components.

Hence, dynamic noise-immunity metrics such as the noise-immunity curve (NIC) [16] in Fig. 3(a) are required. The NIC of a digital gate is a locus of points (T_n, V_n) for which the gate just makes a logic error (defined as the event when the output crosses a predefined voltage threshold). The NIC of a digital gate provides the following information:

1. all points on and above the NIC represents error causing noise pulses while all noise pulses below the NIC do not cause any errors. Hence, higher the NIC of a gate, the less susceptible is the gate to noise.
2. the vertical asymptote of the curve provides the *best-case* delay of the circuit, in general. For single-input gates such as the inverter, this asymptote provides also the *worst-case* delay (or just the delay) of the circuit. Thus, noise-immunity and throughput are intimately (and inversely) related.

The *average noise threshold energy* ($ANTE$) [31] is a convenient measure derived from a NIC that can be employed to compare the various circuit techniques and is defined as

$$ANTE \triangleq E\left({V_n}^2 T_n\right), \tag{1}$$

where $E(\ )$ denotes the average. As circuits are designed for a specific worst-case delay, the average in (1) is taken for noise pulse widths ranging from the best case to the worst case delay of the circuit. Usually noise-immunity enhancing techniques incur power/performance penalty at the circuit level. Thus, normalizing $ANTE$ ($NANTE$) with the energy of the gate gives another metric that compares the effectiveness of different noise-tolerance techniques.

Another measure of noise-immunity, referred to as the *unity noise gain* (UNG), can be obtained by injecting identical noise pulses into all inputs and measuring the resulting voltage output waveform V_{out} as shown in Fig. 3(b)-(c). The noise stimulus consists of a DC offset V_{DC} (to account for possible IR drops) and a scalable pulse V_{pulse}, i.e.,

$$V_{noise} = V_{DC} + V_{pulse}, \tag{2}$$

where the shape of V_{pulse} closely mimics the real noise pulses. UNG is defined as the amplitude of input noise V_{noise} that causes an equal-amplitude output noise at V_{out}, i.e.,

$$UNG = \{V_{noise} : V_{noise} = V_{out}\}. \tag{3}$$

Note that UNG is dependent on the noise pulse width T_{noise}. An interesting interpretation of UNG can be obtained in the case when V_{pulse} is small enough for small-signal analysis to hold. In that case, UNG equals the input amplitude for which the small-signal gain (with V_{DC} being the bias point) at frequency $1/T_{noise}$ is unity. Thus, UNG can be viewed as the AC version of the static noise margins NM_L and NM_H (Note: UNG_L and UNG_H can be similarly defined for static circuits).

The trade-off between performance and noise-immunity is made explicit in Fig. 3(d), in which a unity slope line would represent a desirable scaling trend where the reduction in noise margin tracks delay (and V_{dd}) scaling. However, both high and low V_t technologies will fail to track this trend. Recent joint work between UIUC ViPS Group and Intel CRL Lab has shown that for wide OR gates, a $11-14\%$ improvement in speed results in a $40-50\%$ degradation in UNG metric for a $0.1\mu m$ technology.

Given the well-known relationship between delay and energy, it is clear that designers need to explicitly consider the trade-off between power, performance and noise-immunity in a unified manner. Noise analysis tools and techniques such as [1] that inform the designer of the noise characteristics will be much needed. The noise wall in Fig. 3(d), reminiscent of the power wall being faced by designers of high performance systems, can be breached only by a new design paradigm that is aware of bounds on achievable energy-efficiency and strives to achieve system reliability (as opposed to component reliability) through a combination of circuit, algorithmic and technology-based solutions. In the next section, we present an information-theoretic framework for computing achievable bounds on energy-efficiency in the presence of DSM noise.

3. BOUNDS ON ENERGY-EFFICIENCY

Being able to compute achievable bounds on energy-efficiency under the constraint of reliable system operation provides a direct answer to question of how long can Moore's Law continue and motivates the designer to explore techniques for closing the gap between efficiency of present day systems and the bounds. Lower bounds on energy dissipation have been addressed by researchers in the integrated circuits area [20, 29]. These bounds are derived under the constraint of component reliability. Information theoretic research [9, 22, 32] has derived bounds on component reliability for achieving an arbitrary level of system reliability. The information-theoretic approach satisfies the need to focus on system reliability as opposed to component reliability. However, what is lacking in the latter approach is: (1) the missing link to physical properties of semiconductor technology that permits the derivation of bounds on energy-efficiency and (2) the inherent assumption of unbounded complexity for optimal systems. In this section, we present our recent work [10, 25, 26] that addresses the first issue while the second issue is addressed in section 4.

3.1 Information-Theoretic Framework

Information theory takes a probabilistic model for signals and noise. For example, an information bearing signal source is defined as one that generates symbols Y from the set $S_Y = Y_0, Y_1, \ldots Y_{L-1}$ with a probability $p_i \stackrel{\text{def}}{=} Pr(Y = Y_i)$ for $i = 0, \ldots, L-1$. The information content of such a signal is given by its *entropy* [27] $H(Y)$ as follows

$$H(Y) = -\sum_{i=0}^{L-1} p_i log_2(p_i), \tag{4}$$

A useful relation quantity is the *entropy function* $h(p)$ defined as follows:

$$h(p) = -plog_2(p) - (1-p)log_2(1-p), \tag{5}$$

where $0 \leq p \leq 1$. The *inverse entropy function* $h^{-1}(q)$ where $0 \leq h^{-1}(q) \leq 0.5$ can similarly be defined.

In [26], we have shown that any system function with input X and output Y has a minimum *information transfer rate*

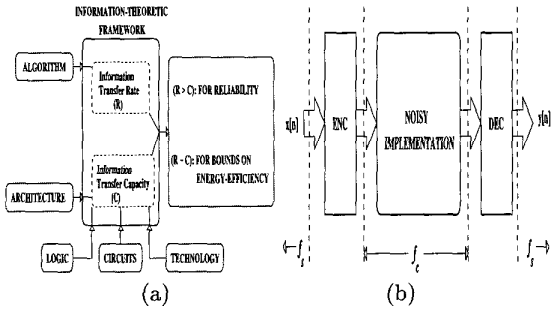

Figure 4: The information-theoretic framework for DSM ICs: (a) framework components, and (b) implementation.

requirement of R bits/s given by

$$R = f_s H(Y), \tag{6}$$

where $H(Y)$ is the output entropy and f_s is the rate at which X is being generated. The information transfer rate R is *implementation-independent.*

The channel capacity per use C_u [10] is obtained by maximizing the mutual information $I(X;Y) = H(Y) - H(Y|X)$ over all possible channel input distributions [27],

$$C_u = \max_{\forall p(x)} [H(Y) - H(Y|X)]. \tag{7}$$

Multiplying C_u with the rate at which the channel is used f_c, we obtain

$$C = C_u f_c, \tag{8}$$

where C is the *information transfer capacity* of the implementation. For DSM integrated circuits, f_c, C_u and hence C are a complex function of the technology, circuit style and architecture. In particular, C increases with V_{dd} (because f_c and noise margins increase) and decreases with DSM noise.

If the constraint $C > R$ is satisfied, then the joint source-channel coding theorem [27] guarantees that an encoder-decoder combination (see Fig. 4(b)) exists that guarantees a vanishingly small probability of error at the decoder output. We refer to the constraint $C > R$ as the *reliability constraint.* Thus, by making C approach R, we can obtain circuit parameters values that that minimize energy of the noisy implementation (not including the encoder-decoder) in Fig. 4(b) while maintaining reliability. For these bounds to be approachable in practice, one needs a low-complexity (low compared to the noisy circuit) encoder-decoder. In section 4, we show that a combination of circuit as well as algorithmic noise-tolerance techniques are excellent candidates to employ for approaching the bounds.

3.2 Computing Lower Bounds

Based upon the discussion so far, the following optimization problem can be formulated for a single output gate,

$$minimize \quad E_b = \frac{P_{tot}}{R} = \frac{P_{cap} + P_{stat} + P_{sc}}{R} \tag{9}$$

subject to:

$$[h(t) - h(\epsilon)] f_c = R \tag{10}$$

$$f_c = \frac{k_m (V_{dd} - V_t)^2}{V_{dd} C_L} \tag{11}$$

where $P_{cap} = 0.5 t C_L V_{dd}^2 f_c$, P_{stat} and P_{sc} are the capacitive, static and short-circuit components of power dissipation, t is the transition activity, E_b is the energy/bit of information being transferred, k_m is the device transconductance and C_L is the load capacitance. The term ϵ is the probability that a logic error occurs and is a function of the standard deviation σ_N of the noise amplitude V_n thereby embodying the impact of DSM noise.

There is an intricate relationship between R, σ_N, t, C_L, V_{dd}, V_t, f_c, k_m and ϵ in (9), (10), and (11). By solving the above problem in its most general form in [13], we have shown that in a scenario where P_{cap} dominates, **the supply voltage for minimum energy $V_{dd,opt}$ is greater than the minimum supply voltage ($V_{dd,min}$) for reliable operation**, i.e., minimum energy is consumed not when $C = R$ but when C is close to R. Further, we have shown that for off-chip signaling, the **lower bounds on energy-efficiency are 24X below** the energy-efficiency achieved by present day systems. For various special cases, we describe the following interesting results.

The lower bound on f_c for reliable operation of a symmetric, single output, noisy logic gate can be obtained from (10) as

$$f_{c,min} = \frac{R}{1 - h(\epsilon)}. \tag{12}$$

The above equation indicates that as DSM noise (i.e., ϵ) increases, the minimum frequency at which the circuit needs to be clocked also increases.

The minimum value of V_{dd} for reliable operation of a symmetric, single output, noisy logic gate, denoted by $V_{dd,min}$, can be shown from (10-11) to satisfy the following quadratic,

$$\frac{(V_{dd,min} - V_t)^2}{V_{dd,min}} = \frac{R C_L}{k_m [1 - h(\epsilon)]}, \tag{13}$$

which clearly shows that $V_{dd,min}$ increases with DSM noise.

The lower bound on transition activity at the output of a symmetric, single output, noisy logic gate employing transition signaling can be obtained as

$$t \geq h^{-1}\left[\frac{R}{f_c} + h(\epsilon)\right]. \tag{14}$$

Note, if $f_c = f_{c,min}$, $V_{dd} = V_{dd,min}$ then $t = 0.5$ in (14). However, this condition may not result in minimum energy dissipation. An increase in V_{dd} leads to an increase in f_c and hence a decrease in t. The decrease in t can offset the increase in V_{dd} and f_c resulting in a net reduction in dynamic energy consumption. Hence, the rationale for the non-intuitive result $V_{dd,opt} > V_{dd,min}$ referred to earlier.

In the absence of noise, i.e. $\epsilon = 0$, substituting $R = \mathcal{H} f_s$ bits/s and $f_c = R_b f_s$ (R_b is the number of code bits assigned per symbol) into (14), we obtain the lower bound on t for the noiseless case [25].

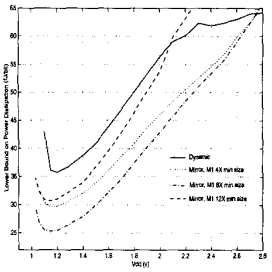

Figure 5: Lower bounds on energy dissipation for the mirror technique.

From the discussion so far it is clear that the lower bounds improve (i.e., reduce) as the error frequency ϵ reduces. One way to reduce ϵ is to employ noise-tolerance circuit techniques [2, 4, 6, 31]. These techniques add more circuit elements to the original domino gate and hence would incur an energy penalty at the same supply voltage. However, a good noise-tolerant circuit technique can achieve equal or better noise-immunity at a lower supply voltage than the corresponding domino circuit. Thus, noise-tolerance techniques can improve the lower bounds on energy, provided the reduction in ϵ offsets the energy penalty due to noise-tolerance. Recently, this conjecture was verified (see Fig. 5) for a 3-input OR gate transferring information at a rate $R = 150Mbits/sec$ in 0.35μm CMOS [30]. This work indicates that the lower bound on energy consumption of the noise-tolerant circuit is 31% below that of the conventional domino circuit. Further, this lower bound is achieved when the $ANTE$ noise-immunity metric of the mirror technique is $1.64X$ more than that of the domino circuit technique. Further improvements in noise-immunity do not reduce the lower bounds because the energy penalty starts to dominate.

The results in [30] were obtained for a noise voltage with standard deviation of $400mV$, which Fig. 5 indicates is comparable to $V_{dd,opt} = 1.1V$. Similar results in [13, 26] point clearly to *noise-tolerance* as a practical means of approaching the bounds on energy dissipation as described in the next section.

4. NOISE-TOLERANT VLSI

In this section, we describe noise-tolerance techniques for combating DSM noise while maintaining energy-efficiency. Motivation for noise-tolerance is derived from the information-theoretic results of section 3 which indicate that signal and noise powers need to be comparable in order to approach the bounds on energy-efficiency. This means that from an energy-efficiency perspective it is better to make errors and correct them rather than expending energy to reduce noise. The use of error-correcting codes for noisy gates [7, 21] and arithmetic units [23, 24] have been considered before but not in conjunction with energy-efficiency. Indeed, we will see later that in order to satisfy the low-complexity constraint on the encoder-decoder combination in Fig. 4(b), noise-tolerance techniques at higher levels of the design abstraction such as the architectural and algorithmic levels are required. This is so that the energy cost of error control can be amortized over complex blocks.

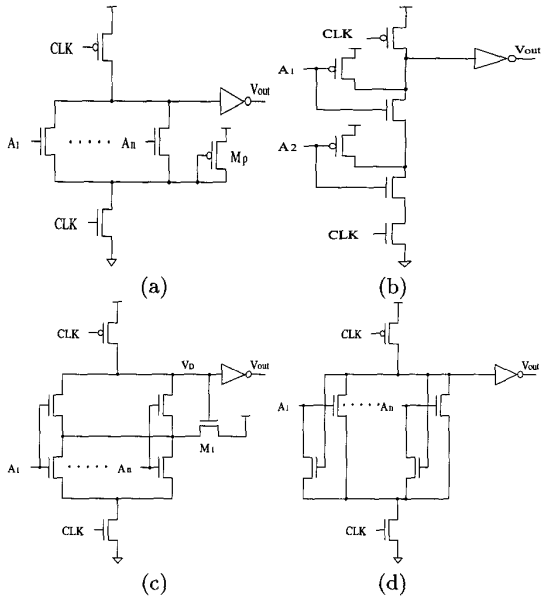

Figure 6: Noise-tolerant circuit techniques: (a) the PMOS pull-up, (b) the CMOS inverter, (c) the mirror, and (d) the twin-transistor techniques.

4.1 Noise-tolerant Circuit Design

Dynamic circuits, especially the wide-fanin OR gates using low V_t transistors for better pull-down speed, are error-prone due to their low switching threshold voltage $V_{st} = V_t$. Increasing V_{st} improves noise-immunity at the expense of power and/or performance. Nevertheless, we have already shown (see Fig. 5) that if the improvement in noise-immunity (i.e., reduction in ϵ) is sufficiently large compared with the energy penalty then the *minimum energy* consumed by the more complex noise-tolerant circuit will be smaller. Thus, noise-tolerant circuit techniques that effectively improve noise-immunity are required.

Several techniques have been developed so far to enhance the noise-immunity of dynamic circuits. The first technique referred to as the *PMOS pull-up technique* [4] (see Fig. 6(a)) utilizes a pull-up device to increase the source potential of the NMOS network thereby increasing the transistor threshold voltage V_t and V_{st} during the evaluate phase. This technique suffers from large static power dissipation. The *CMOS inverter technique* [2] utilizes a PMOS transistor for each input thereby adjusting V_{st} to equal that of a static circuit. This technique cannot be used for NOR-type circuits.

The *mirror technique* [31] (see Fig. 6(c)) utilizes two identical NMOS evaluation networks and one additional NMOS transistor M_1 to pull up the source node of the upper NMOS network to $V_{dd} - V_t$ during the precharge phase thereby increasing V_{st}. The mirror technique guarantees zero DC power dissipation but a speed penalty is incurred if the transistors are not resized.

The *twin-transistor technique* (see Fig. 6(d)) [5, 6] utilizes an extra transistor for every transistor in the pull-down net-

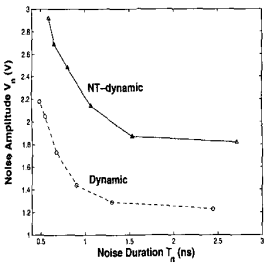

Figure 7: Measured noise-immunity curves for the twin-transistor technique.

work in order to pull up the source potential. The twin-transistor technique consumes no DC power. Both the mirror and twin transistor techniques have been experimentally proved via the design and test of prototype chips in $0.35\mu m$ CMOS technology in the ViPS laboratory at UIUC. Figure 7 shows that the measured improvement in NIC for the twin-transistor technique [6] is greater than $2.4X$ with a 15% increase in energy dissipation at the same supply voltage.

4.2 Algorithmic Noise-tolerance

Algorithmic techniques for handling intermittent errors in combination with noise-tolerant circuit techniques described in the previous subsection, have the potential of approaching the lower bounds on energy envisaged by the configuration in Fig. 4(b). Research in fault-tolerant computing has addressed this problem to some extent, however the solutions do not address the energy-efficiency issue. Recently, we have proposed the notion of algorithmic noise-tolerance (ANT) [11, 12], whereby the statistical properties of signals and the architecture are exploited to develop energy-efficient techniques for mitigating soft errors at the algorithmic level. These techniques work best in the context of DSP and communication systems where the system performance metrics are in terms of SNR and/or bit error-rate (BER), which are statistical quantities themselves.

The key idea behind ANT (see Fig. 8(a)) is to have a low-complexity error-free error control (**EC**) block that detects and corrects errors that may arise in a comparatively large main noisy (**MN**) block. This is precisely the scenario envisaged in Fig. 4(b). Indeed the complexity of the **EC** block is closely tied to the frequency of errors ϵ in the **MN** block which in turn depends upon the statistics of the signal as well as that of DSM noise, and the architecture. Thus, by proper tuning of ϵ via noise-tolerant circuit techniques (see section 4.1) and then applying ANT techniques raises a distinct possibility of approaching the lower bounds on energy dissipation derived in section 3.

ANT techniques can also be employed to improve energy-efficiency in scenarios where DSM noise is not a problem but where aggressive design techniques create DSM noise-like behavior at the algorithmic level. For example, scaling the supply voltage increases the propagation delay of a logic gate. Therefore, the achievable energy reduction via voltage scaling of a conventional DSP system is limited by a critical supply voltage $V_{dd-crit}$ which is determined by the system throughput requirement. In fact, $V_{dd,crit}$ is a function of the

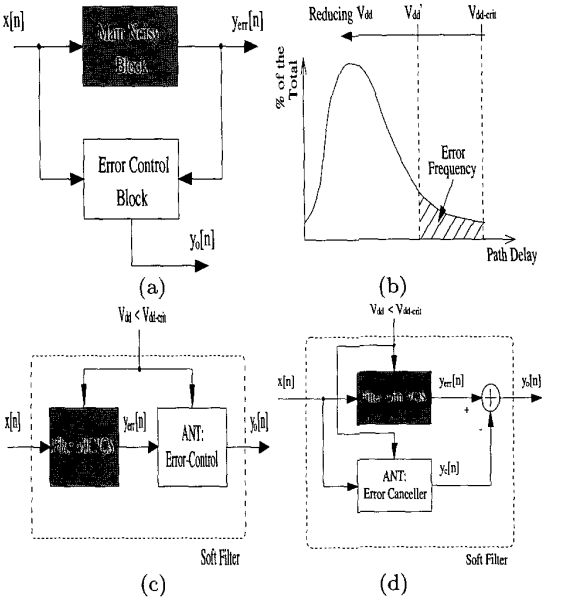

Figure 8: Algorithmic noise-tolerance (ANT) (a) and its use in soft DSP framework: (b) path delay distribution of a ripple-carry adder, (c) the prediction based error-control scheme, and (d) error-cancellation scheme.

critical path delay of the module. Figure 8(b) shows the path delay distribution of a ripple carry adder. Note that there is one critical path that determines the value of $V_{dd,crit}$. If the supply voltage is scaled beyond $V_{dd-crit}$ (referred to as *voltage overscaling* (VOS)) then intermittent errors occur at the adder output whenever the inputs exciting the critical path appear. If the adder is in a filtering block then this leads to a degradation in algorithmic performance which can be compensated for via ANT techniques. The resulting DSP system is referred to as *soft DSP* [11] as shown in Fig. 8(c)-(d).

For a frequency selective filter, we have shown recently that the soft DSP approach [11] employing the prediction based error control Fig. 8(b) provides $60\% - 80\%$ reduction in energy dissipation **over conventional voltage scaling** for filter bandwidths up to 0.5π with a marginal loss in SNR. The error-cancellation scheme in Fig. 8(c) similarly provides up to 70% reduction in energy dissipation by exploiting the relationship between the soft errors and the input in a statistical manner. Note that error-control algorithms such as the prediction-based error control do not rely on any particular properties of soft errors and hence are equally effective in the presence of DSM noise. Indeed, we have also shown that [11] the prediction based schemes are effective for DSM noise that result in an ϵ as high as 10^{-3}, i.e., each output bit is in error once in a 1000 samples.

5. NOISE IN ANALOG CIRCUITS

In this section, we describe the fundamental noise mechanisms in DSM devices and the impact of these noise sources in RF circuits.

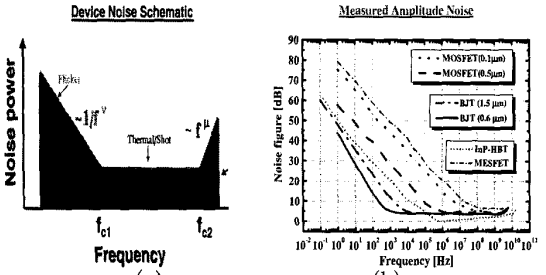

Figure 9: Device noise: (a) schematic of device noise indicating three distinct frequency regimes and (b) measured results.

5.1 Fundamental Noise Mechanisms

The fundamental noise mechanisms in semiconductors [8, 18, 33] are due to random motion of charge carriers in a force free environment (thermal noise), discrete flow of charge in a field (shot noise), and generation-recombination of carriers interacting with traps (flicker noise). The equations for the power spectral density (PSD) of current fluctuations due to flicker noise (S_i^F), shot noise (S_i^S) and thermal noise (S_i^T) are given by

$$S_i^F = K\frac{I^\alpha}{f^\beta} \tag{15}$$

$$S_i^S = 2qI \tag{16}$$

$$S_i^T = 4kTR \tag{17}$$

where R is the resistance of the material, T is the temperature, I is the steady state current, and K is a material specific constant. Note that both thermal and shot noise are frequency independent while flicker noise has an explicit frequency and bias dependence.

5.2 Device Noise

The fundamental noise sources described in section 5.1 contribute to device noise through superposition from various regions of the device. Fig. 9(a) shows a schematic of the device noise PSD as a function of frequency. Flicker noise dominates at low frequencies (below $f_{c1} = 1MHz$) exhibiting what is known as the $1/f$ behavior. Between f_{c1} and $f_{c2} = 1GHz$, the dominant noise sources are the frequency independent thermal and shot noise mechanisms. Above f_{c2}, device noise exhibits an increase with frequency due to reactive components (e.g. capacitances) coupling thermal/shot noise between different regions of the device.

Expressions for various noise power spectral densities in BJTs and MOSFETs can be derived from those of the fundamental noise mechanisms as described in (15)-(17) using the basic lumped circuit models of the devices [18, 19]. For example, the flicker noise PSD due to the drain current in a MOSFET is given by,

$$S_{I_D}^F = K_D\frac{I_D^\alpha}{f^\beta} \tag{18}$$

where I_D is the drain current.

The noise figure of a device and is a measure of the noise power added to an input signal by the active device. Fig. 9(b) shows measured amplitude noise in various device technologies showing clearly the the three major frequency regions discussed. It can be seen that BJTs, in general, exhibit a lower level of flicker noise as compared to MOSFETs.

5.3 Noise in High-speed Circuits

Amplifier noise is a small-signal phenomenon and can thus be treated by a linear approximation. It is directly determined by the noise and gain of the devices used in the design. The noise figure of an amplifier can be computed from the noise parameters of the active devices used in the circuit. The major noise source in **oscillators** is phase noise caused by mixing of device noise (flicker, shot, thermal) with the carrier frequency due to the nonlinear operation of the circuits. In general, noise in oscillators is a large-signal phenomenon and hence linearization techniques have limited applicability. Thus, advanced analytical and numerical techniques [3] are required.

In digital circuits, the timing of pulses exhibits a random fluctuation as a function of time referred to as **jitter** which becomes a serious problem as clock frequencies increase into the GHz regime. Jitter is fundamentally caused by the noise of individual components of the circuit (active devices, resistors, interconnect delays, etc.) and results in fluctuations around a fundamental period of oscillation. This fluctuation has a standard deviation σ_t that is used as a measure of jitter. For example, the thermal noise of transistor input resistances is shown to give rise to a jitter of the form

$$\sigma_{R_x}^t = \sqrt{4kTR}F(I_E, C_c). \tag{19}$$

Similarly, other noise sources at the oscillator input will modulate the fundamental frequency and contribute proportionally to jitter.

Interconnects in VLSI chips are a source of noise referred to as cross-talk, which originates from capacitive and inductive coupling of signals between adjacent lines. A quantitative treatment of cross-talk requires an appropriate modeling of interconnect as transmission lines. The magnitude of the cross-talk between two lines is determined by their mutual capacitance C_m and mutual inductance L_m. Since the capacitive noise is proportional to $C_m dV/dt$ and the inductive noise is proportional to $L_m dI/dt$, cross-talk can be treated as being proportional to V_{dd}/t and proportional to I_{sat}/t, where t is the pulse rise or fall time.

Another more fundamental source of noise in VLSI interconnects is the thermal noise of transmission lines. It can be shown that by treating interconnect as a distributed transmission line, the thermal noise can be expressed as

$$S_v^T = 4kTRF(\gamma, l) \tag{20}$$

Here the thermal noise due to the resistance R of the interconnect is modified by a function of only the propagation coefficient γ and the total length l of the interconnect.

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