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ENERGY-EFFICIENCY BOUNDS FOR NOISE-TOLERANT DYNAMIC CIRCUITS

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ABSTRACT

Presented in this paper are lower bounds on energy-efficiency of the *mirror* noise-tolerant dynamic circuit technique. These lower bounds are derived by solving an energy optimization problem subject to an information-theoretic constraint. Design overheads associated with the noise-tolerant circuit techniques are discussed and incorporated into the optimization problem. Simulation results for a 3-input OR gate transferring information at a rate $R = 150Mbits/sec$ in 0.35μm CMOS indicate that the lower bound on energy consumption of the noise-tolerant circuit is $25fJ/bit$, which is 31% below that of the conventional domino circuit. This lower bound is achieved when the noise-immunity of the mirror technique is $1.64X$ more than that of the domino circuit technique.

1. INTRODUCTION

With feature sizes being reduced from the current 0.18μm to future $0.1 - 0.05\mu$m generations, noise has emerged as a new factor that may ultimately determine the performance achievable in future microprocessors at an affordable cost. The *1999 International Technology Roadmap for Semiconductors* [1] indicates that integrated circuits and systems in the year 2008 will need to be designed with high-leakage transistors, large V_t variations, low supply voltages, operating with high clock-frequencies, in the presence of ground bounce, IR drops, crosstalk and clock jitter. *Deep submicron* (DSM) noise has emerged as the primary cause of a reliability problem that challenges the very foundation of the cost and performance benefits of very large scale integration.

At the same time, future 3G wireless systems are driving the need for energy-efficient design techniques. Energy optimization techniques have been studied [2] at various levels of design abstraction from technology to system/algorithmic levels. While low-power design is still an active area of research, not much work has been done in developing power reduction techniques in the presence of noise. In other words, reliability and energy-efficiency issues have not been addressed together. Preliminary results on this problem have been reported recently in [3, 4].

Given the advent of DSM noise, it has also become important to determine the limits to which energy-efficiency can be improved without sacrificing reliability. While low-power design techniques reduce energy, they do not enable us to determine the lower bounds on energy-efficiency that can be achieved. In particular, the lower bounds need to be a function of DSM noise and the complexity of the algorithms being employed. In the past, we have proposed an *information-theoretic framework* [5, 6] that enables us to determine these lower bounds in a rigorous manner. Past work [6] has determined these lower bounds for static circuits. In this paper, we consider dynamic circuit techniques such as domino [7] and noise-tolerant domino [3]. In particular, we compare the energy-efficiency bounds for conventional domino and noise-tolerant domino circuit techniques and determine to what extent noise-immunity needs to be enhanced before the energy overhead starts to dominate. It is known that noise-tolerant circuit techniques [3, 4, 8, 9] invariably consume more energy due to the additional circuit elements needed to enhance the noise-immunity. Thus, one would expect noise-tolerant circuit styles to be less energy-efficient than conventional techniques. However, for the same degree of noise-immunity, we have shown [4] that noise-tolerant circuits consume 30% less energy than conventional dynamic circuits. In this paper, we further demonstrate that noise-tolerance improves the energy-efficiency of circuits when operating at the lower bound.

In section 2, we briefly review our past work on developing an information-theoretic framework for DSM circuits. In section 3, we present the models for power and speed for dynamic circuits and formulate the optimization problem whose solution provides us with the lower bounds on the energy-efficiency. In section 4, we determine the lower bounds on energy dissipation of domino circuits and noise-tolerant dynamic circuits by solving the optimization problem formulated in section 3.

2. INFORMATION-THEORETIC FRAMEWORK: A REVIEW

In this section, we briefly introduce the *information-theoretic framework* for deriving the lower bounds on energy dissipation of noisy logic gates.

Consider a 2-input OR gate as shown in Fig. 1(a), where the input X is generated randomly from $S_x = \{00, 01, 10, 11\}$. In the presence of DSM noise, the output Y can be in error. Thus, Y can be considered as a binary random variable with a finite probability of error given by

$$\epsilon \triangleq P(Y \neq y|_x), \tag{1}$$

where $Y = y|_x$ is the output obtained in the absence of noise when the input $X = x$. The noisy OR gate can be represented

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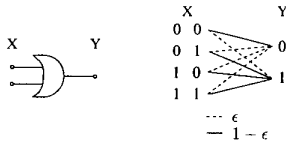

(a) (b)

Figure 1: A simple information transfer system: (a) two-input OR gate and (b) the corresponding channel model.

by the discrete-channel model [6] shown in Fig. 1(b). Note that the probability of error ϵ for a noise-tolerant OR circuit will be smaller than that for a conventional circuit when presented with similar noise environments.

We now distinguish between an *algorithm* and its *implementation*. The OR algorithm has a computational complexity that we capture in terms of the *information transfer rate* requirement $R = f_s H(Y)$ bits/sec, where f_s is the rate at which the input is arriving and $H(Y)$ is the output entropy given by

$$H(Y) = -p_y \log_2(p_y) - (1 - p_y) \log_2(1 - p_y), \qquad (2)$$

where p_y is the probability that $Y = 1$.

The OR implementation in Fig. 1(b) is a noisy channel that has an *information transfer capacity* C which is given by

$$C = \max \left[f_c \left[h(p_y) - h(\epsilon) \right] \right], \qquad (3)$$

where $h(x) = -x \log_2(x) - (1 - x) \log_2(1 - x)$ is the *entropy function*, p_y is the probability of the output Y being "1" ($p_y = t$ for domino circuits, where t is the output transition probability), and f_c is the maximum signaling rate. Note that f_c is the rate at which the noisy OR gate is being used and this rate can be different from f_s (the input rate) because of coding.

From (3), we make note of the fact that ϵ depends upon the DSM noise and the noise-immunity of the OR gate, while f_c depends upon the supply voltage, load capacitance, circuit style and process parameters. Thus, the information transfer capacity C is a composite function of circuit, process and noise parameters. Information theory [10] indicates that it is possible to achieve reliable operation by coding the input as long as $C > R$. In [5, 6], we showed that the lower bounds on energy-efficiency can be obtained by solving the following optimization problem

$$\begin{aligned} &\textit{minimize:} && E_b = \frac{P_{tot}}{R}, \\ &\textit{subject to:} && \left[h(p_y) - h(\epsilon) \right] f_c = R, \end{aligned} \qquad (4)$$

where E_b is the *energy per information bit* and P_{tot} represents the total power dissipation. The solution to (4) results in $C \approx R$.

In this paper, we compare the lower bounds on energy-efficiency of conventional domino and the mirror noise-tolerant dynamic circuit technique [3].

3. MODELS FOR POWER, SPEED AND NOISE-IMMUNITY

In this section, we derive the lower bounds on energy-efficiency of conventional domino and noise-tolerant dynamic circuits by solving (4). In order to achieve this, we determine ϵ, f_c and P_{tot} in terms of V_{dd} for conventional domino and the mirror technique so that (4) can be solved.

The models of power and speed presented in this section are by no means the most accurate as they assume simplified transistor models. In fact, obtaining accurate device models for DSM technologies is an active area of research in its own right. However, the models in this section will suffice for the purpose of this paper where we illustrate the method for obtaining lower bounds on energy dissipation.

3.1. Power Model

In digital CMOS circuits, the total average power dissipation is given by

$$P_{tot} = P_{cap} + P_{sc} + P_{stat}, \qquad (5)$$

where P_{cap}, P_{sc} and P_{stat} are the capacitive, short-circuit and static power dissipations, respectively. The capacitive component P_{cap} is given by

$$P_{cap} = t C_L {V_{dd}}^2 f_c, \qquad (6)$$

where t is the transition probability, C_L is the load capacitance, V_{dd} is the supply voltage, and f_c is the signaling rate. Note, for dynamic circuit styles, the transition probability t equals the probability of output being "1".

The average short-circuit power dissipation P_{sc} in dynamic circuits can be described as

$$P_{sc} = t \overline{I_{sc}} V_{dd}, \qquad (7)$$

where $\overline{I_{sc}}$ denotes the average short-circuit current evaluated over each signaling period. We include the transition probability t in (7) because the short-circuit current I_{sc} is present only when the output switches to "1". In section 4, we will show that both conventional domino circuits (with keepers) and noise-tolerant dynamic circuits consume non-trivial short-circuit power.

The static power dissipation has two components

$$P_{stat} = P_{sl} + P_{DC}, \qquad (8)$$

where P_{sl} is due to the subthreshold leakage current and P_{DC} is due to the DC current. The subthreshold leakage power dissipation P_{sl} can be approximated by [11]

$$P_{sl} = I_s e^{-V_t / V_T} V_{dd}, \qquad (9)$$

where I_s is a technology and device size dependent constant, V_t is the NMOS threshold voltage, and V_T is the thermal voltage, which equals $26mV$ at room temperature. For future DSM technologies, P_{sl} is predicted to become comparable to capacitive power dissipation. The mirror technique [3] does not consume any DC power (though the certain existing noise-tolerant circuit techniques [9] do consume DC power) and hence in this paper we do not include P_{DC} in the optimization problem.

3.2. Speed Model

Many noise-tolerant dynamic circuit techniques are based on the principle shown in Fig. 2, where a current source $i_{pull-up}$ is introduced to compensate for the leakage current that would be flowing through the NMOS transistor when the noise pulse V_n appears due to DSM disturbances. This increases the propagation delay. The

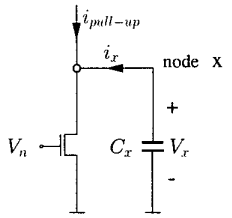

Figure 2: The principle behind noise-tolerant schemes for dynamic circuits.

impact of noise-tolerance on the delay can be accounted for as follows

$$f_c = \frac{(V_{dd} - V_t)^\alpha}{2V_{dd}} \left(\frac{k_{eff}}{C_L}\right)_{critical}, \qquad (10)$$

where k_{eff} denotes the effective transconductance of the balanced NMOS/PMOS transistors and α is the velocity saturation index ranging from 1 (velocity saturated) to 2 (without velocity saturation). Note that k_{eff} will be smaller for noise-tolerant circuits as compared to conventional circuits.

3.3. Probability of Error ϵ

The error probability ϵ for a circuit can be obtained from the *noise immunity curves* (NICs) [3] shown in Fig. 3(a) for a domino gate and the mirror circuit technique in 0.35μm CMOS. A point on the NIC indicates the duration and amplitude of the input noise pulse V_n that will cause an output error. Thus, noise pulses corresponding to the points that lie above the NIC will cause output errors. Clearly, the more noise-immunity a circuit technique is, the higher its NIC will be. Further, the NIC is also a function of the supply voltage.

Assume that the evaluation time equals $T_c/2 = 1/(2f_c)$ and that the corresponding point on the NIC is denoted by V_N. Given a noise model that consists of a distribution on the amplitude and duration, $f_{V_n,T_n}(v,t)$ as shown in Fig. 3(b), the error probability ϵ can be obtained by

$$\epsilon = \int_{V_N}^{\infty} \int_{t_v}^{T_c/2} f_{V_n,T_n}(v,t) dt dv, \qquad (11)$$

where the second integral starts from t_v (determined by the variable v of the first integral and the given NIC) and ends at $T_c/2$. Note that, from (11), ϵ is a function of V_{dd} because both T_c (see (10)) and V_N are functions of V_{dd}. From Fig. 3, noise-tolerant dynamic circuits will have a smaller probability of error ϵ as compared to conventional domino circuits. As $h(x)$ is a monotonically increasing function of x for $x < 0.5$, from (4), a smaller value of ϵ can be utilized to reduce the transition probability t while still satisfying the information-theoretic constraint. A net reduction in the overall power dissipation will occur if the energy savings due to the reduced t dominates the overhead due to noise-tolerance techniques.

4. COMPUTATION OF LOWER BOUNDS ON ENERGY-EFFICIENCY

For a given information transfer rate R, the lower bound on energy dissipation can be obtained by solving (4), where P_{tot}, f_c, and ϵ

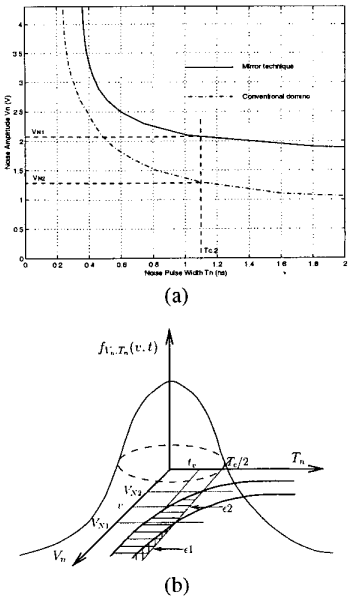

Figure 3: Noise immunity curves and noise distribution: (a) NIC and (b) determining ϵ from NIC.

are given by (5)-(8), (10), and (11), respectively. We start with the minimum possible supply voltage $V_{dd,min}$, where $V_{dd,min}$ is the supply voltage when $p_y = 1/2$ in (4), and then increase V_{dd} in small steps. Note, increasing V_{dd} results in a faster speed (higher f_c) and hence we can decrease t while still satisfying the information-theoretic constraint. The minimum energy consumption corresponding to each V_{dd} can thus be found by solving (4).

Fig. 4 shows two 3-input OR gates implemented by the conventional domino (with a keeper) and the mirror technique, both designed in 0.35μm, 3.3V, CMOS technology. We include only P_{cap} and P_{sc} as these designs consume no P_{DC}, and P_{sl} is relatively small for this technology ($V_t = 0.6V$).

As we designed the two circuits with the same speed, the pull-down NMOS transistors in Fig. 4(b) are sized up resulting in larger parasitic capacitances. We account for this design overhead by extracting the capacitances from the layout and adding them to a $30fF$ load capacitor for each design. In the simulation, we choose the information transfer rate $R = 150Mbits/sec$. The minimum supply voltage for this transfer rate is around $1.1V$. We assume noise amplitude V_n to be zero mean Gaussian with $\sigma_n = 400mV$, and noise duration T_n to be uniformly distributed between 0 and $T_c/2$.

There are two methods to tune ϵ in the mirror technique: 1.) by changing the power supply V_{dd-nt} and 2.) by resizing transistor M1. These two approaches result in different energy and throughput overheads. Hence, we will evaluate them separately.

Fig. 5 illustrates the lower bounds on energy dissipation for a domino 3-input OR gate and a noise-tolerant 3-input OR gate when $V_{dd-nt} = 1.5V_{dd}$, $1.0V_{dd}$, $0.75V_{dd}$, and $0.5V_{dd}$, respectively, with transistor M1 being 4 times the minimum size. The lower bound on energy dissipation of the conventional domino gate is found to be $36fJ/bit$, whereas that of the mirror tech-

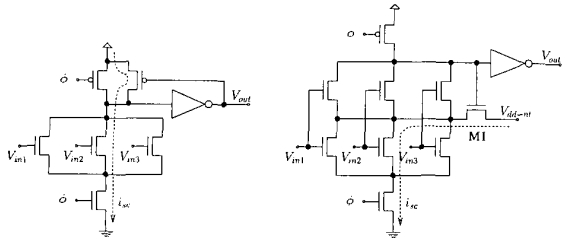

Figure 4: Dynamic style 3-input OR gates: (a) conventional domino and (b) the mirror technique.

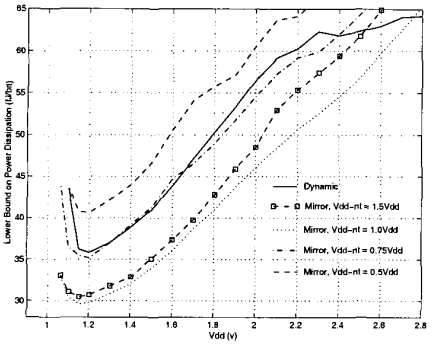

Figure 5: Lower bounds on energy dissipation for different V_{dd-nt}.

nique with $V_{dd-nt} = V_{dd} = 1.15V$ is $30fJ/bit$, which is 17% lower. This implies that noise-tolerant designs are more energy-efficient than conventional domino designs when operating at the lower bound. For V_{dd-nt} values around V_{dd}, the lower bound on energy-efficiency increases indicating that $V_{dd-nt} = V_{dd}$ is the optimal solution. If $V_{dd-nt} = 1.5V_{dd}$ then P_{sc} starts to dominate and if $V_{dd-nt} = 0.75V_{dd}$ then ϵ starts to increase and so does t.

Fig. 6 illustrates the lower bounds on energy dissipation for a domino 3-input OR gate and noise-tolerant 3-input OR gates with transistor M1 being 4, 8, and 12 times minimum size and $V_{dd-nt} = V_{dd}$. We observe that up-sizing transistor M1 leads to a smaller ϵ, but at the same time results in larger parasitic capacitances and short-circuit current. The optimum trade-off between the noise-immunity and energy consumption is found when M1 is 8 times the minimum size, where the lower bound on energy dissipation is $25fJ/bit$. This is 31% below that of the conventional domino gate. Increasing the width of M1 further makes the energy overhead offset the noise-immunity improvement, thus resulting in a higher energy bound.

Also can be seen in Figs. 5–6 that the minimum power supply voltage of noise-tolerant circuits is lower than that of conventional domino circuits. This is because a smaller ϵ leads to a smaller signaling rate f_c when the transition probability t achieves its maximum value (see (4)). In addition, consistent with our past work [6] is the observation from Figs. 5–6 that the minimum supply voltage for reliable operation is smaller than the voltage for the minimum energy.

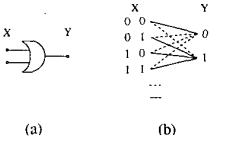

Figure 6: Lower bounds on energy dissipation for different M1.

5. CONCLUSIONS

In this paper, we compare the energy-efficiency bounds for conventional domino and noise-tolerant domino circuits. We have shown that noise-immunity enhancing techniques improve the energy-efficiency of circuits when operating at the lower bound. Future work on this topic includes the computation of bounds on energy-efficiency for complex VLSI blocks and development of design techniques that approach these bounds.

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