A Low-power Multimedia Communication System for Indoor Wireless Applications

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Abstract

A low-power multimedia communication system is proposed. Power reductions are achieved by employing *dynamic algorithm transforms* and *joint source-channel coding* to reconfigure the system in the presence of variabilities in source and channel data. Configuration parameters are source rate, error correction capability of the channel encoder/decoder, number of powered-up fingers in the RAKE receiver and transmit power of the power amplifier. Energy-optimum configurations are obtained by minimizing energy consumption under the constraints of end-to-end distortion and total transmission rate. The proposed system is tested over a variety of images, distances (ranging from 2 to 100 meters) and multipath channels. Simulation results using $0.18\mu m$, $2.5V$ CMOS parameters show that the reconfigurable system can achieve average energy savings of 59% as compared to a fixed system designed for the worst case. Also, the proposed system consumes 16% less energy as compared to a transmit-power-controlled system.

1 Introduction

With the emergence of personal communication services (PCS) [1], portable multimedia systems are expected to be used more frequently and for longer durations. This requires that power consumption [2] in these systems be kept at a minimum in order to extend the battery life. In contrast, multipath fading in radio channels combined with the need to transmit multimedia data necessitates the use of large transmit power and complex signal processing algorithmsthus reducing the battery life. In current day cellular phones, the bulk of the power is consumed in the power amplifier that generates the transmit power. However, as we move towards an era of micro-cells and pico-cells, power consumption of the baseband processing unit becomes comparable to that of the power amplifier. Efforts such as Bluetooth (`http://www.bluetooth.com`) for short-range radio links in portable devices such as mobile PCs and mobile phones, as well as the HomeRF (`http://www.homerf.org`) open industry specification for RF digital communications in the home, are some examples of steps toward pico-cell communications. Therefore, techniques which jointly minimize the power consumption in the power amplifier and the baseband processing unit are desirable.

There are several options for hardware platforms for implementing the digital components. On one end of the spectrum are programmable DSPs which offer

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higher flexibility at the expense of higher power consumption and low throughput. On the other end are ASICs with low power and high throughput at the cost of lower flexibility. Reconfigurable computing platforms such as FPGAs and domain-specific processors [3] seek to maintain the flexibility attributes while improving the throughput. Our approach to the design of reconfigurable DSP is to add just the right degree of flexibility (as demanded by the application) to the ASICs resulting in application specific reconfigurable integrated circuits (ASRICs). The ASRIC approach is suitable for mobile multimedia systems of the future as it maintains the energy and throughput efficiency of ASICs.

A design methodology for low-power ASRICs termed as *dynamic algorithm transforms (DAT)* wa proposed in [4]. The energy savings are achieved by tailoring the algorithm/architecture to data/channel variabilites. DAT requires the definition of: (1) input state-space, (2) configuration-space, (3) energy models and (4) DSP models. The input state-space models the input variabilities and the configuration-space is the set of hardware configurations. The energy model relates the configuration to energy. DSP models provide a link between DSP algorithm design, the input state-space and the configuration-space. In this paper, we focus on the design of a reconfigurable wireless multimedia communication system that achieves low-power by exploiting the variabilities in the multimedia data and the wireless channel. In order to achieve this goal, we employ recent advances in joint source-channel coding (JSCC) [5] and DAT [4].

The proposed system can be motivated as follows. Figures 1(a) and 1(b)

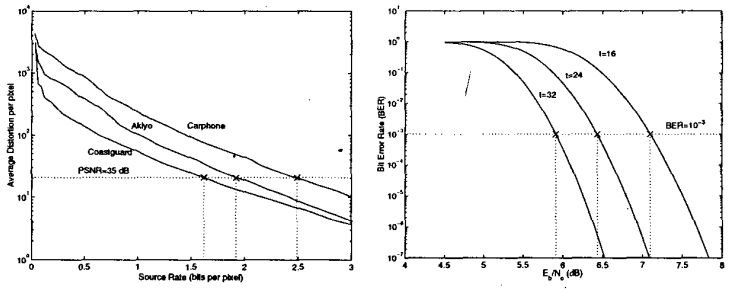

Figure 1: (a) Source variabilities (rate-distortion curves) and (b) channel variabilities (bit-error-rate curves).

show the effect of variabilities in source (different images) and channel (different E_b/N_0s) on the rate-distortion curves (for set partitioning in hierarchical trees (SPIHT) [6] coder) and bit-error rate (BER) curves (for Reed Solomon (RS) coder), respectively. Thus, if the image changes from "*coastguard*" to "*carphone*" and the channel E_b/N_0 changes from $5dB$ to $7dB$, then to keep the $PSNR$ same, one can adjust the source rate and the number of correctable errors t. Out of the numerous choices, the optimal selection of parameters is obtained via joint source-channel coding techniques and dynamic algorithm transforms. The proposed system is tested is employed in an indoor office environment and

tested via the evaluation methodology in [7]

The rest of the paper is organized as follows. In next section, we present an overview of the system. In section III, we present the key ingredients such as energy and DSP models. The simulation results are presented in section IV.

2 Indoor Wireless Multimedia System

An indoor wireless multimedia communication system is shown in Figure 2. The mobile terminal is characterized by the parameter vector $[R_s, t, P_t, \mathbf{c}_{rake}]$, where R_s is the source rate (in *bits per pixel*), t is the number of correctable symbol errors, P_t is the transmit power (in mW) and $\mathbf{c}_{rake}$ is the configuration vector for the RAKE receiver. This system is suitable for environments with short distances ($< 100m$) and slow/block fading channels.

The use of DAT requires the definition of: (a) an input state space $\mathcal{S}$, (b) a configuration space $\mathcal{C}$, (c) DSP models for estimating distortion $\mathcal{D}$, and (d) energy models for estimating energy consumption $\mathcal{E}$. In this section, we present $\mathcal{S}$, $\mathcal{C}$ and energy optimization problem. The DSP and energy models are presented in section III.

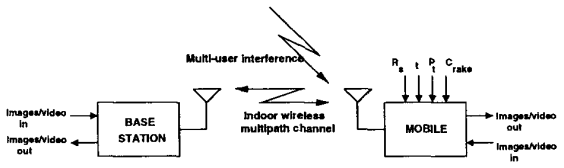

Figure 2: Indoor wireless multimedia communication system.

2.1 Input State Space

The input state space $\mathcal{S}$ is a collection of all input states or scenarios of interest for which reconfiguration is desired. The size of $\mathcal{S}$ depends upon the input variabilities and the granularity of the reconfigurable hardware. For example, the state vector s in the context of a wireless multimedia communication system is defined as:

$$\mathbf{s}=[(r_1, d_1), (r_2, d_2), \cdots, (r_K, d_K), h_1, h_2, \cdots, h_L], \tag{1}$$

where (r_i, d_i)s are points on the rate-distortion (R-D) curve (see Figure 1(a)), and h_is are the complex gains in the multipath channel impulse response,

$$h(t) = \sum_{i=1}^{L} h_i \delta(t - \tau_i), \tag{2}$$

where τ_i is delay corresponding to the i^{th} path. As shown in Figure 2, in addition to multipath, there is also multiuser interference which can be exploited by employing a reconfigurable multiuser receiver. In this paper, for the sake of simplicity, we ignore the variabilities in multiuser interference and exploit variabilities due to source and multipath channels. In section IV, we employ channel models representing the worst-case interference.

2.2 Configuration Space

The configuration space $\mathcal{C}$ is the set of hardware configurations. The definition of configuration vector and size of $\mathcal{C}$ is dependent upon the algorithm and the hardware platform. Figure 3 shows a detailed block diagram of the reconfigurable multimedia communication system. The blocks within dotted lines in Figure 3(a) are reconfigurable and the others are fixed/hardwired. All digital blocks (to the left of ADC and DAC) except the source codec are assumed to have an ASIC implementation with $0.18\mu m$, $2.5V$ standard cell CMOS technology. The source codec is implemented on a programmable processor and is assumed to have a fixed energy consumption. This is because the energy consumption of the main computational block (frequency transform or subband decomposition) is usually independent of the source rate R_s. Similarly, the modulators, square-root raised cosine filters, ADC, DAC and low-noise amplifier are fixed. We assume that the analog blocks (to the right of and including ADC and DAC) presented in [8] are being employed.

The configuration vector is defined as follows:

$$\mathbf{c} = [R_s, t, \mathbf{c}_{rake}, P_t], \tag{3}$$

where R_s is the source rate (in bits per pixel), t is the number of errors the channel codec can correct, $\mathbf{c}_{rake}$ is configuration vector for the RAKE receiver ($c_{rake,i} = 0$ implies that i^{th} finger is powered down) and P_t is the transmit power (or output power delivered by the power amplifier). We assume that the

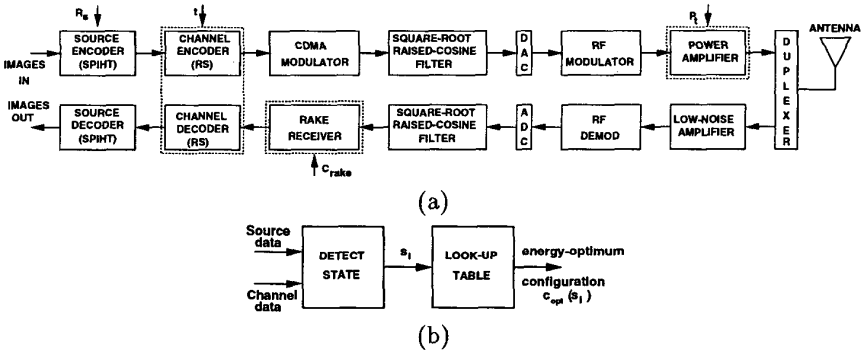

Figure 3: A reconfigurable multimedia system: (a) transceiver and (b) controller.

source and channel codecs are SPIHT [6] and Reed-Solomon, respectively.

Figure 3(b) shows the block diagram of the controller. The first block in the controller detects the input state $\mathbf{s}_i$ (see (1)), while the second block stores the energy-optimum configurations $\mathbf{c}_{opt}(\mathbf{s}_i)$ obtained by solving an energy optimization problem, which is described next.

2.3 Energy Optimization Problem

We want to determine the configuration vector $\mathbf{c}_{opt}(\mathbf{s}_i)$ which minimizes energy consumption per pixel while satisfying constraints on (1) distortion $\mathcal{D}$ per pixel (defined as mean squared error between the original image at the transmitter input and the reconstructed image at the receiver output) and (2) total rate R_{tot} (which is defined as sum of source and channel bits per pixel). Therefore, the energy optimization problem can be written as:

$$\begin{aligned} \mathbf{c}_{opt}(\mathbf{s}_i) &= \arg\min_{\mathbf{c}\in\mathcal{C}} \mathcal{E}(\mathbf{c}) \\ s.t. \quad & \mathcal{D}(\mathbf{c}, \mathbf{s}_i) \leq \mathcal{D}_o \\ & R_{tot}(\mathbf{c}) \leq R_o, \end{aligned} \tag{4}$$

where $\mathcal{E}(\mathbf{c})$ is sum of the energy consumption of the reconfigurable blocks given by,

$$\mathcal{E}(\mathbf{c}) = \mathcal{E}_{rscodec}(t) + \mathcal{E}_{rake}(\mathbf{c}_{rake}) + \mathcal{E}_{pa}(P_t), \tag{5}$$

where $\mathcal{E}_{rs}$, $\mathcal{E}_{rake}$ and $\mathcal{E}_{pa}$ are the energy consumption of the RS codec, RAKE receiver and power amplifier, respectively. The energy consumptions of the source encoder and other hardwired blocks are not included in the optimization problem. The optimization problem in (4) represents the core of DAT where energy is minimized subject to a system-level performance constraint. The constraints themselves are satisfied via joint source-channel coding algorithms.

The energy and DSP models employed in the estimation of $\mathcal{E}(\mathbf{c})$ and $\mathcal{D}(\mathbf{c}, \mathbf{s})$ are described next.

3 Energy and DSP Models

In this section, we present relationships between energy consumption, distortion, input state and the configuration vector.

3.1 Energy Models

Energy models are employed to relate the configuration vector to a high-level estimate of the energy consumption of the algorithm. In the following, we present energy models for the RS codec, the RAKE receiver and the power amplifier. These models are obtained via real-delay simulations [9] of the hardware blocks employing $0.18\mu m$, $2.5V$ CMOS standard cells obtained from `http://www.chips.ibm.com/techlib/products/asics/databooks.html`.

1. RS Encoder/Decoder

The energy models [10] for adder, multiplier and inverse blocks over Galois Field ($GF(2^m)$) are given by

$$\mathcal{E}_{gfadd} = 3.3 \times 10^{-5} m \quad (mW/MHz) \tag{6}$$

$$\mathcal{E}_{gfmult} = 3.7 \times 10^{-5} m^3 \quad (mW/MHz) \tag{7}$$

$$\mathcal{E}_{gfinv} = 3.7 \times 10^{-5} (2m-3) m^3 \quad (mW/MHz), \tag{8}$$

where m is the number of bits per symbol. These models are employed to obtain an estimate of the energy consumption of RS codec in different configurations given as follows:

$$\mathcal{E}_{rscodec}(t) = 6t(2^m - 1 + t)\mathcal{E}_{gfmult} + 6t(2^m - 1 + t/3)\mathcal{E}_{gfadd} + 3t\mathcal{E}_{gfinv} \ / \ codeword. \tag{9}$$

2. RAKE Receiver

Energy consumption of the RAKE receiver in Figure 4(a) is dependent upon the powered-up fingers (i.e. taps for which $c_{rake,i} = 1$). Figure 4(b) shows

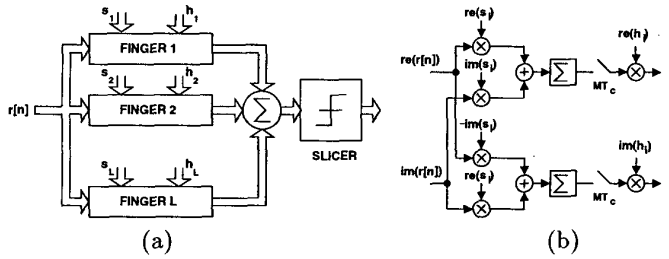

Figure 4: The RAKE receiver: (a) block diagram and (b) architecture of a finger.

architecture of a finger in RAKE receiver. The received signal $r[n]$ is correlated with the delayed spreading sequences $s_i = s[n - \tau_i]$ and then multiplied by a complex gain h_i^*. The outputs from all the fingers are added together and passed to the slicer to obtain the bits. If L is the number of fingers, then energy consumption of the RAKE receiver is given by,

$$\mathcal{E}_{rake}(\mathbf{c}_{rake}) = \sum_{i=0}^{L-1} c_{rake,i}\mathcal{E}_{rake,i} \ / \ bit, \tag{10}$$

where $\mathcal{E}_{rake,i}$ is the energy consumed by the i^{th} finger of the RAKE receiver. The multiplier energy models given in [4] are employed for estimates of $\mathcal{E}_{rake,i}$.

3. Power Amplifier

Energy consumption of the power amplifier is characterized by its power-aided-efficiency (PAE) η (defined as the ratio of the output power P_t to the power drawn from the supply). Power amplifiers are typically designed to maximize η at the maximum output power $P_{t,max}$, with η being a decreasing function of P_t.For the digitally-programmable power amplifier in [8], the efficiency $\eta(P_t)$ of this power amplifier can be approximated as follows:

$$\eta(P_t) = \eta_{max}\sqrt{\frac{P_t}{P_{t,max}}}, \tag{11}$$

where η_{max} is the maximum efficiency, and $P_{t,max}$ is the maximum transmit power. If f_{bit} is the bit-rate, then the power amplifier energy consumption per

bit $\mathcal{E}_{pa}$ is given by,

$$\mathcal{E}_{pa}(P_t) = \frac{P_t}{f_{bit}\eta(P_t)} \ / \ bit. \tag{12}$$

3.2 DSP Models

DSP models are employed to relate the configuration vector to the DSP performance metric such as distortion, bit error rate (BER) or signal-to-noise ratio (SNR). In the following, we present DSP models for the source coder, channel coder, RAKE receiver and power amplifier.

1. Source Coder

The DSP performance metric for the source coder is average distortion per pixel and is computed [5] as follows:

$$\mathcal{D}(\mathbf{s}, \mathbf{c}) = \sum_{i=0}^{M-1} D(i)p(i) + D(M), \tag{13}$$

where M is the number of codewords transmitted per image, $D(i)$ is the distortion value if only the first i codewords are correctly received, $p(i)$ is the probability of receiving the first i codewords correctly and $(i+1)^{th}$ codeword in error and $D(M)$ is the residual distortion because of a finite source rate R_s. The $D(i)$ values are obtained from the rate-distortion curve. The $p(i)$ values are obtained from the code error probability and is given by:

$$p(i) = (1 - p_{e,c})^i p_{e,c}, \tag{14}$$

where $p_{e,c}$ is the probability of error for the channel coder.

2. Channel Coder

The DSP performance metric for the channel coder is the probability of error $p_{e,c}$. For a Reed-Solomon code with codeword length of $2^m - 1$ symbols and error correction capability of t symbols, we have

$$p_{e,c} = \sum_{j=t+1}^{2^m-1} \binom{2^m - 1}{j} p_{e,s}^j (1 - p_{e,s})^{2^m - 1 - j}, \tag{15}$$

where $p_{e,s}$ is the symbol error probability and is computed as:

$$p_{e,s} = 1 - (1 - Q[\sqrt{SNR_o}])^m, \tag{16}$$

where SNR_o is the signal-to-noise ratio at the output of the RAKE receiver and $Q[x]$ is the probability that a standard Gaussian random variable has value greater than x.

3. Power Amplifier and RAKE Receiver

The DSP performance for the power amplifier and RAKE receiver is defined by SNR_o and is computed as:

$$SNR_o = \frac{P_t PL(d)}{P_n} \sum_{i=0}^{L-1} c_{rake,i} |h_i|^2, \tag{17}$$

where P_t and P_n are the transmit power and noise power respectively, $PL(d)$ is the propagation loss for distance d between the transmitter and receiver, L is the number of fingers in the RAKE receiver, $c_{rake,i}$ is the configuration signal for i^{th} RAKE finger and h_i is the channel coefficient for the i^{th} path.

4 Application to Indoor Office Channels

In this section, we employ the proposed reconfigurable multimedia system in an indoor office environment. In section IV(A), we present simulation setup followed by simulation results in section IV(B).

4.1 Simulation Set-up

The proposed receiver is employed in an indoor office environment. The propagation models for indoor office channels are obtained from the IMT-2000 evaluation methodology [7]. In these models, the propagation effects are divided into two distinct types: (1) mean path loss to model distance and (2) channel loss to model multipath effects. We assume that distance d can vary from $10m$ to $100m$. Channel models A (low delay spread) and B (medium delay spread) obtained from [7] are employed in the simulations.

We assume that we are transmitting a database of images with 176 × 144 pixels per frame in *quarter common intermediate format (QCIF)* (obtained from `ftp://sotka.cs.tut.fi/cost/Ossi/sequences/`). We also fix the total rate R_o to 2 *bits per pixel* (*bpp*), and the desired peak-signal-to-noise ratio to be $35 - 40dB$. Some other system parameters are given in Table 1.

Rates	Frame rate	10 $frames/sec$ (176 × 144 pixels per frame
	Bit rate	760.32 $kbits/sec$ (BPSK)
	Chip rate	12.16 $Mchips/sec$ (length 16 spreading sequences)
Power Amplifier	$P_{t,max} = 10\ mW$, $\eta_{max} = 50\%$	
Rake receiver and Channel Codec	0.18μ, $2.5V$ CMOS Technology	
Low-noise amplifier	Noise figure=5 dB,B.W.=12.16 MHz	
Constraints	$\mathcal{D}_o$	35 dB (in terms of $PSNR$)
	R_o	2 *bits per pixel* (*bpp*)

Table 1: System Parameters.

4.2 Simulation Results

The proposed receiver is tested for distances ranging from $2m$ to $100m$, multipath channels A and B and QCIF images "*akiyo*", "*carphone*", "*claire*", "*coastguard*", "*container*", "*hall_objects*", "*mother_and_daughter*" and "*silent*". The energy consumption of the system in the optimum configuration is shown in Figure 5(a). The total energy varies by more than a factor of 8 from $2m$ to $100m$. The variation of the total energy across images is more significant at longer distances than at shorter distances. Since a fixed system would operate at the maximum energy, the benefits of optimization over distance are clear.

The fraction of energy consumption in each component of the transmission system is shown in Figure 5(b). At short distances, the RAKE receiver and

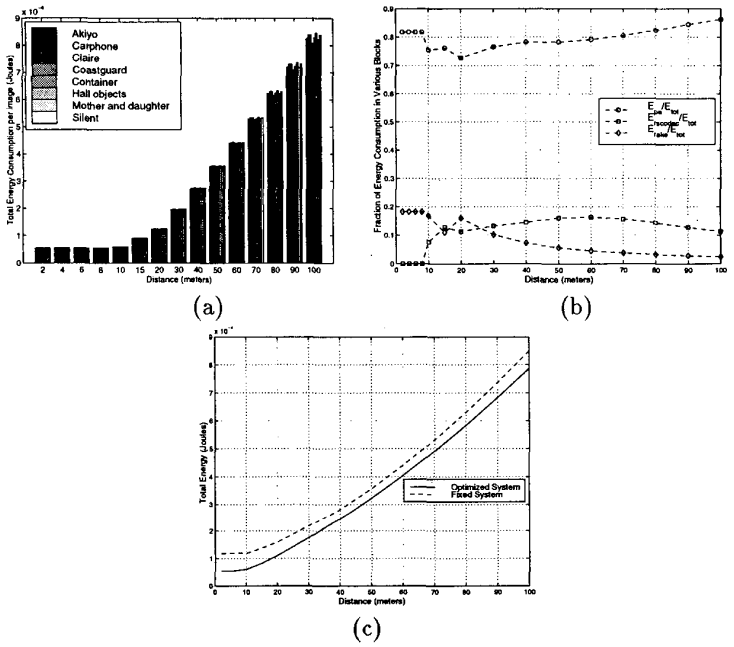

Figure 5: Simulation results: (a) total energy consumed in the optimized system, (b) fraction of energy consumed in each component and (c) comparison with transmit-power-controlled systems.

transmit power are the most significant since the BERs at this distance are relatively low so as to not require additional channel coding. At a distance of $20m$, the fraction of digital energy reaches a peak of 29%, where the RS coder is able to lower BERs by introducing channel coding. At distances over $20m$, the fraction of digital energy decreases since more transmit energy is required to compensate for path loss.

Energy savings (defined as $\mathcal{E}_{sav} = (\mathcal{E}_{worst} - \mathcal{E})/\mathcal{E}_{worst}$) with respect to a system designed for the worst-case state can also be evaluated. The worst case corresponds to distance of $100m$ and image "*carphone*" in Figure 5(a). The energy savings relative to this fixed worst case design range from 0% to 93% for the scenarios shown in Figure 5(a). If we assume that all scenarios are equally probable, then the average energy savings is 59%.

Given that a feedback channel exists for the image transmission system, a system that employs power control to account for the variation of transmit power over distance but does not account for the variation in the digital block parameters can also save energy. Figures 5(c) shows a comparison of total energy consumed by the optimized system and the transmit-power-controlled system averaged over both channels and all images. It can be seen that the proposed system consumes less energy than the transmit-power-controlled system. The average energy savings with respect to the transmit-power-controlled

system are 15.6%.

Therefore, we conclude that the proposed reconfigurable multimedia system is a viable low-power option for the transmission of images over the indoor wireless channels. The energy consumption of digital blocks was found to be less than one-third of the total energy consumption. This is mainly due to the threshold effect experienced by the Reed-Solomon based channel coders in low SNR regions. The convolutional channel coders however have a graceful degradation with the channel SNR, and is a good alternative for the future work. Reconfigurable architectures for source coders is also a topic of future research. Finally, the approach in this paper can be made part of a design methodology for multimedia ASRICs.

5 Acknowledgments

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