NOISE-TOLERANT DYNAMIC CIRCUIT DESIGN *

Lei Wang and Naresh R. Shanbhag
Coordinated Science Laboratory / ECE Department
University of Illinois at Urbana-Champaign
1308 West Main Street, Urbana, IL 61801
E-mail: [leiwang, shanbhag]@uivlsi.csl.uiuc.edu

Abstract – **Noise in deep submicron technology combined with the move towards dynamic circuit techniques for higher performance have raised concerns about reliability and energy-efficiency of VLSI systems in the deep submicron era. To address this problem, a new noise-tolerant dynamic circuit technique is presented. In addition, the average noise threshold energy (*ANTE*) and the energy normalized *ANTE* metrics are proposed for quantifying the noise immunity and energy-efficiency, respectively, of circuit techniques. Simulation results in 0.35 micron CMOS for NAND gate designs indicate that the proposed technique improves the *ANTE* and energy normalized *ANTE* by 2.54X and 2.25X over the conventional domino circuit. The improvement in energy normalized *ANTE* is 1.22X higher than the existing noise-tolerance techniques. A full adder design based on the proposed technique improves the *ANTE* and energy normalized *ANTE* by 3.7X and 1.95X over the conventional dynamic circuit. In comparison, the static circuit improves *ANTE* by 2.2X but degrades the energy normalized *ANTE* by 11%. In addition, the proposed technique has a smaller area overhead (69%) as compared to the static circuit whose area overhead is 98%.**

1. INTRODUCTION

Deep submicron noise has emerged as a critical issue that limits the reliability and integrity of high performance ICs [4] [5] [6] [11] [12]. Static circuits are deemed robust to noise. However, their inherent drawbacks, such as slow speed and high power consumption, have forced IC designers to consider dynamic techniques in the next generation of high performance VLSI systems. While it is well known that dynamic circuits are faster and consume less power, they are inherently susceptible to noise. As mentioned earlier, this limits the applicability of dynamic circuits in the deep submicron era. Thus, effective noise-tolerance techniques are needed.

In this paper, we present a noise-tolerant dynamic circuit technique that has better performance in terms of noise immunity, energy efficiency, speed, and area, as compared to the existing techniques [7] [8]. In addition, we propose a metric referred to as average noise threshold energy (*ANTE*) to quantify the noise immunity of different techniques. The proposed technique is employed to design a high-speed full adder in 0.35μm CMOS. Simulation results are presented to demonstrate the merits of the proposed technique.

In section 2, we discuss deep submicron noise sources and their impact on the performance of dynamic circuits. Existing noise-tolerance techniques [7] [8] for dynamic circuits are introduced, and the proposed technique is presented. The concept of average noise threshold energy (*ANTE*) is also developed in this section. Simulation results on the performance of noise-tolerance techniques, as well as static and conventional dynamic circuits are presented and evaluated in section 3.

* This work was supported by DARPA contract DABT63-97-C-0025 and NSF CAREER award MIP-9623737.

2. NOISE-TOLERANT DYNAMIC CIRCUIT DESIGN

In this section, we discuss deep submicron noise sources and their impact on the performance of dynamic circuits. Existing noise-tolerance techniques for dynamic circuits are introduced, and the proposed technique is presented. We also develop the average noise threshold energy (*ANTE*) as a metric to evaluate noise immunity.

2.1. Deep Submicron Noise

Noise in VLSI circuits is defined as any disturbance that drives node voltages away from a nominal value. The deviated voltage value may or may not cause logic failure. Noise sources that have substantial impact on the performance of digital circuits include ground bounce, crosstalk, charge sharing, process variations, charge leakage, alpha particles, electro-magnetic radiation, etc. [1] [3].

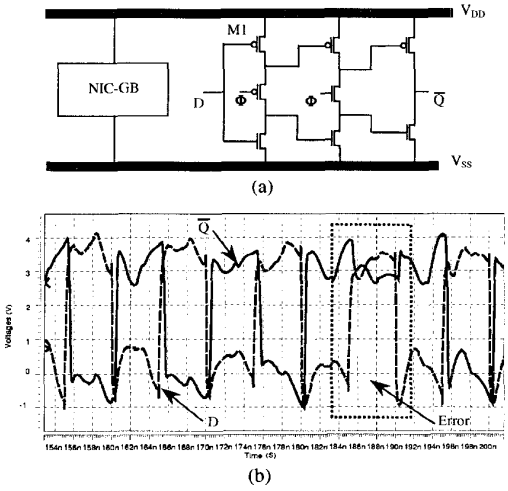

Fig. 1. Noise impact on dynamic D-latch:
(a) Circuit schematic, and (b) Input-output waveform.

Considering the circuit in Fig. 1(a), a noise injection circuit (NIC-GB) injects ground bounce noise into the supply V_{DD} and ground V_{SS} of a dynamic D-latch. The circuit is designed in 0.35μm CMOS technology and simulated via HSPICE at $5ns$ clock period with a load capacitor of $20fF$. The input and output waveforms are shown in Fig. 1(b). As indicated in the waveforms, one logic error occurs during the simulation. This is because ground bounce noise on V_{DD} turns on transistor M1, which should otherwise be off when D = "1" and Φ = "0". Although the above experiment only demonstrates the impact of ground bounce noise, more

comprehensive experiments have shown the composite influence of several noise sources [1].

In particular, noise pulses must have sufficiently high amplitude and long duration to cause unrecoverable logic errors in dynamic circuits. We employ this fact in developing the concept of average noise threshold energy (*ANTE*) in section 2.4.

2.2. Existing Noise-Tolerance Techniques

One effective way to improve noise immunity is to increase the switching threshold voltage V_{th} of the gate, where V_{th} is defined as the input voltage at which the output changes state. For example, a domino NAND gate (see Fig. 2(a)) has $V_{th} = V_{tn}$, where V_{tn} is the threshold voltage of NMOS. Increasing V_{th}, on the other hand, inevitably sacrifices circuit performance such as speed and power consumption, which are the most attractive aspects of dynamic circuits. Thus, any applicable noise-tolerance technique should provide substantial improvement in noise immunity with minimal performance penalty.

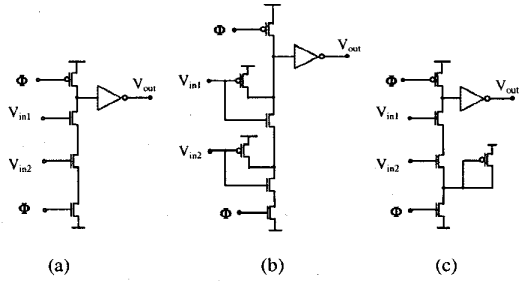

Fig. 2. Dynamic NAND gate:
(a) Domino, (b) CMOS inverter tech., and (c) PMOS pull-up tech.

Several techniques have been developed so far to improve noise immunity of dynamic circuits. The first technique referred to as the *CMOS inverter technique* [7] (see Fig. 2(b)) modifies the NMOS evaluation net by utilizing static inverters for noisy signal inputs. Clearly, V_{th} of the NAND gate equals to V_{th} of the static inverter, which can be adjusted by tuning the transistor width to length ratios. The noise immunity will be enhanced if V_{th} is increased above V_{tn}. The CMOS inverter technique can be applied in the design of noise-tolerant CMOS receivers, dynamic AND/NAND gates, dynamic multiplexing circuits, and dynamic differential input circuits. However, it cannot be used for dynamic OR/NOR logic design since certain input logic combinations will short V_{DD} to ground.

The second technique referred to as the *PMOS pull-up technique* [8] (see Fig. 2(c)) is intended to reduce the charge leakage noise. This technique utilizes a pull-up device, either a voltage source or a MOS transistor, to provide biased voltage in dynamic evaluation net. This increases V_{th} during the evaluation phase. Although this technique is easy to implement, it suffers from large static power dissipation. Therefore, it is not suitable for low-power applications.

2.3. Noise-Tolerant Dynamic Circuit Design

In the following, we present a new noise-tolerance technique referred to as the *mirror technique*. As shown in Fig. 3, the proposed noise-tolerant dynamic circuit requires two identical NMOS evaluation nets. One additional NMOS transistor M3, whose gate voltage is controlled by output signal, provides a conduction path between the common node of evaluation nets and V_{DD}. This technique employs the principle of a Schmitt trigger [9] [10], which can be explained as follows: during the precharge phase, the clock signal Φ turns M1 on, and output voltage V_{out} is charged to logic high. Assuming that the common node voltage V_x is initially discharged, then V_x reaches the value V_{DD}-V_{tn}. Due to body-effect, the switching threshold voltage of the top NMOS net is increased, thereby increasing the noise immunity.

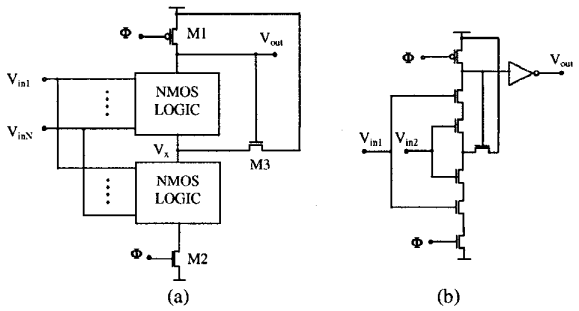

Fig. 3. Proposed noise-tolerant dynamic circuit technique:
(a) General schematic, and (b) NAND gate schematic.

It must be mentioned that the serial arrangement of two evaluation nets in the proposed technique guarantees zero static power dissipation. Note, however, that there can be a speed penalty if the devices are not resized.

2.4. Average Noise Threshold Energy (*ANTE*)

In this paper, we apply noise immunity curve (denoted by C_{nic}) proposed in [13] to measure the noise-tolerance performance. Fig. 4 shows two typical noise immunity curves. As mentioned earlier, for an error to occur, noise pulse must have sufficiently high amplitude and long duration. Every point on the noise immunity curve represents such noise pulse and all points above the curve represent noise pulses that will cause an error. Evidently, a circuit whose noise immunity curve is given by C_{nic1} has better noise immunity than the one with C_{nic2} as its noise immunity curve.

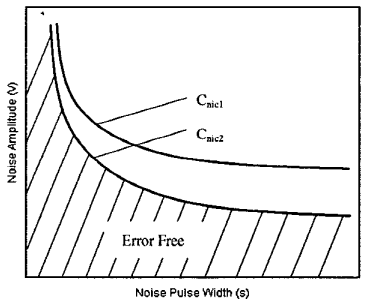

Fig. 4. Noise immunity curve.

To get a numerical value of noise immunity, we propose the metric of *average noise threshold energy* (*ANTE*), which is defined as the average input noise energy that the circuit can tolerate. Since each point on noise immunity curve C_{nic} represents an amplitude V_{noise} and width T_{noise} of the input noise pulse that causes logic errors, and assuming the noise energy is equal to the energy dissipated in an 1Ω resistor, the corresponding *ANTE* measure is obtained as:

$$ANTE = E(V_{noise}^2 T_{noise}) \quad (2.1)$$

where $E(\ )$ denotes the expectation operator.

Noise-tolerance techniques provide improved noise immunity at the expense of area, speed, and power. While noise immunity curves, such as those in Fig. 4, and *ANTE* measure provide comparisons of noise immunity, they don't indicate the energy penalty for achieving such improvement. Hence, another metric, *energy normalized ANTE*, is defined as follows:

$$Energy\ \ Normalized\ \ ANTE = \frac{ANTE}{\varepsilon} \qquad (2.2)$$

where ε represents the energy dissipated per cycle. Thus, the energy normalized *ANTE* provides a measure of the energy penalty incurred in improving noise immunity.

3. SIMULATION RESULTS AND COMPARISONS

In this section, performance of the proposed mirror noise-tolerance technique is investigated. In particular, the proposed technique is employed in the design of a high-speed full adder. Simulation results of the existing noise-tolerance techniques as well as static and conventional dynamic implementations are provided for comparisons. The merits of the proposed technique are also discussed.

3.1. Simulation results for a NAND gate

Fig. 3(b) shows the NAND gate implemented by the proposed noise-tolerance technique, while those using CMOS inverter technique and PMOS pull-up technique are shown in Fig. 2(b) and Fig. 2(c), respectively. We choose the NAND gate for comparisons because CMOS inverter technique cannot be employed for NOR-based circuits.

The noise-tolerant circuits in Fig. 2(b), Fig. 2(c) and Fig. 3(b) were designed to meet the following specifications:

(1) Power supply: $3.3V$
(2) Load capacitor: $20fF$
(3) Clock cycle: $1GHz$
(4) DC noise immunity: ~ $1.8V$

where the DC noise immunity is defined as the maximum amplitude of the input noise pulse with infinitely long duration that will cause a logic error. The conventional dynamic circuit in Fig. 2(a) was designed to meet the specifications (1) - (3).

Fig. 5 and Table 1 show the simulation results of different NAND gate implementations. As predicted, noise-tolerance techniques improve noise immunity at the expense of more power consumption and larger silicon area. As shown in Table 1, the proposed technique improves the *ANTE* and energy normalized *ANTE* by 2.54X and 2.25X over the conventional domino circuit. The improvement in energy normalized *ANTE* is 1.22X higher than the existing noise-tolerance techniques. In addition, the proposed technique has a smaller area overhead (85%) as compared to PMOS pull-up technique whose area overhead is 107%. It must be mentioned that the noise immunity (in terms of *ANTE* and energy normalized *ANTE*) and performance loss (in terms of area and power) of the proposed technique and CMOS inverter technique are similar. However, CMOS inverter technique cannot be used for dynamic OR/NOR logic design. Another result from the simulation is that PMOS pull-up technique degrades the energy normalized *ANTE* by 34%. This is expected because of its large static power dissipation.

3.2. Simulation results for a full adder

Here we present noise-tolerant full adder design employing the proposed mirror technique. Performance of the full adders designed by the proposed technique and two alternative implementations by static logic and conventional dynamic logic (refer to Fig. 7) are provided for evaluation. All of the designs are optimized to satisfy the following specifications:

(1) Power supply: $3.3V$
(2) Load capacitor: $20fF$
(3) Clock cycle: $1GHz$

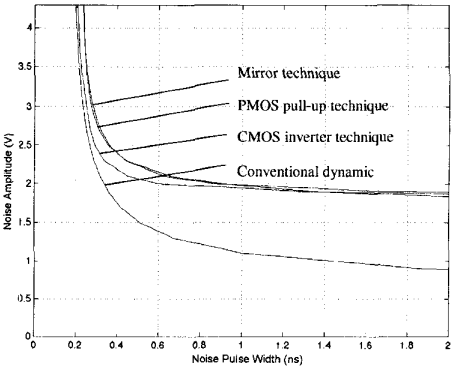

Fig. 5. Noise immunity curves of NAND gate implementations.

Table 1. Performance of NAND gate implementations.

	Area (μm^2)	Energy (pJ)	*ANTE* (nJ)	Energy Normalized *ANTE*
Mirror tech.	86.5	0.856	3.196	4817
PMOS pull-up tech.	96.8	2.250	3.173	1411
CMOS inverter tech.	82.3	0.865	2.898	3350
Conventional dynamic	46.7	0.585	1.255	2145

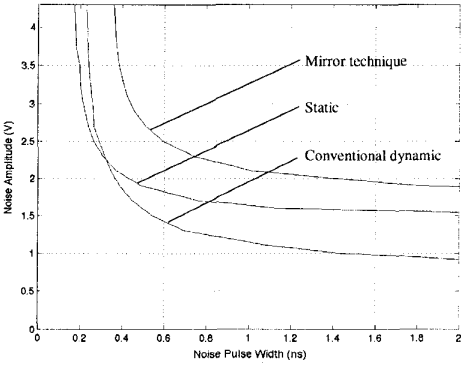

Fig. 6. Noise immunity curves of full adder implementations.

Table 2. Performance of full adder implementations.

	Area (μm^2)	Energy (pJ)	*ANTE* (nJ)	Energy normalized *ANTE*
Static	574.3	2.202	3.115	1414
Conventional dynamic	288.8	0.889	1.405	1580
Mirror tech.	487.2	1.693	5.203	3073

Noise immunity curves in Fig. 6 indicate that the proposed technique has better noise immunity than conventional dynamic circuit and static circuit. Table 2 also indicates that the proposed technique improves the *ANTE* and energy normalized *ANTE* by 3.7X and 1.95X over the conventional dynamic circuit. In

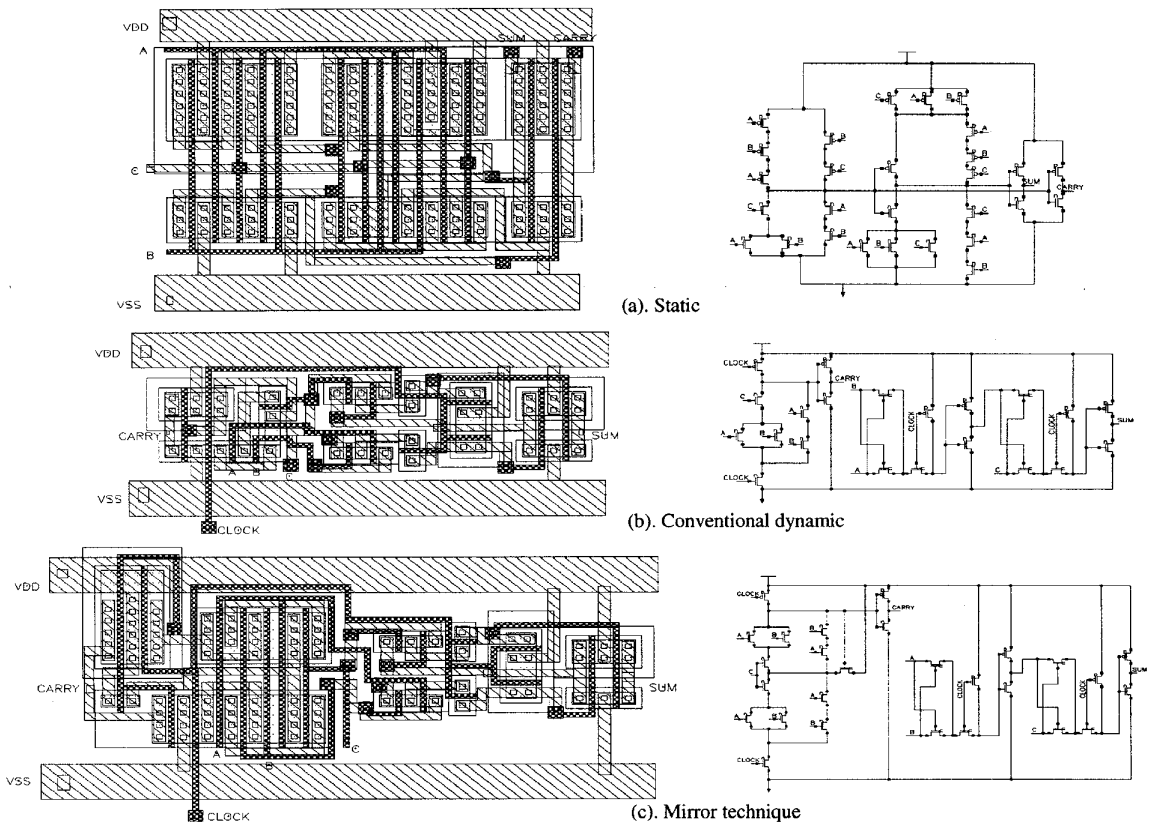

Fig. 7. Layout and schematic of full adder implementations.

comparison, the static circuit improves *ANTE* by 2.2X but degrades the energy normalized *ANTE* by 11%. In addition, the proposed technique has a smaller area overhead (69%) as compared to the static circuit whose area overhead is 98%.

4. CONCLUSIONS

The proposed noise-tolerant dynamic circuit technique can significantly improve the noise immunity with a performance loss (in terms of area and power) that is much less than the existing noise-tolerance techniques and static technique.

Further work is being directed towards minimizing the complexity of the proposed technique. For example, this can be done by utilizing the input signal probability to simplify the mirror NMOS net. Smaller silicon area and less power consumption can be expected for the improved version.

REFERENCES

[1] K. L. Shepard and V. Narayanan, "Noise in deep submicron digital design", *ICCAD96*, pp.524-531, 1996.

[2] N. R. Shanbhag, "A mathematical basis for power-reduction in digital VLSI systems", *IEEE Trans. on Circuits and Systems, Part II,* Vol.44, No.11, pp.935-951, Nov. 1997

[3] P. Larsson and C. Svensson, "Noise in digital dynamic CMOS circuits", *IEEE Journal of Solid-State Circuits*, Vol.29, No.6, pp.655-662, Jun. 1994.

[4] H. H. Chen and D. D. Ling, "Power supply noise analysis methodology for deep-submicron VLSI chip design", *1997 Design Automation Conference*, pp.638-643, 1997.

[5] D. Takashima *et al.*, "Noise suppression scheme for gigabit-scale and gigabytes data-rate LSI's", *IEEE Journal of Solid-State Circuits*, Vol.33 No.2, pp.260-267, Feb. 1998.

[6] A. Devgan, "Efficient coupled noise estimation for on-chip interconnects", *ICCAD97*, pp.147-151, 1997

[7] J. J. Covino, "Dynamic CMOS circuits with noise immunity", US Patent 5650733, 1997.

[8] G. P. D'Souza, "Dynamic logic circuit with reduced charge leakage", US Patent 5483181, 1996.

[9] S. M. Kang and Y. Leblebici, *CMOS Digital Integrated Circuits: Analysis and Design*, McGraw-Hill, 1996.

[10] J. M. Rabaey, *Digital Integrated Circuits: A Design Perspective*, Prentice Hall, 1996.

[11] E. T. Lewis, "An analysis of interconnect line capacitance and coupling for VLSI circuits", *Solid-State Electron.*, Vol.27, pp.741-749, 1984.

[12] D. W. Dobberpuhl *et al.*, "A 200-MHz 64-b dual-issue CMOS microprocessor", *IEEE Journal of Solid-State Circuits*, Vol.27, No.11, pp.1555-1566, Nov. 1992.

[13] G. A. Katopis, "Delta-I noise specification for a high-performance computing machine", *Proceedings of the IEEE*, Vol.73, No.9, pp.1405-1415, Sept. 1985.

[14] The 1997 National Semiconductor Technology Roadmap, *URL: http://www.sematech.org.*