Adaptive Error-Cancellation for Low-Power Digital Filtering

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Abstract

This paper presents a low-power digital filtering technique derived via algorithmic noise-tolerance (ANT). The proposed technique achieves substantial energy savings via voltage overscaling (VOS), where the supply voltage is scaled beyond the minimum (referred to as $V_{dd-crit}$) necessary for correct operation. The resulting performance degradation is compensated for via an adaptive error-cancellation (AEC) algorithm. In particular, we employ an energy optimum AEC to optimize the energy-performance trade-off and reduce the overhead due to ANT. It is shown that the proposed AEC technique is well-suited for designing low-power broadband signal processing and communication systems. Up to 71% energy savings over optimally voltage-scaled conventional systems can be obtained in the context of frequency-division multiplexed (FDM) communications without incurring any performance loss.

1. Introduction

Power dissipation has become a critical VLSI concern for portable and wireless systems with increasingly higher computational capacity. Supply voltage scaling [1] is effective in energy reduction due to the resulting linear reduction in static power dissipation and quadratic reduction in dynamic power dissipation. However, scaling the supply voltage increases the propagation delay. Therefore, the achievable energy reduction of general VLSI as well as DSP-specific systems is bounded by the minimum voltage (referred to as $V_{dd-crit}$) where the throughput requirement is just met. Overscaling supply voltage (VOS) below the $V_{dd-crit}$ induces input-dependent soft errors if the critical delay paths and other longer paths are excited. This results in a performance degradation which necessitates *algorithmic noise-tolerance* (ANT) techniques for correct operation.

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Past work [2] has reported a prediction-based ANT technique which achieves substantial energy savings over conventional DSP systems while being subject to a marginal performance loss. The prediction-based ANT is suitable for DSP architectures with a path delay distribution and input statistics such that soft errors due to VOS are of large magnitude and occur infrequently. This condition is easily met for narrowband filters implemented via delay-imbalanced arithmetic units. We also proposed an *adaptive error-cancellation* (AEC) technique [3] that can tolerate higher error frequencies that could be due to excessive VOS and uncorrelated input signals. Up to 40% energy reduction was obtained in [3] for narrowband filters without performance loss. In this paper, we derive the design of energy-optimum AEC-based soft filters and determine the energy-performance trade-off. Simulation results demonstrate that an energy-optimum AEC achieves 43% – 71% energy savings over conventional DSP systems in the context of frequency-division multiplexed (FDM) communications without incurring any performance loss.

In section 2, we review our past work in using AEC for ANT. In section 3, we derive the energy-optimum AEC by using the *Lagrange multiplier* method [4]. Simulation results are presented and evaluated in section 4.

2. Algorithmic Noise-Tolerance (ANT) for Low-Power DSP

In this section, we present the VOS and ANT concepts and describe the proposed AEC technique for designing low-power DSP systems.

2.1. Energy savings via VOS

Dedicated DSP systems are designed subject to an application specific throughput requirement, i.e.,

$$T_{cp} \le T_s, \tag{1}$$

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where T_s is the sample period determined by the application and T_{cp} is the critical path delay of the corresponding DSP architecture. Supply voltage scaling reduces the energy dissipation but on the other hand increases the propagation delay of the underlying arithmetic units. Thus, present-day energy reduction via voltage scaling is limited by a minimum supply voltage $V_{dd-crit}$ at which the condition $T_{cp} = T_s$ is met. Voltage overscaling (VOS) refers to the reduction of the supply voltage to $V_{dd-sub} = V_{dd-crit}/k_v$, where $k_v > 1$ is the voltage overscaling factor (VOSF). This leads to additional energy savings but results in output errors if critical delay paths and other longer paths are excited by certain input patterns. We denote these output errors as *soft errors*.

We note that soft errors appear first in the MSBs, as most arithmetic units employed in practice use LSB-first computation. This creates errors of large magnitude thereby requiring ANT techniques for error control. The overall approach of employing VOS in combination with ANT for low-power is referred to as *soft DSP*.

2.2. Adaptive error-cancellation (AEC)

Soft errors due to VOS are input-dependent and hence can be cancelled by using the proposed AEC technique as shown in Fig. 1. This technique is akin to *echo cancellation* schemes employed in voiceband modems.

In the presence of soft errors due to VOS, the output $y_{vos}[n]$ of an N-tap VOS filter $H(z)$ can be expressed as

$$\begin{aligned} y_{vos}[n] &= \sum_{k=0}^{N-1} h_k x[n-k] + e_s[n] \\ &= y[n] + e_s[n] \\ &= s[n] + \eta[n] + e_s[n], \end{aligned} \quad (2)$$

where $y[n]$ is the error-free output composed of a desired signal $s[n]$ and signal noise $\eta[n]$, $e_s[n]$ denotes the soft output error, h_k is the k^{th}-tap coefficient, and $x[n-k]$ is the k^{th} delayed input sample.

Since soft error $e_s[n]$ in the current output is determined by input samples $x[n], x[n-1], \cdots, x[n-N+1]$, we can use these data samples to generate a statistical replica of $e_s[n]$, denoted by $\widehat{e}_s[n]$, and then subtract it from the output. The resulting output $y_o[n]$ is given by

$$y_o[n] = y[n] + e_s[n] - \widehat{e}_s[n]. \quad (3)$$

For effective error-control, an ANT technique needs to make $\widehat{e}_s[n] \approx e_s[n]$ and thus $y_o[n] \approx y[n]$. This can be achieved by using the popular *least mean square* (LMS) al-

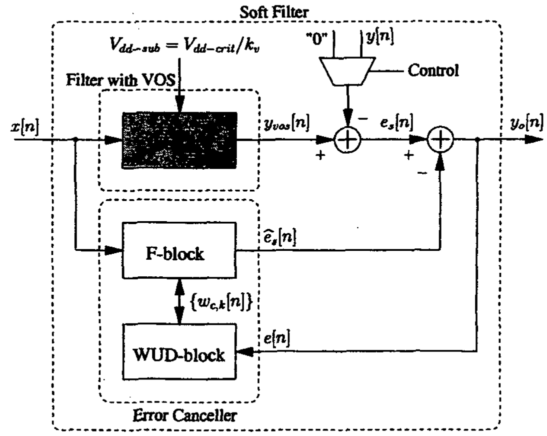

Figure 1: The proposed ANT technique based on adaptive error-cancellation.

gorithm, as given below [5]

$$\widehat{e}_s[n] = \sum_{k=0}^{N-1} w_{c,k}[n-1]x[n-k], \quad (4)$$

$$e[n] = e_s[n] - \widehat{e}_s[n], \quad (5)$$

$$w_{c,k}[n] = w_{c,k}[n-1] + \mu e[n]^* x[n-k], \quad (6)$$

where $\underline{\mathbf{w}} = \{w_{c,0}[n], w_{c,1}[n], \cdots, w_{c,N-1}[n]\}$ is the tap-weight vector of the error canceller $H_c(z)$, $e[n]$ is the residual soft error after cancellation by the AEC, and μ is the step-size. The computations in (4) are done in the filter (F) block of the AEC and those in (6) are executed in the weight-update (WUD) block.

Note that the LMS algorithm (4)–(6) can be employed to autocalibrate a soft DSP integrated circuit in the field so as to be able to account for non-stationary variations in the process, temperature, input signal and other deep submicron (DSM) effects.

3. Energy-Optimum AEC-based ANT

The above AEC in section 2.2 employs an error canceller $H_c(z)$ having the same order as that of the primary filter $H(z)$, thereby involving a large energy overhead which may defeat the original goal of energy reduction. In this section, we derive a low-complexity AEC via energy optimization subject to a performance constraint.

3.1. Performance metrics

The output *SNR* of a VOS filter employing the AEC for ANT is termed as SNR_{ANT}, which is given by

$$SNR_{ANT} = 10\log_{10}\left(\frac{{\sigma_s}^2}{{\sigma_n}^2 + {\sigma_e}^2}\right), \quad (7)$$

where ${\sigma_s}^2$, ${\sigma_n}^2$ and ${\sigma_e}^2$ are the variances of the desired signal $s[n]$, signal noise $\eta[n]$ and the residual soft error $e[n]$ (or estimation error, see (5)), respectively.

In practice, AEC-based soft filters are designed for an application-specific performance requirement SNR_{design}, such as

$$SNR_{ANT} \geq SNR_{design} = \left(\frac{{\sigma_s}^2}{\sigma^2_{n,design}}\right), \quad (8)$$

where $\sigma^2_{n,design}$ denotes the variance of the worst-case signal noise at filter output.

The average energy savings $\mathcal{E}_{sav}$ achieved by an AEC-based soft filter is defined as

$$\mathcal{E}_{sav} = \left(1 - \frac{\mathcal{E}_{soft}}{\mathcal{E}_{conv}}\right) \times 100\%, \quad (9)$$

where $\mathcal{E}_{conv}$ is the energy dissipation of the conventional filter at an optimally scaled voltage of $V_{dd-crit}$ and $\mathcal{E}_{soft}$ is the energy dissipation of the soft filter at an overscaled voltage of V_{dd-sub}. It can be seen from Fig. 1 that $\mathcal{E}_{soft}$ has two components

$$\mathcal{E}_{soft} = \mathcal{E}_H + \mathcal{E}_{AEC}, \quad (10)$$

where $\mathcal{E}_H$ is the energy dissipation of the primary filter $H(z)$ and $\mathcal{E}_{AEC}$ is the energy overhead due to the error canceller $H_c(z)$.

The energy-optimum AEC can be formulated as an energy optimization problem subject to a performance constraint, as given below

$$\begin{aligned} &\textit{minimize:} && \mathcal{E}_{soft}, \\ &\textit{subject to:} && SNR_{ANT} \geq SNR_{design}. \end{aligned} \quad (11)$$

3.2. Energy-optimum AEC

The optimization problem (11) is composed of three interconnected problems: *1.) How to choose the primary filter $H(z)$? 2.) What is the optimum value of VOSF? and 3.) How to find the energy-optimum AEC for a given $H(z)$ and VOSF?* The first problem involves finding an optimum ratio of ${\sigma_n}^2$ and ${\sigma_e}^2$ (see (7)), as a larger ${\sigma_n}^2$ relaxes the design of $H(z)$ (smaller $\mathcal{E}_H$) but requires a more complex AEC (larger $\mathcal{E}_{AEC}$). Similarly, for the second problem, a larger VOSF leads to more energy savings in $H(z)$ (smaller $\mathcal{E}_H$) but also induces a larger performance degradation and thus requires a more complex AEC (larger $\mathcal{E}_{AEC}$). In general, these two problems involve a set of nonlinear equations describing the relationship between the algorithmic performance and the corresponding energy properties. In addition, these nonlinear equations also depend on the filter design techniques and datapath architectures being employed. Therefore, numerical methods are practical for the first two problems. On the other hand, we will show later that the third problem can be solved analytically. Thus, the practical approach for solving (11) is to employ the energy-optimum AEC for possible $H(z)$ and VOSF combinations to find the overall energy-optimum. This search procedure can be greatly simplified because we can easily predict the search directions. In fact, it can be shown that the optimum solution to (11) is obtained at the point where $H(z)$ has the "loosest" design (corresponding to the largest possible ${\sigma_n}^2$ and in general the smallest $\mathcal{E}_H$) and VOSF achieves the largest value that makes $SNR_{ANT} = SNR_{design}$. This is because $\mathcal{E}_H$ is much larger than $\mathcal{E}_{AEC}$, thus $\mathcal{E}_{soft}$ is minimized when $\mathcal{E}_H$ is minimized and VOSF is maximized. In what follows, we derive an energy-optimum AEC for any given $H(z)$ and VOSF, i.e., the solution of the third problem. When applying this AEC at the point as mentioned above, we obtain an overall energy-optimum AEC-based soft filter as the solution to (11).

The reason for the existence of energy-optimum AEC is that performance degradation due to VOS is dominated by soft errors from a few of the taps of $H(z)$ having large coefficients. Thus, a reduced-order AEC exists that can restore the algorithmic performance. We define a vector $\underline{\mathbf{b}} = \{b_0, b_1, \cdots, b_{N-1}\} \in \mathcal{B}^N$, where N is the order of the primary filter $H(z)$ and $\mathcal{B}^N$ is an N-dimension vector space with binary elements b_j's $\in \{0,1\}$. We let $b_j = 1$ if the j^{th} tap of error canceller $H_c(z)$ is powered up and $b_j = 0$ otherwise. The length N_c of error canceller $H_c(z)$ can be written as

$$N_c = \sum_{j=0}^{N-1} b_j. \quad (12)$$

Assume that the input signal $x[n]$ is a zero-mean and uncorrelated random sequence. The variance of residual soft error $e[n]$ after cancellation by the AEC can be expressed as

$${\sigma_e}^2 = {\sigma_{es}}^2 - \sum_{j=0}^{N-1} b_j {w_j}^2 {\sigma_x}^2, \quad (13)$$

where ${\sigma_x}^2$ and ${\sigma_{es}}^2$ are the variances of the input signal $x[n]$ and soft output error $e_s[n]$, respectively, for a given $H(z)$ and VOSF, and w_j's are the optimum coefficients of $H_c(z)$, given by [5],

$$w_j = \frac{E\left(x[n-j]e_s[n]\right)}{{\sigma_x}^2}. \quad (14)$$

Note that from (7)−(8), $\sigma_e{}^2$ in (13) due to the N_c-tap AEC has the following constraint

$$\sigma_e{}^2 \leq \sigma^2_{n,design} - \sigma_n{}^2, \tag{15}$$

where $\sigma_n{}^2$ is determined by the given $H(z)$.

To describe the energy overhead $\mathcal{E}_{AEC}$, we assume that the **WUD**-block is switched off after convergence. This implies

$$\mathcal{E}_{AEC}(\underline{\mathbf{b}}) = \sum_{j=0}^{N-1} b_j \mathcal{E}_{F,j}, \tag{16}$$

where $\mathcal{E}_{F,j}$ is the energy dissipation due to the j^{th}-tap computation in the **F**-block. Given the coefficient w_j, $\mathcal{E}_{F,j}$ can be estimated via the *weighted multiplier energy model* [6].

Using the above notations, the energy optimization problem for AEC can be written as

$$\begin{aligned} &\underset{\underline{\mathbf{b}}\in\mathcal{B}^N}{\textit{minimize:}} && \mathcal{E}_{AEC}(\underline{\mathbf{b}}), \\ &\textit{subject to:} && \sigma_e{}^2 \leq \sigma^2_{n,design} - \sigma_n{}^2, \end{aligned} \tag{17}$$

where $\mathcal{E}_{AEC}(\underline{\mathbf{b}})$, $\sigma_e{}^2$, $\sigma_n{}^2$ and $\sigma^2_{n,design}$ are given by (16), (13), (7) and (8), respectively.

Employing the Lagrange multiplier method [4], we obtain the solution $\underline{\mathbf{b}}^* = \{b_0^*, b_1^*, \cdots, b_{N-1}^*\} \in \mathcal{B}^N$ of (17) as

$$b_j^* = \begin{cases} 1 & \text{if } \frac{\mathcal{E}_{F,j}}{w_j{}^2\sigma_x{}^2} < \lambda^*, \\ 0 & \text{if } \frac{\mathcal{E}_{F,j}}{w_j{}^2\sigma_x{}^2} \geq \lambda^*, \end{cases} \tag{18}$$

where λ^* is the solution of *sensitivity vector* of the Lagrange multiplier. This gives the energy-optimum length $N_c^{\mathbf{opt}}$ of the error canceller $H_c(z)$ as

$$N_c^{\mathbf{opt}} = \sum_{j=0}^{N-1} b_j^*. \tag{19}$$

From (18), if the j^{th} tap of $H_c(z)$ has a large coefficient w_j while consuming a relatively small energy $\mathcal{E}_{F,j}$, then $b_j^* = 1$. In other words, the input $x[n-j]$ has to be utilized to cancel the soft output errors. On the other hand, we can switch off the j^{th} tap of $H_c(z)$ if this tap consumes more energy (large $\mathcal{E}_{F,j}$) but has a trivial contribution to the error cancellation (small w_j). In practice, we can start to turn off those taps in $H_c(z)$ with smaller value of $\frac{\mathcal{E}_{F,j}}{w_j{}^2\sigma_x{}^2}$ until the performance constraint is violated. This avoids the computation of λ^*.

We will now describe the relationship between the performance degradation due to VOS and the energy-optimum configuration of the AEC. We denote $e_{s,j}[n]$ as the soft error component from the j^{th} tap of $H(z)$. As $e_{s,j}[n]$ is excited by the input $x[n-j]$, it is reasonable to assume that $e_{s,j}[n]$ is statistically independent from soft error $e_{s,i}[n]$ and input $x[n-i]$ for $i \neq j$. Thus, we can rewrite (14) as

$$\begin{aligned} w_j &= \frac{E\left(x[n-j]\left(\sum_{i=0}^{N-1} e_{s,i}[n]\right)\right)}{\sigma_x{}^2} \\ &= \frac{E\left(x[n-j]e_{s,j}[n]\right)}{\sigma_x{}^2}. \end{aligned} \tag{20}$$

In general, if the j^{th} tap of $H(z)$ has a large coefficient h_j, then critical paths and other longer paths get excited easily, thereby resulting in a larger value for $e_{s,j}[n]$ and thus $E\left(x[n-j]e_{s,j}[n]\right)$. From (20), this results in $H_c(z)$ having a large coefficient w_j which from (18) makes $b_j^* = 1$. This is to be expected as $e_{s,j}[n]$ is induced by $x[n-j]$ and thus can only be cancelled by the j^{th} tap in the AEC. As the filter bandwidth increases, the predominant contribution to the soft error energy at the output will be from fewer taps of $H(z)$. This is because wideband filters have a narrow impulse response. Thus, more b_j^*'s will be zero and a smaller $N_c^{\mathbf{opt}}$ will result. Increasing N_c beyond $N_c^{\mathbf{opt}}$ will not benefit algorithmic performance but instead cause extra energy overhead. In summary, the proposed AEC technique has a smaller hardware complexity, and therefore a better energy-efficiency, when employed for wideband filters.

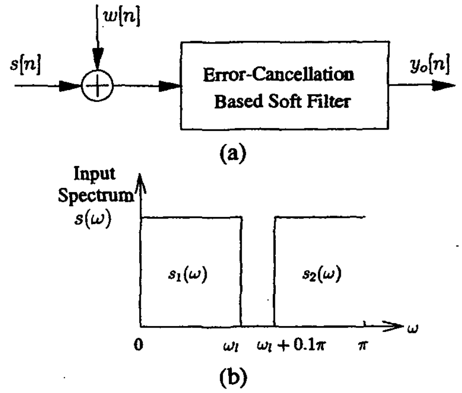

Figure 2: Simulation setup: (a) lowpass filtering via the proposed ANT technique and (b) input signal spectrum.

4. Simulation Results

In these simulations, we employ AEC-based soft filters to perform frequency selective filtering (see Fig. 2(a)). The purpose is to extract the primary signal $s_1[n]$ embedded in a white Gaussian noise $w[n]$ and a bandpass signal $s_2[n]$ in the adjacent band (see Fig. 2(b)). This simulation setup emulates a frequency-division multiplexed (FDM) signal. We assume all the signals $s_1[n]$, $s_2[n]$ and noise $w[n]$ are statistically independent from each other.

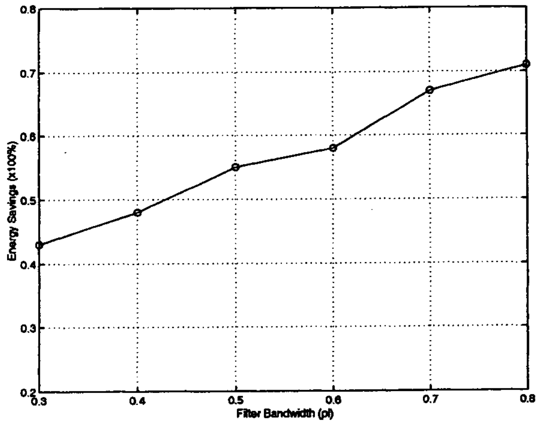

Figure 3: Energy savings due to energy-optimum AEC filters.

Table 1: Design specifications for energy-optimum AEC filters.

BW	$H(z)$			$H_c(z)$		
	N	B_{input}	B_{coeff}	N_c^{opt}	B_F	B_{WUD}
0.3π	32	8b	10b	14	7b	10b
0.4π	32	8b	10b	12	7b	10b
0.5π	32	8b	10b	10	7b	10b
0.6π	32	8b	10b	10	6b	10b
0.7π	32	8b	10b	8	6b	10b
0.8π	32	8b	10b	6	6b	10b

In order to evaluate the energy-performance trade-off for FDM systems with different bandwidths, we change the bandwidth ω_l of signal $s_1[n]$ from 0.3π to 0.7π. All the simulations employ 2's complement carry-save Baugh-Wooley multipliers and ripple-carry tree-style adders. The precisions of F-block and WUD-block are determined by using the method proposed in [7]. A logic level simulation [3] is used to detect delay violations due to VOS and calculate the resulting performance degradation. The energy dissipation is obtained via the gate-level simulation tool MED [8] for a $0.25\mu m$ CMOS technology. The energy overhead due to AEC represents the computations in the F-block, as the WUD-block is switched off after the AEC has converged.

We employ the optimization strategy given in section 3 to design the AEC-based filters for different bandwidths. The SNR_{design} for these simulations is $22dB$ at the output. Table 1 provides the design specifications for the energy-optimum AEC and Fig. 3 plots the results of energy savings in comparison with optimally voltage-scaled conventional filters at the required algorithmic performance. It is shown that the hardware complexity of the energy-optimum AEC decreases with filter bandwidth increasing from 0.3π to 0.8π. This is because wideband filters have a narrow soft-error energy distribution with respect to filter taps. Therefore, fewer filter taps contribute to the performance degradation and this reduces the complexity of AEC algorithm, thereby enabling greater energy reduction. The achievable energy savings ranges from 43% to 71% as filter bandwidths increase from 0.3π to 0.8π. This demonstrates that the proposed AEC technique is well-suited for broadband DSP and communication systems.

5. Conclusions

In this paper, we study the performance of the proposed AEC technique in a wideband signal processing system. In particular, we employ the energy-optimum AEC design derived via the Lagrange multiplier method for low-complexity ANT. It is shown that the resulting AEC achieves significant energy reduction over optimally voltage-scaled conventional systems without incurring performance degradation. Future work is being directed towards the application of the proposed ANT technique to adaptive filters and to practical broadband communication systems, such as Gigabit Ethernet receivers.

6. References

[1] R. Gonzalez, B. M. Gordon, and M. A. Horowitz, "Supply and threshold voltage scaling for low power CMOS," *IEEE J. Solid-State Circuits*, vol. 32, pp. 1210-1216, August 1997.

[2] R. Hegde and N. R. Shanbhag, "Energy-efficient signal processing via algorithmic noise-tolerance," *Proc. of Intl. Symp. on Low-Power Electronics and Design*, pp. 30-35, Aug. 1999.

[3] L. Wang and N. R. Shanbhag, "Low-power signal processing via error-cancellation," *Proc. of IEEE Workshop Signal Process. Syst. (SiPS)*, pp. 553-562, Oct. 2000.

[4] A. L. Peressini, F. E. Sullivan and J. J. Uhl, Jr., *The Mathematics of Nonlinear Programming*, Springer-Verlag, 1988.

[5] S. Haykin, *Adaptive Filter Theory*, Prentice Hall, 1996.

[6] M. Goel and N. R. Shanbhag, "Dynamic algorithm transformations (DAT) - A systemic approach to low-power reconfigurable signal processing," *IEEE Trans. VLSI*, vol. 7, pp. 463-476, Dec. 1999.

[7] M. Goel and N. R. Shanbhag, "Finite-precision analysis of the pipelined strength-reduced adaptive filter," *IEEE Trans. Signal Processing*, vol. 46, pp. 1763 -1769, June 1998.

[8] M. G. Xakellis and F. N. Najm, "Statistical estimation of the switching activity in digital circuits," *Design Automation Conf.*, pp. 728-733, June 1994.