A Noise-Tolerant Dynamic Circuit Design Technique

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Abstract

A new circuit technique, referred to as the twin-transistor technique, for increasing the noise immunity of dynamic logic circuits is presented. This technique makes dynamic logic gates more tolerant to noise appearing at the gate inputs. A multiply-accumulate circuit has been designed and fabricated using a 0.35μm process to verify this technique. Experimental results indicate that the twin-transistor technique provides a significant improvement in the noise immunity of dynamic circuits (>2.4X) with only a modest increase in power dissipation (15%) and no loss in throughput.

I. Introduction

As devices are scaled into the deep sub-micron regime, noise is becoming an increasingly important issue in integrated circuit design [1]. The sources of noise in digial ICs include circuit switching, capacitive/inductive crosstalk and process variations. High-speed techniques at the circuit level such as dynamic logic add additional noise sources, namely charge-sharing and leakage [2] and increase circuit sensitivity to noise. These trends provide the motivation for developing high speed noise-tolerant circuit design techniques [3, 4, 5, 6].

In [3], we showed that the sensitivity of dynamic circuits to crosstalk noise could increase with voltage scaling. We also proposed the *twin-transistor* technique that provides a significant improvement in the immunity of dynamic logic circuits to input noise(e.g., crosstalk). In this paper, we present experimental results derived from measurements of a test IC containing a multiply-accumulate circuit designed using the twin-transistor technique, and fabricated using 0.35μm process technology.

The next section will briefly describe the twin-transistor technique. Section III discusses the design of the pipelined MAC test IC. Experimental results showing the improvement in noise immunity and the penalty in terms of power dissipation are presented in Section IV.

II. Twin-Transistor Technique

A one-transistor domino buffer is shown in Fig. 1(a). The noise threshold of this gate, defined as the minimum input voltage required to cause switching, is approximately the transistor threshold voltage V_t. For reliable operation in the presence of noise (e.g. crosstalk, switching noise), it is desirable to increase this threshold. The twin-transistor technique [3], illustrated in Fig. 1(b), can be used to accomplish this. The additional crosscoupled transistor, $M2$, called the twin-transistor, increases the turn-on voltage of $M1$ by pulling up the voltage of the common source node. Note that $M2$ is ON since the node X has been precharged to V_{dd}. The increased noise threshold is seen from the voltage transfer characteristics shown in Fig. 1(c).

Like all noise-tolerant circuit techniques, the twin-transistor technique achieves additional noise immunity at the expense of energy. It has been shown that the twin-transistor technique is more energy-efficient than existing noise-tolerant dynamic circuit design techniques [3]. The twin-transistors increase circuit capacitance and therefore the delay. The size of the twin-transistors can be used to tradeoff delay against the noise threshold. Fig. 2 shows this tradeoff for a 2-input AND gate. The delay penalty is seen to be about 60ps per unit voltage increase in the noise threshold. The delay can however be maintained by increasing the sizes of the transistors in the principal NMOS pulldown path. For example, to maintain the delay of a 2-input domino AND gate implemented with minimum-size transistors when twin transistors are added, it is sufficient to double the sizes of the

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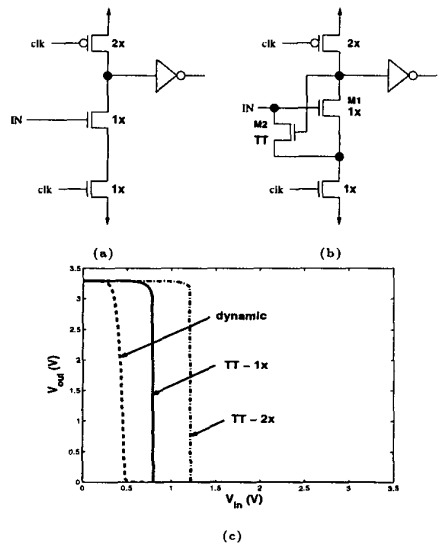

Figure 1: A simple buffer implemented using (a) conventional domino, and (b) twin transistors. The dc transfer characteristics are shown in (c) for the conventional circuit and the twin transistor circuit for two different sizes of $M2$ in multiples of $(W/L)_{min} = (0.6\mu m/0.4\mu m)$.

three transistors in the NMOS pulldown path.

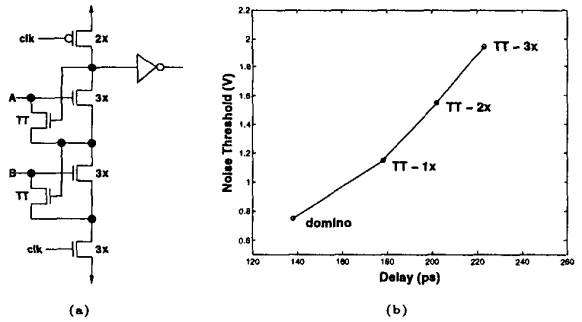

Figure 2: (a)A 2-input AND gate implemented using twin transistors. (b) Simulation results of a 2-input AND gate driving an identical gate, showing that the size of the twin transistors can be used to tradeoff delay against noise immunity.

Twin-transistors also help to mitigate the charge-sharing problem that occurs in dynamic logic circuits. This is fortunate since the use of twin-transistors prevents the use of additional transistors to precharge intermediate nodes [2]. An added benefit of this technique is that the internal nodes are precharged only when the inputs are such that charge-sharing can potentially occur.

III. Test IC Design

A test IC has been designed and fabricated in order to obtain experimentally measured values of the improvement in noise immunity and the increase in power dissipation due to the twin-transistor technique, over conventional dynamic logic.

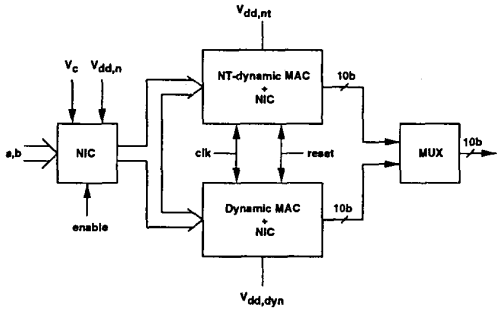

Figure 3: A simplified block diagram schematic of the testchip.

A. MAC

A simplified schematic of the test IC is shown in Fig. 3. Two MACs are built on-chip - one using conventional domino logic (MAC-I), and another using twin-transistors(MAC-II). Both the MACs are pipelined at the bit level and designed to operate at a maximum speed of 500MHz at 3.3V supply. The transistors used in the NMOS pulldown path of all dynamic logic gates in MAC-II are twice as large as their counterparts in MAC-I to offset the effect of twin-transistors on delay. The twin-transistors in MAC-II are all of minimum size. Separate supply pins are used for the two MACs to enable measurement of the additional power dissipation caused by the use of twin-transistors. Inputs V_c and $V_{dd,n}$ control the amount of noise injected by the NIC when it is enabled. The *reset* input disables the accumulator section of the MAC. Inputs and outputs are skewed to accomodate the bit-level pipelining scheme.

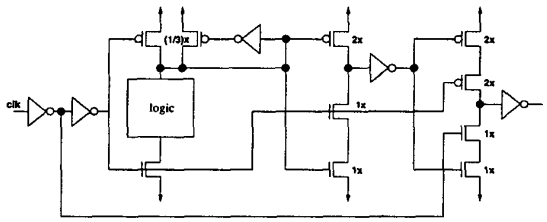

Figure 4: Schematic of a general pipelined logic gate used in the MAC. The 'logic' block is replaced by the appropriate NMOS network (and twin transistors in the noise-tolerant implementation).

The multiplier is a simple array multiplier consisting of AND gates, half and full adders. It is pipelined so that one bit of the product is available at the end of each clock cycle. The general structure of a pipelined logic gate used on this chip is shown in Fig. 4. The part of the schematic labelled 'logic' is replaced with the appropriate NMOS pulldown network (along with twin-transistors in the case of MAC-II). Inverters are inserted wherever necessary to avoid the situation of a dynamic node driving a dynamic gate [7].

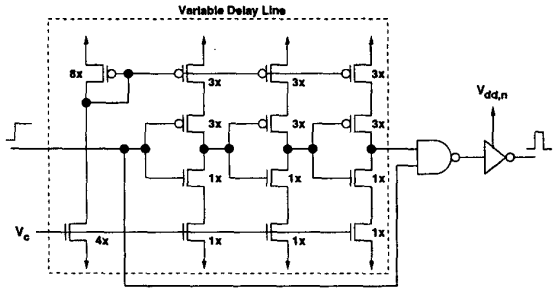

Figure 5: A simplified schematic of the Noise Injection Circuit. Voltages V_c and $V_{dd,n}$ enable the control of the noise duration and amplitude respectively.

B. Noise Injection Circuit

The function of the noise injection circuit (NIC) is to inject a noise pulse of desired amplitude and width into a logic gate. NICs are distributed throughout the chip to inject noise at several points in the logic evaluation path. The basic idea used in the design of the NIC is to produce a glitch at the output of a gate by staggering its inputs in time. The circuit implementation of this idea is illustrated in Fig. 5.

A tunable delay line is used to delay one of the inputs to a dual input gate. The delay and hence the noise pulse duration T_n can be controlled through the voltage V_c. The amplitude of the noise V_n can be controlled through the supply voltage of the final inverter $V_{dd,n}$. Fig. 6 shows a typical noise waveform and the definition of noise amplitude and duration, that is used to quantify noise immunity. Fig. 7 shows the range of noise waveforms that can be generated using this technique. It can be seen that the amount of noise injected into a dynamic gate can be varied over a significant range through the control voltages, V_c and $V_{dd,n}$.

IV. Experimental Results

The test IC was fabricated in 0.35μm technology through MOSIS using the process HPGMOS10QA. A photomicrophotograph of the chip is shown in Fig. 8. The die size is 2mm x 2mm and it integrates about 10k transistors.

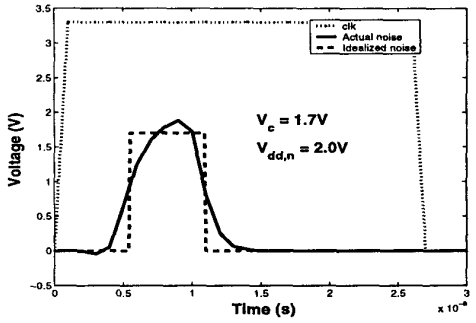

Figure 6: HSPICE simulation results showing a typical noise waveform. The idealized noise waveform is constructed so that its duration equals the time for which the noise voltage exceeds 50% of its peak value. The amplitude is chosen so as to preserve the area under the noise waveform.

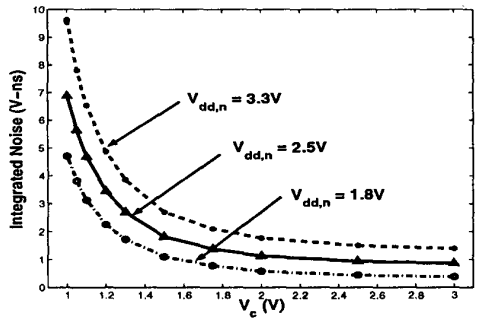

Figure 7: Simulation results showing the dependence of the integral of the noise waveform on V_c and $V_{dd,n}$.

The noise immunity curve of a logic gate is defined as the set of all combinations of noise amplitudes V_n and durations T_n that cause the gate output to switch. Noise immunity curves were obtained experimentally using the tunable noise injection circuit described in the previous section. Measured values of V_c and $V_{dd,n}$ (Fig. 5) that cause an error in the output of the MAC, are mapped to corresponding noise amplitudes and durations using simulation results such as those shown in Fig. 7. The noise immunity curves for the two multiplier implementations derived using this approach are shown in Fig. 9. It can be seen that the twin-transistor technique increases the noise threshold by about 0.65V, over that of conventional dynamic logic. Noise immunity can be quantified using the Average Noise Threshold Energy (ANTE) measure defined in [6]. Briefly, ANTE is given by the equation:

$$ANTE = E({V_n}^2 \cdot T_n), \quad (1)$$

where $E()$ denotes the expectation operator and (V_n, T_n)

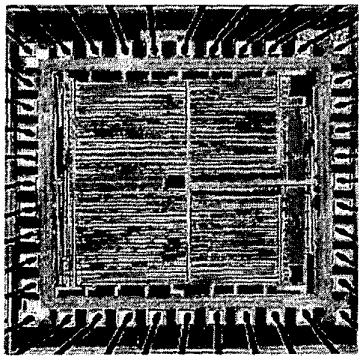

Figure 8: A photomicrograph of the testchip.

are points on the noise immunity curve.

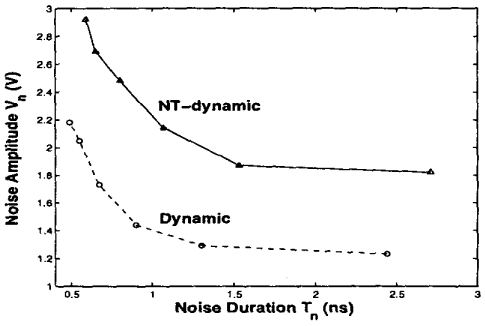

Figure 9: Experimentally measured noise immunity curves of the dynamic and NT-dynamic multiplier. The curves are the average of the results over several input combinations.

From the noise immunity measurement results shown in Table 1, it can be seen that the use of twin-transistors provides an improvement in ANTE that is greater than 2.4X for a 2-input AND gate and the multiplier. This improvement is obtained at the cost of additional power dissipation. Information about power dissipation is summarized in Table 2. Power dissipation values for the AND gate and full adder were obtained from HSPICE simulations while those for the MAC were measured experimentally. The percentage power penalty is smaller in the case of the complete MAC (15%) as compared to a full adder or an AND gate due to the pipelining overhead (latches, buffers, clock tree) that is common to both the dynamic and the noise-tolerant dynamic implementations.

Table 1: Noise Immunity (ANTE) results (measured)

	Conventional	Twin transistor
AND2(V^2-ns)	2.47	6.67
Multiplier(V^2-ns)	2.40	5.65

These results show that the twin-transistor technique provides a significant improvement(2.4X) in the noise immunity of dynamic logic circuits, with only a modest increase in power dissipation (15%).

Table 2: Power dissipation at V_{dd}=3.3V, 100MHz

	Conventional	Twin transistor
AND2 (μW) (simulated)	57	69
Fulladder (μW) (simulated)	191	260
MAC (mW) (measured)	10.3	11.9

V. Conclusions

A new noise-tolerant dynamic circuit technique using twin-transistors has been developed and used in the design of a MAC testchip. The testchip was fabricated using 0.35μm technology and experimental measurements demonstrate the improved noise immunity provided by the twin-transistor technique.

VI. Acknowledgements

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