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Low-Power Decimation Filters for Oversampling ADCs Via The Decorrelating (DECOR) Transform

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Abstract

The area and power consumption of oversampling analog-to-digital converters (ADCs) are governed largely by the associated digital decimation filter. This paper presents a low power, area-efficient digital decimation filter for an oversampling ADC application that employs the decorrelating (DECOR) transform in order to reduce the power dissipation and area. The DECOR transform exploits the correlation in the coefficients and data sequences to reduce the precision. Simulation results indicate that a decorrelated 8192-tap decimation filter with a decimation ratio of 64 results in a reduction of 5 bits in the coefficient and accumulator size. This corresponds to savings in complexity of 25%. In multi-stage decimation filters, it is shown that the decimation ratio of the last stage needs to be greater than 4 for DECOR to be useful.

I. Introduction

Oversampling analog-to-digital converter (ADC) techniques have been most popular in systems which need accuracy greater than 13 bits such digital audio, music synthesizers and voice coders. While the conversion rate and resolution of oversampling ADCs are typically determined by their analog components, the power consumption and die area are largely governed by the digital decimation filters [1]. In fact, digital decimation filter blocks occupy more than 60% of the total die area of oversampling ADCs. This paper applies the decorrelating (DECOR) transform [2] to FIR decimators to obtain low-power/low-area implementations. Using DECOR, the transfer function and/or the input is decorrelated such that fewer bits are required to represent coefficients and inputs. Thus the size of the arithmetic units, including ROM, multiplier, adder, and accumulator in the filter is reduced, reducing the power consumption and die area. The DECOR transform results in lower overhead and hence, a higher reduction in power consumption compared to other similar transforms [3]. The delta-sigma modulator in oversampling ADC systems and DECOR transforms are briefly reviewed in section II and III, respectively. In section IV, original filter coefficients and decorrelated coefficients in different FIR decimator architectures are applied to PDM signal to filter out-of-band noise. Then, the signal-to-noise ratio (*SNR*) is estimated along with the number of coefficient bit and power reduction.

II. The Delta-Sigma Modulator

In delta-sigma modulators, sampling and processing of the input signal are performed at an oversampled rate (f_{os}=OSR * f_{ns}), where f_{os} is the oversampling frequency, OSR is the oversampling ratio, f_{ns} is the Nyquist sampling frequency. Most oversampling ADCs are composed of a delta-sigma modulator and decimator. Fig. 1-(a) shows the first order delta-sigma modulator connected to an FIR decimator and Fig. 1-(b) shows the equivalent model of the first order delta-sigma modulator.

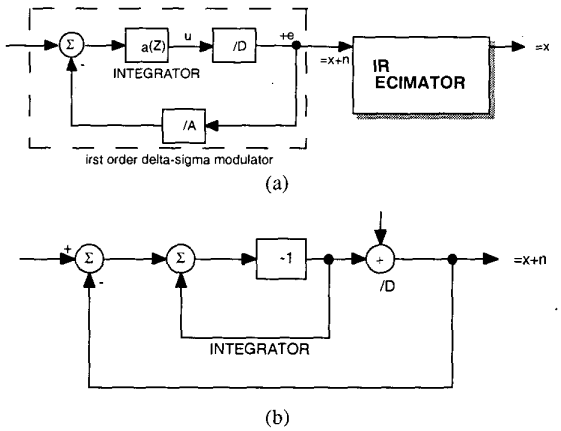

Fig. 1. The oversampling ADC system block diagram: (a) The first order delta-sigma modulator. (b) The equivalent model of the first order delta-sigma modulator.

$H_a(z)$ is the transfer function of the analog loop filter and $e(n)$ is the quantization noise. Analyzing this linearized circuit in the z-domain, the output is found to be

$$Y(z) = H_S(z)X(z) + H_N(z)E(z), \quad (1)$$

where $H_S(z)$ and $H_N(z)$ are the signal and noise transfer functions, respectively, and are given by

$$H_S(z) = \frac{H_a(z)}{H_a(z)+1} z^{-1} \quad (2)$$

$$H_N(z) = \frac{1}{H_a(z)+1} = 1 - z^{-1}, \quad (3)$$

where the loop filter transfer function $H_a(z) = z^{-1}/(1-z^{-1})$. Thus, the digital output contains a delayed replica of the analog input signal plus noise whose spectrum is that of the quantization noise $e(n)$ shaped by the noise transfer function, $H_N(z)$,

$$|H_N(e^{j\omega T})| = 2\sin(\omega T/2), \quad (4)$$

where $T = 1/f_{os}$ is the sampling period. For low frequencies, where $\omega T \ll 1$, $|H_N(z)| \approx \omega T$ indicating that $H_N(z)$ is a high-pass filter function. Thus, the noise power is swept out of baseband and into high frequencies where it can be eliminated by a low-pass digital decimation filter following the modulator stage. Extending equations (2) and (3), we obtain generalized equations for an L-th order delta-sigma modulator as follows,

$$H_S(z) = z^{-L} \quad (5)$$

$$H_N(z) = (1-z^{-1})^L \quad (6)$$

$$|H_N(e^{j\omega T})| = 2^L \sin^L(\omega T/2). \quad (7)$$

Fig. 2 shows the noise-shaping property of delta-sigma modulators.

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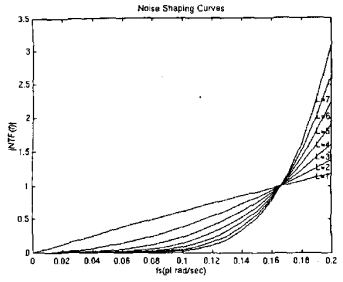

Fig. 2. Noise-shaping curves for various modulator orders *L*.

From Fig. 2, we see that as the modulator order increases more noise in baseband is shifted into the high frequency region. A 5-th order delta-sigma modulator with feedforward and feedback coefficients [4] was synthesized and simulated using the delta-sigma toolbox to create PDM a signal as an input for the decimation filter. The Hanning window is applied in order to reduce frequency sidelobes in estimating the *SNR* in the baseband. From Fig. 3, the estimated *SNR* is 116.1dB which corresponds to the effective number of bits being 18.99 obtained via the following equation [5],

$$SNR = 6.02\,N + 1.76dB, \qquad (8)$$

where N is the number of bits.

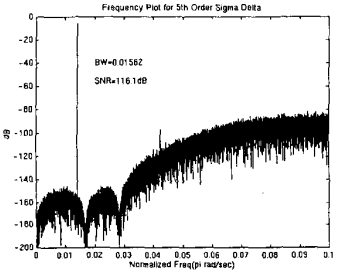

Fig. 3. The frequency plot and estimated *SNR* of a 5-th order delta-sigma modulator.

III. Low-Power Decimator Architectures

In this section, the DECOR transform is briefly reviewed and then applied to fixed coefficient FIR decimators.

A. The DECOR Transform and Decimation Filter

In DECOR, a finite-precision transfer function, $H(z)$, is transformed as:

$$H_{DECOR}(z) = H(z)\frac{(1+\alpha z^{-\beta})^m}{(1+\alpha z^{-\beta})^m} X(z). \qquad (9)$$

Note that the frequency response is not altered by DECOR as long as finite precision effects are considered. The numerator polynomial $H(z)(1 + \alpha z^{-\beta})^m$ results in a filter with decorrelated coefficients requiring fewer bits. However, the denominator $(1 + \alpha z^{-\beta})^m$ introduces a recursive section. In [2], values of $\alpha = -1$, $\beta = 1$, and $m=1$ were recommended for low-pass filters such as the decimator. One can easily verify that a symmetric filter such as the decimator is converted to an anti-symmetric filter and vice-versa when the DECOR transform is applied. The effectiveness of DECOR is increased with a reduction in the passband width, as would be in the case of decimation filter.

B. Low-Power Decimator Architectures

In the FIR decimator [6] shown in Fig. 4, the signal $x(n)$ is digitally filtered by a low-pass filter $h(n)$ with a digital cutoff frequency of π/M, where π is the normalized radian frequency corresponding to half the sampling frequency.

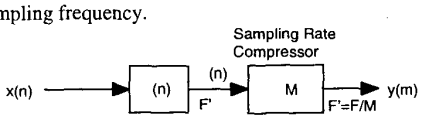

Fig. 4. Conceptual decimator block diagram.

It is clear that as the decimation ratio M increases, the filter bandwidth is reduced, thereby meeting the narrow passband condition for which DECOR is well suited. In practice, the decimation process is performed by computing only one out of every M outputs of the digital filter. A decimator with decimation ratio M can be implemented via a single or multi-stage architecture. Generally, a multi-stage decimator has smaller die size and power dissipation than does a single-stage decimator [6].

Fig. 5 shows a single-stage, 8192-tap, multiplier-free decimator with a decimation ratio of 64 and 1-bit data input.

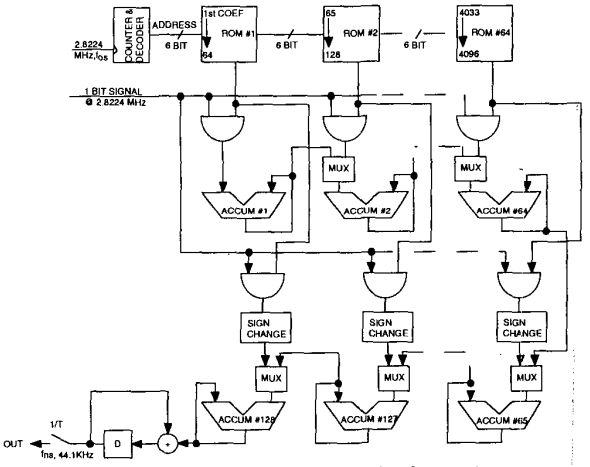

Fig. 5. Single-stage multiplier-free decimator.

The first-half decorrelated coefficients are stored in a 64 page read-only-memory (ROM), each page with 64 words. The sign change is inserted in Fig. 5 to account for the anti-symmetry in the second-half decorrelated coefficients. Fig. 6 shows the decimator block diagram. These can be easily derived from the architecture in [7]. It was assumed that the 2's complement number system was used. The sign change block was inserted to invert the sign of the filter coefficients in the second half of the decimation filter. Further, instead of changing the sign of the coefficient, the sign of the data input is changed.

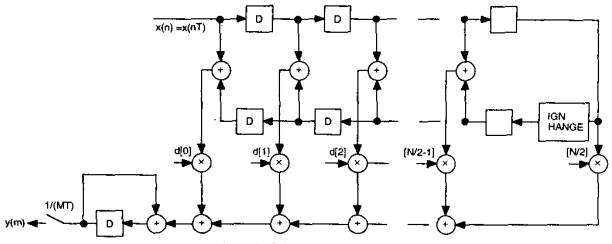

Fig. 6. The decimator block diagram.

IV. Application of DECOR to FIR Decimator

Here, we apply DECOR to typical decimator configurations, including: 1.) a multiplier-free single-stage decimator with a decimation ratio of 64, 2.) a two-stage decimator consisting of a stage of decimation ratio 32 followed by a stage of decimation ratio 2 and 3.) a two–stage decimator consisting of a stage of decimation ratio 16 followed by a stage of decimation ratio 4. This is done in order to determine the range of parameter for which DECOR is effective. Also, the amount of coefficient bit-width reduction is estimated without any rounding or truncation at the multiplier or accumulator output, and the SNR will be estimated before and after applying DECOR. For numerical simulations, the filter coefficients are generated using the Parks-McClellan algorithm. The digital audio specifications (OSR=64, f_{ns}=44.1KHz) [8] were used in our simulations.

A. Single-stage Decimator

Fig. 7–(a) shows the original and decorrelated 8192-tap coefficients of a single-stage decimator with a decimation ratio of 64 and Fig. 7–(b) shows its magnitude response.

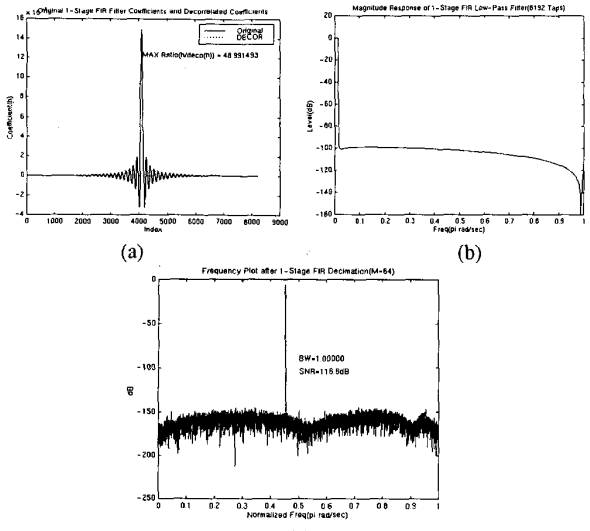

Fig. 7. (a) The original and decorrelated 8192-tap coefficients of single-stage decimator. (b) The magnitude response of Fig. 7-(a).
The frequency plot of the decimator output using the original and decorrelated coefficients of Fig. 7-(a).

As shown in Fig. 7-(c), we get identical frequency responses and *SNRs* (116.6dB) using the original and decorrelated coefficients.
From Fig. 7-(a), we obtain the ratio, 48.99, between the maximum magnitudes of original and decorrelated coefficients, which results in coefficient bit-width reduction of 5 bits.

B. Multi-stage Decimator

Fig. 8–(a) shows a two-stage decimator consisting of stages with decimation ratios 32 and 2. Fig. 8–(b) shows the original and decorrelated coefficients of the two-stage decimator and Fig. 8–(c) shows the magnitude responses of Fig. 8–(b).

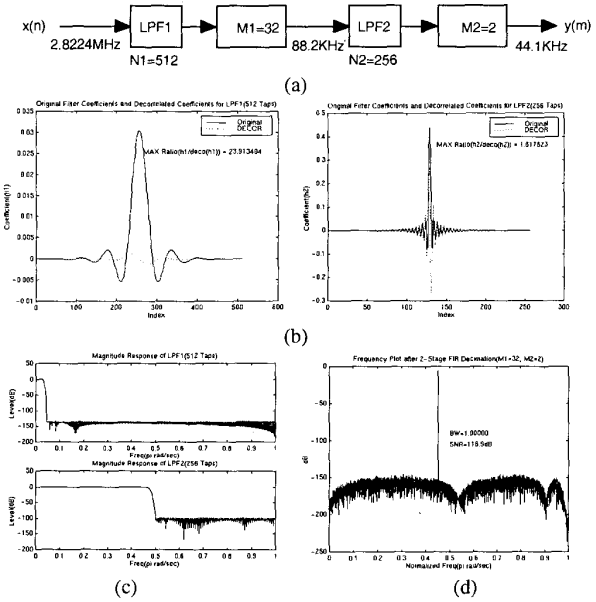

Fig. 8. (a) Two-stage decimator block diagram with 32, 2 decimation ratio in first and second stage. (b) The original and decorrelated coefficients of LPF1 and LPF2 for Fig. 8-(a). (c) The magnitude response of LPF1 and LPF2 corresponding to Fig. 8-(b). (d) The frequency plot of the decimator output using the original and decorrelated coefficients of Fig. 8-(b).

Again, as shown in Fig. 8–(d) we get identical *SNRs* (116.9dB) using the original and decorrelated coefficients. From Fig. 8-(b), we get 4-bit coefficient reduction in LPF1, but no bit coefficient reduction in LPF2. This is due to the fact that the bandwidth of LPF2 is 0.4535π. According to [2], DECOR is effective in power and area reduction for filter bandwidths ranging from 0.3π to 0.05π. Thus the simulation results well agree with this condition.
For another example, a two-stage decimator consisting of a stage of decimation ratio 16 followed by a stage of decimation ratio 4 shown in Fig. 9-(a) was simulated. Fig. 9–(b) shows the original and decorrelated coefficients of the two-stage decimator and Fig. 9–(c) shows the magnitude responses of Fig. 9–(b). From Fig. 9–(d), we get identical *SNRs* (116.9dB) using the original and decorrelated coefficients. From Fig. 9-(b), we get 4-bit coefficient reduction in LPF1 and 1-bit coefficient reduction in LPF2. The bandwidth of LPF1 is 0.01415π and that of LPF2 is 0.2268π.

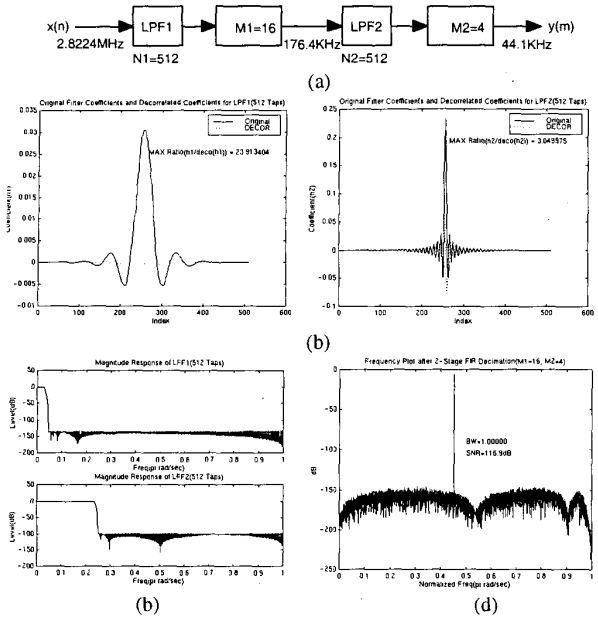

Fig. 9. (a) Two-stage decimator block diagram with 16, 4 decimation ratio in first and second stage. (b) The original and decorrelated coefficients of LPF1 and LPF2 for Fig. 9-(a). (c) The magnitude response of LPF1 and LPF2 corresponding to Fig. 9-(b). (d) The frequency plot of the decimator output using the original and decorrelated coefficients of Fig. 9-(b).

This simulation result implies that DECOR is useful in multi-stage decimators, where decimation ratio in the last stage is greater than 4. Table 1 summarizes the simulation results.

Decimator architectures	Bandwidth	Bit reduction	Transistor count reduction
Single-stage decimator with decimation ratio of 64	0.01415π	5 bit	25 %
LPF1 of two-stage decimator with decimation ratios of 32,2	0.01415π	4 bit	22 %
LPF2 of two-stage decimator with decimation ratios of 32,2	0.4535π	0 bit	0 %
LPF1 of two-stage decimator with decimation ratios of 16,4	0.01415π	4 bit	22 %
LPF2 of two-stage decimator with decimation ratios of 16,4	0.2268π	1 bit	8 %

Table 1. The summary of simulation results.

Considering the N-stage decimator with decimation ratio M_i at i-th stage, the bandwidth of k-th stage is given by,

$$BW_k = \frac{\pi}{\prod_{i=k}^{N} M_i}. \qquad (10)$$

Equation (10) indicates that the earlier stage has much narrower bandwidth than later stage resulting in more power and area reduction. Generally, OSR is identical to the overall decimation ratio M,

$$M = \prod_{i=1}^{N} M_i. \qquad (11)$$

Therefore increasing the OSR improves the effectiveness of DECOR in reducing the power and area of the decimator by narrowing the bandwidth of the decimator.

V. CONCLUSION

In this paper, the DECOR transformation has been applied to decimation filters to reduce the power and area. The decimation process was performed using a PDM signal generated from 5-th order delta-sigma modulator with OSR of 64 and original and decorrelated coefficients of various decimator architectures. The *SNR* was compared and the bit-width reductions in filter coefficients were measured to verify the effectiveness of DECOR to the decimation process.

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REFERENCES

[1] B. P. Brandt and B. A. Wooley, "A low-power, area-efficient digital filter for decimation and interpolation," *IEEE J. Solid-State Circuits*, vol. 29, pp. 679-687, June 1994.

[2] S. Ramprasad, N. R. Shanbhag, and I. N. Hajj, "Decorrelating (DECOR) transformations for low power digital filters," *IEEE Trans. Circuits Syst. – II*, vol. 45, pp. 776-788, June 1999.

[3] N. Sankarayya, K. Roy, and D. Bhattacharya, " Algorithms for low power and high speed FIR filter realization using differential coefficients," *IEEE Trans. Circuits Syst. – II*, vol. 44, pp. 488-497, June 1997.

[4] K. C. Chao, S. Nadeem, W. L. Lee, and C. G. Sodini, "A higher order topology for interpolative modulators for oversampling A/D converters," *IEEE Trans. Circuits Syst.*, vol. 37, pp. 309-318, March 1990.

[5] Behzad Razavi, " Data Conversion System Design," *IEEE Press*, pp. 96-101.

[6] S. R. Norsworthy, R. Schreier, and G. C. Temes, "Delta-sigma data converters," *IEEE Press*, pp. 406-444.

[7] A. V. Oppenheim, and R. W. Schafer, "Discrete-time signal processing," *Prentice Hall*, pp. 313-317.

[8] Ken C. Pohlmann, "Principles of Digital Audio," *McGraw Hill*, pp. 549-559.