Analytical Expressions for Power Dissipation of Macro-blocks in DSP Architectures*

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Abstract

Power minimization is an important objective in present day VLSI design. Macromodels for power dissipation can be used to estimate power at a high-level of abstraction. High-level power estimation methods provide the designer with more flexibility to explore design trade-offs early in the design cycle. In this paper, we present closed-form analytical expressions for power consumption of macro-blocks in terms of the word-statistics. We present an analytical expression for total bit transition activity of a signal line in terms of the word-statistics. We also present analytical power models for macro-blocks in DSP architectures in terms of total bit transition activity and other parameters. Experimental results validating the analytical expressions are also included in this paper.

1 Introduction

Power dissipation is a critical issue in present day VLSI circuit design. Integrated circuits with large power dissipation require expensive packaging to ensure proper heat dissipation. Excessive power dissipation results in over-heating of the components in the circuit and makes them susceptible to failure. Integrated circuits used in portable applications need to consume less power because it extends the battery life. In the design for low power, optimization at the RTL level gives significant power savings compared to gate level or circuit level optimizations. An accurate estimate of power is required at a high-level of abstraction to explore the design space and make design decisions for synthesis of low-power circuit. In DSP architectures, it is necessary to estimate power for a given hardware data flow graph (DFG) or the RTL description of the fixed point (finite precision) implementation of an algorithm. Each node in the hardware DFG corresponds to a macro-block. The total power dissipation associated with a particular hardware DFG is the sum of the power dissipated by each of the macro-blocks in the hardware DFG. Hence, we require accurate models for the power dissipation of macro-blocks to obtain total power dissipation of the DSP circuit represented by the hardware DFG.

DSP architectures are modular and consist of instantiations of macro-blocks such as multiplexers, registers, adders, and multipliers. The purpose of power characterization of macro-blocks is to obtain accurate and simple power models. The power dissipated by a macro-block is input-pattern dependent and hence it is dependent on the input word-statistics. The word-statistics of the signal lines at the input and the output of a node in the hardware DFG can be obtained using transfer function evaluation or by propagating the input statistics. The developed power macromodel must yield correct results for different input statistics and be scalable for different word-lengths.

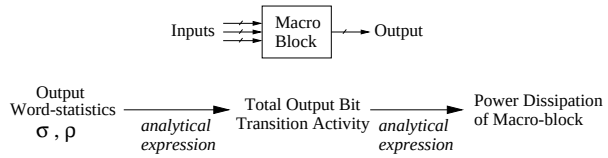

Figure 1: Outline of our approach for power characterization of macro-blocks

There exists a number of techniques for power characterization of macro-blocks. In [1, 2], the authors use random input vectors to characterize the power dissipation of a module. However, the power dissipation of a macro-block can be shown to be strongly dependent on the input statistics. The inability of the these methods to account for the dependence of power dissipation on the input statistics results in an inaccurate model. In [3–5], the authors propose different techniques that account for the dependence of power dissipation on input statistics. In [3], the authors present activity sensitive capacitance models for various library components. The Dual bit type (DBT) model accounts for both the LSB and MSB (sign bit) behavior. In [4], a 3D-table look-up model was proposed for estimating the power consumed by a circuit for any given input/output signal statistics. The 3D-look up table can be constructed by an automatic characterization process. In [5], the authors use RTL cycle-based simulation to estimate the zero-delay statistics and switching activity. Word-level models for glitching activity with about 9 variables are also presented. Our work targets characterization of macro-blocks in DSP architectures and differs from the previous methods in one or more of the following aspects:

- We present simple *closed-form analytical expressions* (macromodel) for power dissipation of macro-blocks in terms of the word-statistics.
- Macromodel evaluation is easy and straight forward and it does not require any simulations.
- Macromodels are scalable (valid for various word-lengths) and give accurate results for various input statistics.

In this work, we present analytical expressions for power dissipated by a macro block in terms of the word-statistics of the output of a macro-block. Fig. 1 shows the outline of the scheme. The main parameter used in the power characterization of a macro-block is the total output bit transition activity. In the following sections, we will show that the

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power dissipation is strongly dependent on the total output bit transition activity. The total output bit transition activity can account for the variation in power dissipation due to different input statistics and the word-length of the macro-block. For some macro-blocks, we include additional parameters such as word-length into the macromodel to improve the accuracy of the model. We present a closed-form analytical expression for computing the total bit transition activity from the word-statistics. This expression is developed using the break-points presented in [3] and the analytical expression for MSB activity. Details of these analytical expressions are presented in the subsequent sections. In [6], an exact and approximate method are proposed to compute the bit correlation coefficient which is used to compute the total bit transition activity. However, unlike [6] we present closed-form analytical expressions for total bit transition activity. In addition, we characterize and present analytical expressions for the power dissipation of macro-blocks using total bit transition activity.

In this paper, we focus on the power characterization of macro-blocks used in digital filters such as adders, delays, multiplexers, and multipliers with a fixed coefficient. This method can be applied to other macro-blocks as well. In this work, we ignore the glitching activity at the inputs to the macro-block. This is because high performance DSP architectures are highly pipelined. We assume that the inputs to the macro-block are fed from latches. The power dissipation of a macro-block is obtained using MED [7], a gate level power estimator with real-delay logic simulations that accounts for glitching activity. Hence, the power dissipation due to glitching activity at nodes in the circuit is taken into account.

This paper is organized as follows: In Section 2, we describe the relationship between signal statistics at the input or output of a macro-block and the power dissipation of the macro-block. In Section 3, we use the analytical expression for total bit transition activity to characterize the power dissipation of multiplexers. In Section 4, we present the power characterization of adders. In section 5, we present the power characterization of Baugh-Wooley array multiplier with a fixed coefficient. In section 6, we present the application of the power macromodels to digital filter circuits. Finally, in section 7 we present the conclusions.

2 Signal statistics for power characterization

The power dissipated by a circuit is dependent on the input vectors applied to the circuit. The statistics at inputs to the circuit are used to capture the *average* behavior of the input vectors. The power dissipation of a circuit can be shown to be a function of the average bit-statistics of the output and the input signal lines [4]. Hence, in order to characterize the power dissipation of a circuit at a high level of abstraction, it is necessary to obtain the bit-statistics at the all input and output signal lines and establish a relationship between the bit-statistics and the power dissipation. The bit-statistics can be obtained either by RTL simulations or from the word-statistics.

In DSP architectures, at the algorithm (RTL) level of abstraction the word-statistics *mean*(μ), *variance*(σ^2), *correlation coefficient*(ρ) and the word-length of all signal lines are

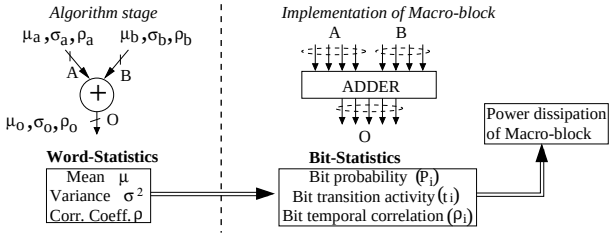

Figure 2: Relationship between signal statistics and power dissipation

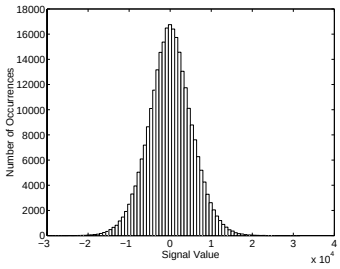

Figure 3: Histogram of word-values for Audio2

specified or they can be computed from the word-statistics of the inputs to the circuit. In order to estimate the power dissipation at this level of abstraction, it is necessary to characterize the power dissipation in terms of the word-statistics. Fig. 2 shows the relationship between signal statistics and the power dissipation of the macro-block. DSP circuits consist of instantiations of macro-blocks like adders and multipliers. Hence, pre-designed circuits for each of these macro-blocks can be used. In order to estimate power at the RTL level of abstraction, it is necessary to establish a functional relationship between the word-statistics, bit-statistics and the power dissipated by the macro-block as shown in Fig. 2.

2.1 Word-Statistics

In this section, we describe techniques to obtain the bit vectors and bit-statistics from word-statistics. In order to compute the bit-statistics from the word-statistics, the probability distribution (mass function) of the word-values and the bit representation of the word-values are required. Many DSP inputs can be closely approximated by a Gaussian process. Fig. 3 shows a histogram of the signal values of Audio2, a 16 bit audio signal. From the figure, it can be seen that the distribution of the word-values can be approximated by a Gaussian distribution. In this work, we assume that the input signal is generated by a zero-mean Gaussian random process. This is not a restrictive assumption as a number of signals like speech and music signals can be considered to be zero-mean Gaussian signals. Signals in DSP systems are represented in finite precision using a certain signal encoding. In this work, we consider the two's-complement encoding of the signals. Although the analytical expressions for bit-statistics are obtained assuming a Gaussian distribution of the word values, these results closely approximate the bit-statistics for any symmetric distribution centered about zero amplitude. The expressions for the bit-statistics in terms of the word-statistics are described in our previous work [8]. Due to the dependencies among the bit-statistics, all the bit-statistics are not required for power characterization. In the next sub-section, we describe the relationship between the bit-statistics and the power dissipation of a macro-block. The

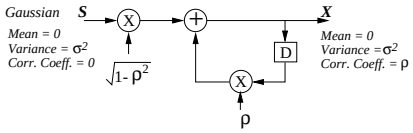

Figure 4: Signal generation model

average power dissipated by a circuit is obtained by gate-level simulations. These simulations require generation of bit-vectors for the specified word-statistics. The signal generation model described in section 2.1.1 is used to generate the bit vectors for the given word-statistics.

2.1.1 Signal generation model

Power characterization requires gate level simulation and it requires generation of word-values for a large number of word-statistics. A signal generation model is necessary to generate word-values for any given word-statistics. In this work, we use a lag-one auto regressive AR(1) model to generate the word-values for the specified statistics. The bit vectors are obtained using the two's-complement representation of the word-values. The signal generation model shown in Fig. 4 is used to generate the input signals for all the simulations described in this paper. For each simulation run, 10000 input vectors are generated.

2.2 Bit-Statistics

In this sub-section, we present a description of the bit-statistics that can be used to characterize the power dissipation of a macro-block. The power dissipation of a macro-block was related to the *average input bit probability*, *average input transition activity*, and *average output transition activity* in [4]. In [8], it was shown that for a zero-mean Gaussian signal the average bit probability is a constant (0.5) and is independent of the word-statistics. Hence, the power dissipation can be approximated as a function of bit transition activity. In this work, we use the total output bit transition activity to characterize the power dissipation. Total output bit transition activity is the sum of the transition activity of all output bits. It will be shown in subsequent sections that the power dissipation of macro-blocks is a strong function of total output bit transition activity. In next sub-section, we use the dual bit model and present the expression for total bit transition activity.

2.2.1 Total Bit Transition Activity

The dual bit-type (DBT) model for word-level signals was proposed in [3]. The DBT model has two break points, BP_0 and BP_1, that are computed using the word-level statistics of the signal. The expressions for the break points BP_0, BP_1 presented in [3] are given by Eqns. (1) and (2).

$$BP_0 = log_2(\sigma) + log_2(\sqrt{1-\rho^2} + |\rho|/8) \quad (1)$$

$$BP_1 = log_2(3\sigma) \quad (2)$$

In this work, we use the above break-points to compute the average bit transition activity. The uniform white noise model is valid for the least significant bits up to the break point BP_0. The transition activity of these bits is 0.5. The transition activity of the sign bits, bits from the most significant bit to BP_1 is given by the following expression [9],

$$t_{msb} = \frac{1}{\pi} cos^{-1}(\rho). \quad (3)$$

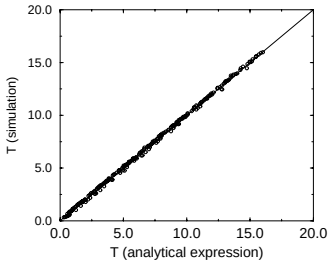

Figure 5: Validation of expression for total bit transition activity

Table 1: Total bit transition activity for real signals

Name	W_L	μ	σ	ρ	$\mathbf{T}^e$ Expt.	$\mathbf{T}$ Theor.	% error
Audio1	16	0.0	8191.7	0.9854	6.8704	6.6224	-3.61
Audio2	16	1.1333	5347.3	0.8541	6.9760	6.9696	-0.09
Audio3	16	-140.35	5312.4	0.9455	6.5024	6.6512	2.29
Audio4	16	-2.8609	3434.4	0.9835	5.8560	6.0896	3.98
Audio5	16	-2.9087	3469.2	0.9884	5.7264	6.0240	5.19
Audio6	16	-2.8637	3438.3	0.9219	6.5472	6.5232	-0.36
Audio7	16	1.4285	7349.2	0.9628	6.4240	6.7440	4.98
Audio8	8	-0.6898	12.1936	0.9402	2.2560	2.3792	5.46
Audio9	8	-0.6979	12.9297	0.9198	2.3792	2.5120	5.58
Audio10	8	-0.6947	18.2008	0.9400	2.5240	2.6056	3.23

For the bits between BP_0 and BP_1 a linear approximation between 0.5 and t_{msb} is used to obtain the bit transition activity. The total bit transition activity ($\mathbf{T}$) is the sum of the bit transition activity values. It is given by the following expression,

$$\mathbf{T} = 0.5 \;\; BP \;\; + \;\; (W_L - BP) \;\; \frac{1}{\pi} cos^{-1}(\rho), \quad (4)$$

where W_L is the signal word-length, and BP is the average value of the break points BP_0, BP_1.

2.2.2 Validation for real and synthetic signals

In this sub-section, we present the experimental validation of the analytical expression for total bit transition activity. The total bit transition activity is computed analytically using Eqn. (4) and experimentally for various synthetic signals and real signals. The synthetic signals are generated using the signal generation model described in section 2.1.1. We first present the results for synthetic signals. Fig. 5 shows a scatter plot of the total bit transition activity $\mathbf{T}$ obtained using the analytical expression and simulation for different values of W_L (4, 8, 12, 16, 20, 24, 28, 32), ρ (0.0, 0.25, 0.5, 0.75, 0.9, 0.95, 0.99) and 5 different σ^2 values spread over the entire range (minimum variance to maximum variance). It can be seen that there is a good match between the results obtained by simulations and the analytical expression. The average absolute error was found to be 2.8%. We now present the experimental validation of the analytical expression for total bit transition activity using real signals. Table 1 shows the total bit transition activity obtained using the analytical expression (Theor.) and experimentally (Expt.) for real signals. It can be seen that there is a good match between the theoretical and experimental values.

3 Power Characterization using Total Output Bit Transition Activity

The total bit transition activity is a function of the word-length, and the word-statistics. Eqn. (4) shows the relationship between total bit transition activity and word-length,

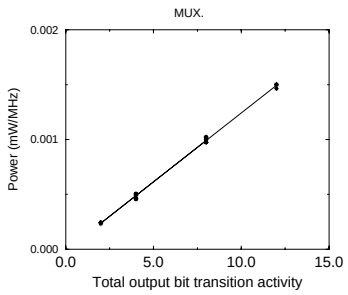

Figure 6: Variation of power with total output bit transition activity for a multiplexer

word-statistics. The power dissipation of the macro-blocks is a strong function of the total output bit transition activity ($\mathbf{T}$). Power characterization using total output bit transition activity reduces the number of variables and gives simple analytical relationships. This is because it can account for the variation in power dissipation due to different input statistics and different word-lengths. In this section and subsequent sections we present experimental results that relate the power dissipation of the macro-blocks to the total output bit transition activity.

In this work, the power dissipation values are obtained by using MED [7], a gate level power estimator. Since the simulator uses a real-delay model, it can account for the glitching activity in the circuit. An extended simulation for 10000 input vectors is performed to obtain an estimate of the average power dissipation. The input vectors are generated using the signal generation model shown in Fig. 4. A gate-level netlist is generated for each of the circuits using a gate library with delay and capacitance values typical of a 0.5μ CMOS technology.

The power characterization of multiplexers, registers and other similar data-path elements using total output bit transition activity is straight forward. This is because there is no interaction between different bit slices, and the capacitance associated with each bit is approximately the same for all bits. Hence, the power dissipation is a linear function of the total output bit transition activity ($\mathbf{T}$). Multiplexers are typically used in folded architectures, where multiple operations are mapped on to the same hardware unit. Fig. 6 shows the variation of power dissipation of a multiplexer with the total output bit transition activity. The simulations were performed for different word-lengths ($W_L = 4, 8, 16, 24$). For each word-length the total output bit transition activity was varied by choosing different input statistics. For instance, for a 24 bit signal ($\mathbf{T} = 12, 8, 4$) were used. From the plot it can be seen that there is a linear relationship between the power dissipation and total output bit transition activity. The coefficients of this linear relationship were obtained by least squares fit and are given in the following equation,

$$P_{mux} = 0.0001255\ \mathbf{T} - 1.359 \times 10^{-05}\ \text{mW/MHz}. \qquad (5)$$

Similar models can also be developed for other data-path elements. The power macro-model for multiplexers given by Eqn. (5) is compact and is accurate for a large number of statistics. The analytical expression can be used for all input word-lengths greater than 4 and for all $\mathbf{T}$ values computed using the word-statistics in Eqn. (4).

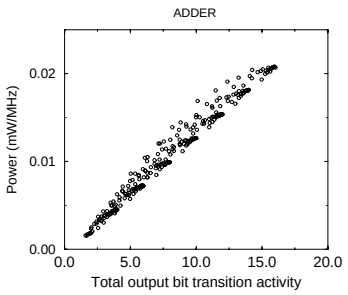

Figure 7: Variation of power with total output bit transition activity for adder

4 Adder Power Characterization

Adders are the most commonly used components in application specific processors and DSP architectures. In this paper, we present the power characterization of ripple carry adders. Power characterization for other adders can be performed using a similar method. Simulation results for circuits with input word-length W_L = 4, 8, 12, 16, 20, 24, 28, 32, are used for power characterization. For each circuit, simulations are performed for the following output word-statistics: ρ values 0.0, 0.25, 0.5, 0.75, 0.9, 0.95, 0.99 and two different σ^2 values spread over the entire range (minimum variance to maximum variance). For each choice of output statistics (ρ, σ^2) the simulations are performed for two different sets of input statistics. Fig. 7 shows the variation of power with total output bit transition activity for various word-statistics and word-lengths. It can be seen that the power dissipation of an adder is approximately a linear function of the total output bit transition activity. In our experiments, we observed that the spread or deviation of the power dissipation values from the linear relationship was for circuits with larger word-length. These higher power dissipation values for circuits with larger word-length at the specified total output bit transition activity could be due to the increased glitching activity in the circuits. To account for the spread, we included word-length as one of the parameters and used least square regression techniques to find the coefficients of the analytical expression. The following expression is the analytical model for the power dissipation of a ripple carry adder,

$$\begin{aligned} P_{addr} = \quad & 0.00106\ \mathbf{T} + 1.6439 \times 10^{-04}\ W_L \\ & -9.5627 \times 10^{-04}\ \text{mW/MHz}. \end{aligned} \qquad (6)$$

Simulation results for circuits with input word-length W_L = 6, 10, 14, 18, 22, 26, 30, are used to validate the analytical model for power dissipation of the ripple carry adder. For each circuit, simulations are performed for the following output word-statistics: ρ values 0.0, 0.25, 0.5, 0.75, 0.9, 0.95, 0.99 and two different σ^2 values spread over the entire range (minimum variance to maximum variance). For each choice of output statistics (ρ, σ^2) the simulations are performed for two different sets of input statistics. Fig. 8 is a scatter plot of the power dissipation obtained using the analytical expression and simulation results. It can be seen that the analytical model is accurate. The average absolute error was found to be 4.39%. The power macro-model for ripple carry adder given by Eqn. (6) is compact and is valid for a large number of statistics. The analytical expression can be used for all input word-lengths greater than 4 and for all $\mathbf{T}$ values computed using the word-statistics in Eqn. (4).

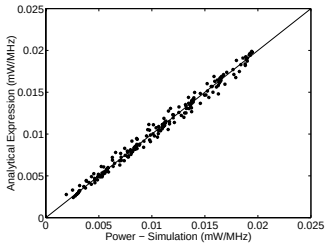

Figure 8: Validation of analytical expression for adder power dissipation

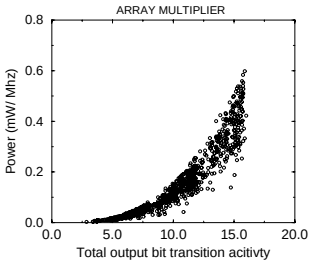

Figure 9: Variation of power with total output bit transition activity for multiplier

5 Multiplier Power Characterization

Array multipliers are commonly used in high performance DSP architectures. In this paper, we present the characterization of a Baugh-Wooley two's-complement array multiplier with a fixed coefficient. Simulation results for circuits with input word-length $W_L = 4, 8, 12, 16$ are used for power characterization. For each circuit, simulations are performed using the following input word-statistics: ρ values 0.0, 0.25, 0.5, 0.75, 0.9, 0.95, 0.99 and three different σ^2 values spread over the entire range (minimum variance to maximum variance). For each choice of input statistics (ρ, σ^2) the simulations are performed for 10 randomly chosen coefficients. Fig. 9 shows the variation of power with total output bit transition activity for various input statistics and random coefficients. It can be seen that there is a strong dependence of power dissipation on total output bit transition activity. Accurate power characterization of a fixed coefficient array multiplier is a hard problem. This is because for a given coefficient word-length W_L, there can be 2^{W_L} different coefficients. Hence, it is unlikely that a simple analytical expression would give highly accurate results. Our approach is to identify the parameters that have a strong influence on the power dissipation of the array multiplier and use them for power characterization. Although the power dissipation is strongly dependent on the total output bit transition activity, a number of different input statistics and coefficients can give approximately the same total output bit transition activity. This causes spread in the power dissipation values for a particular value of the total output bit transition activity. For instance, the coefficients 65 (01000001) and 63 (00111111) will result in approximately the same output word-statistics for the same input statistics. Hence, the multipliers with these coefficients will have approximately the same total output bit transition activity. But the power dissipated by the array multiplier with coefficient 63 is more than the power dissipated by the array multiplier with coefficient 65. This results in the different power dissipation values for the same total output bit

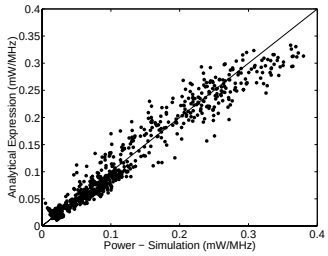

Figure 10: Validation of analytical expression for multiplier power dissipation

transition activity. To account for the spread, a parameter N_h which denotes the number of logic high bits in the coefficient is used. N_h denotes the number of rows in the array multiplier for which the partial products are evaluated for each input vector. These partial products are added to obtain the output bit values of the multiplier for that input vector. The parameters $\mathbf{T}$ and N_h are used to characterize the power dissipation of the multiplier. The coefficients of the analytical expression are obtained using least square regression techniques. The following expression is the analytical model for the power dissipation of a Baugh-Wooley two's-complement array multiplier with a fixed coefficient,

$$P_{mult} = 0.00228\ \mathbf{T}^2 + 0.00268\ N_h\mathbf{T} - 0.02858\ \mathbf{T} - 0.01851\ N_h + 0.12106\ \text{mW/MHz}. \quad (7)$$

Simulation results for circuits with input word-length $W_L = 6, 10, 14$ are used to validate the analytical model for power dissipation of the multiplier. For each circuit, simulations are performed using the following input word-statistics: ρ values 0.0, 0.25, 0.5, 0.75, 0.9, 0.95, 0.99 and three different σ^2 values spread over the entire range (minimum variance to maximum variance). For each choice of input statistics (ρ, σ^2) the simulations are performed for 10 random coefficients. Fig. 10 is a scatter plot of the power dissipation obtained using the analytical expression and simulation results. It can be seen that the analytical model is reasonably accurate. The average absolute error was found to be 21.73%. More complex models that use certain parameters derived from the coefficient can be used to improve the accuracy of the model. The power macro-model for Baugh-Wooley two's-complement array multiplier with a fixed coefficient given by Eqn. (7) is compact and is valid for a large number of statistics. The analytical expression can be used for all input word-lengths greater than 4, for all N_h values greater than 0 and for all $\mathbf{T}$ values computed using the word-statistics in Eqn. (4).

6 Application of Power Macromodels to Digital Filter Circuits

In this section, we use the power macromodels presented in the paper to compute the power dissipation of digital filter circuits. We also present comparisons with accurate gate level power estimation of the filter circuits using MED [7] to validate the power values obtained by using the analytical power models. Fig. 11 shows a second order FIR filter. The input signal is a zero-mean Gaussian signal with variance (σ^2), correlation coefficient (ρ) and it is generated using the signal generation model described in section 2.1.1. Since the

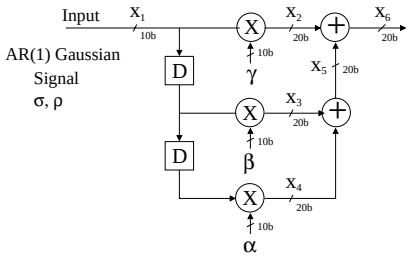

Figure 11: Second order FIR filter

Table 2: Results for the second order FIR filter

Inp. Stats.		Filter Coeff.			Power (P^a)	Power (P)	% error
σ_1	ρ_1	α	β	γ	Anal. Expr.	MED sim.	
170	0.0	143	287	399	0.3637	0.3612	0.69
		127	271	399	0.3729	0.3617	3.09
		15	143	271	0.3364	0.3010	11.76
128	0.5	143	287	399	0.2924	0.3353	-12.79
		127	271	399	0.2970	0.3365	-11.74
		15	143	271	0.2501	0.2795	-10.52

input (X_1) is a zero-mean Gaussian signal, all the internal signals (X_2, X_3, X_4, X_5) and the output signal (X_6) are zero-mean Gaussian signals. Hence, the total bit transition activity can be computed at all these signal lines using the word-statistics in the analytical expression (Eqn. 4). The word-statistics at all the internal signal lines and the output signal line can be computed in terms of the input word-statistics (σ, ρ) and the coefficients of the filter by propagating the statistics. The word-statistics at signal lines X_2, X_3, X_4 are given by,

$$\sigma_2^2 = \gamma^2\sigma^2 \; ; \quad \sigma_3^2 = \beta^2\sigma^2 \; ; \quad \sigma_4^2 = \alpha^2\sigma^2 \; ; \quad \rho_2 = \rho_3 = \rho_4 = \rho$$

The word-statistics at signal line X_5 are given by,

$$\sigma_5^2 = (\alpha^2 \; + \; \beta^2 \; + \; 2\alpha\beta\rho) \;\; \sigma^2$$

$$\rho_5 = \frac{(\alpha^2+\beta^2)\rho \; + \; \alpha\beta(1+\rho^2)}{\alpha^2 \; + \; \beta^2 \; + \; 2\alpha\beta\rho}$$

The word-statistics at signal line X_6 are given by,

$$\sigma_6^2 = [(\alpha^2+\beta^2+\gamma^2) \; + \; 2\beta\rho(\alpha+\gamma) \; + \; 2\alpha\gamma\rho^2] \;\; \sigma^2$$

$$\rho_6 = \frac{(\alpha^2+\beta^2+\gamma^2)\rho \; + \; 2(\alpha+\gamma)(1+\rho^2) \; + \; \alpha\gamma\rho(1+\rho^2)}{(\alpha^2+\beta^2+\gamma^2) \; + \; 2\beta\rho(\alpha+\gamma) \; + \; 2\alpha\gamma\rho^2}$$

The word-statistics at all the signal lines can be obtained by using the values of the input statistics and the coefficients in the above expressions. Using the word-statistics and the word-length, the total bit transition activity can be computed at all the signal lines. The total bit transition activity can be used in the analytical expressions for the power dissipation of adders and multipliers to obtain an estimate of the power dissipated by the DSP filter circuit.

Table 2 shows the power dissipation computed using the analytical expressions and using accurate gate level power estimation tool, MED [7] for different sets of coefficients of the FIR filter. For each set of coefficients, we use two different input statistics and compute the power values. The units for the power dissipation values (P^a, P) is (mW/ Mhz). From the results, it can be seen that there is a close match between the power values obtained using the analytical expressions and gate level power estimation using MED.

7 Conclusion

In this paper, we presented *closed-form analytical expressions* for the power dissipation of macro-blocks in DSP architectures. We first presented an analytical expression for the total bit transition activity in terms of the word-statistics. Analytical expressions for the power dissipation of macro-blocks were presented in terms of the total output bit transition activity and other parameters like word-length. The analytical expressions are simple and easy to evaluate. They are valid for a wide range of word-statistics and are scalable with word-length. These analytical expressions for power dissipation of macro-blocks can be used in a high-level synthesis tool to obtain power-optimal circuits. We also presented experimental validation of all the analytical models developed in this paper. The average absolute error in the expression for the total bit transition activity was found to be 2.8%. The average absolute error in the expressions for the power dissipation of a ripple carry adder and Baugh-Wooley two's-complement array multiplier with a fixed coefficient was found to be 4.39% and 21.73% respectively.

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